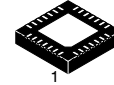# 3-Phase Gate Driver, 60 V

NCD83591

QFN28 4x4, 0.4P
CASE 485GF

Overview

The NCD83591 is an easy to use, multi−purpose 3−phase gate−driver optimized for low BOM cost. The wide operating voltage range make this device ideal for industrial and commercial applications from 5 V (min) up to 60 V (max).

Features

- Operation from 5 V to 60 V Supply Voltage with Tolerance from 4 V to 70 V
- Constant Current Drive of Power FET, Configurable from 5 mA to 250 mA (16 Settings by Input Level to VDRV Pin)
- Internally Generated Gate Drive Supply Voltages
- Tolerant to −12 V DC for High Side Gate and Source Output Pins
- Gate Sensing for Cross Conduction Protection and Optimized Dead Time
- Embedded High GBW General Purpose Amplifier (Intended for Current Sensing and Externally Configurable)
- Embedded Charge Pump Function Allowing DC Static Drive
- Strong Hold−off Current Preventing Self−turn−on
- Internal Gate Pull−down to GND during Loss of VDD (Core) Power
- Under Voltage Lock Out on VM, VGL, and VGH−VM
- 5 V/3.3 V Compatible 6 Input Control Plus Enable
- Up to 30 kHz Motor PWM with Individual Six Gate Control Mode
- 4 kV HBM and 1 kV CDM ESD Protection
- This is a Pb−Free Device

Applications

- Power Tools
- Industrial Actuators and Cobots
- Automated Guided Robots
- Light Mobility (E−Bikes, E−scooters, Hoverboards)

MARKING DIAGRAM

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 o
   83591
   AWLYWW
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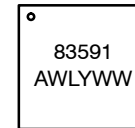
83591 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCD83591MNTXG	QFN28 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
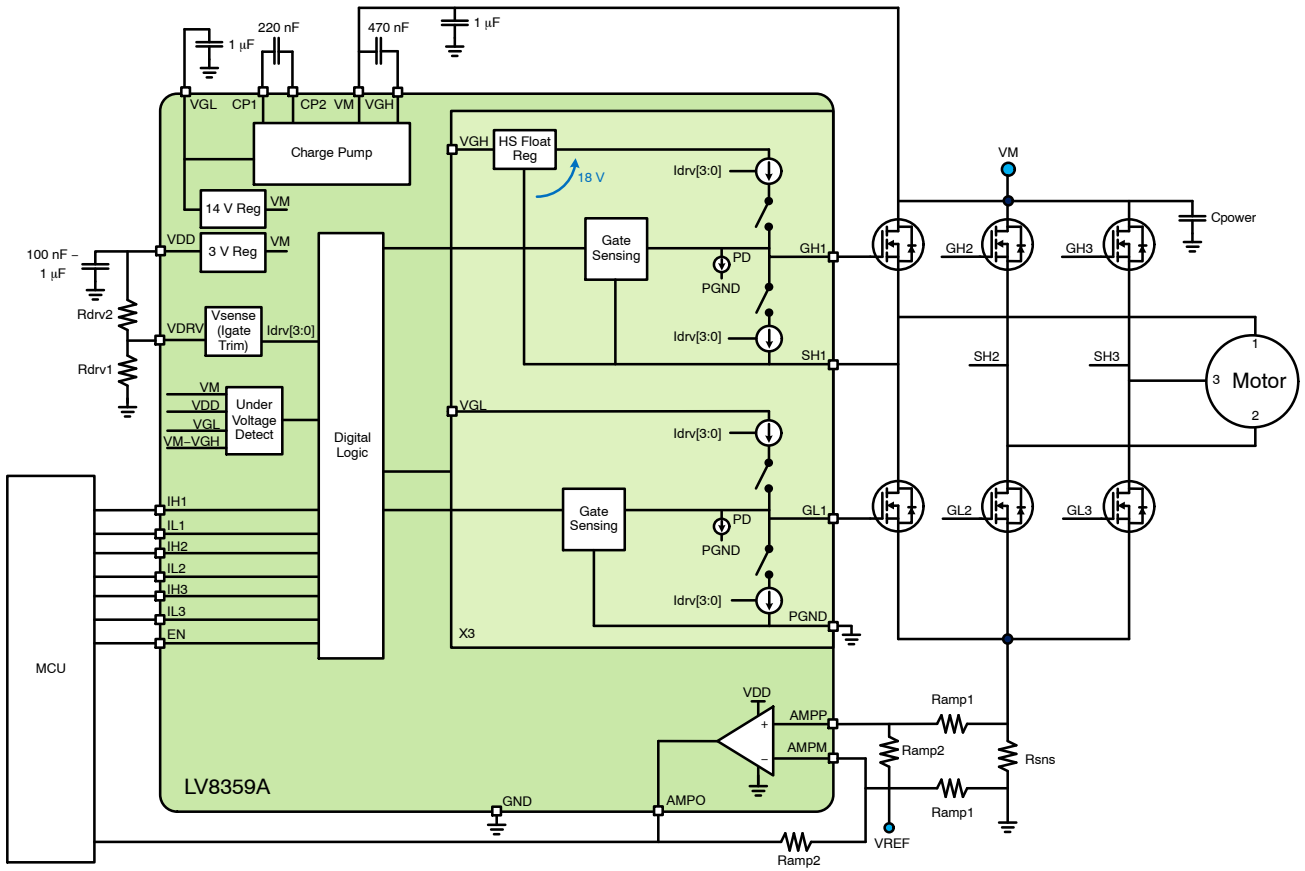
NCD83591

APPLICATION CIRCUIT

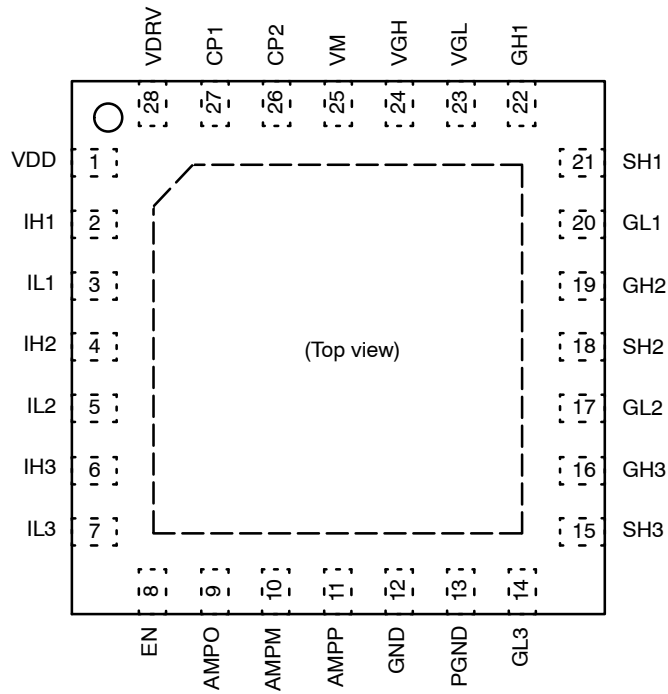**Figure 1. Typical Application Diagram**

NCD83591

PIN ASSIGNMENT

Figure 2. NCD83591 Pinout

PIN ASSIGNMENTS & PIN DESCRIPTION

Pin #	Name	Description
1	VDD	Internal 3 V regulator bypass pin
2	IH1	Active high control for GH1
3	IL1	Active low control for GL1
4	IH2	Active high control for GH2
5	IL2	Active low control for GL2
6	IH3	Active high control for GH3
7	IL3	Active low control for GL3
8	EN	Active high control to enable driver outputs
9	AMPO	Configurable AMP output
10	AMPM	Configurable AMP negative input
11	AMPP	Configurable AMP positive input
12	GND	General ground
13	PGND	Power stage ground
14	GL3	Gate driver output for phase 3 low side external FET
15	SH3	Connection for motor phase 3
16	GH3	Gate driver output for phase 3 high side external FET
17	GL2	Gate driver output for phase 2 low side external FET
18	SH2	Connection for motor phase 2
19	GH2	Gate driver output for phase 2 high side external FET
20	GL1	Gate driver output for phase 1 low side external FET

PIN ASSIGNMENTS & PIN DESCRIPTION (continued)

Pin #	Name	Description
21	SH1	Connection for motor phase 1
22	GH1	Gate driver output for phase 1 high side external FET
23	VGL	Internal 14 V regulator bypass pin
24	VGH	Output of charge pump and storage capacitor pin
25	VM	Motor voltage
26	CP2	Pumping node of charge pump
27	CP1	Switching node of charge pump
28	VDRV	Voltage used to control driver currents

ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to GND unless otherwise noted)

Parameter	Pins	Ratings	Unit
Motor Supply Voltage	VM	−0.3 to 70	V
Gate Low Voltage	VGL	−0.3 to 20	V
Gate High Voltage	VGH	−0.3 to 90	V
Gate High Voltage Relative to VM	VGH – VM	−0.3 to 20	V
High Side Output	GH[1–3]	−12 to VGH + 0.3	V
Voltage between High Side Output and Motor Phase	GH[1–3] – SH[1–3]	−0.3 to 20	V
Motor Phase	SH[1–3]	−12 to VGH + 0.3	V
Low−side Output	GL[1–3] (relative to PGND)	−0.3 to VGL + 0.3	V
Logic Power Supply	VDD	−0.3 to 3.65	V
Digital Inputs	IH[1–3], IL[1–3], EN	−0.3 to 6	V
Analog Inputs/Outputs	AMPM, AMPP, AMPO, VDRV	−0.3 to VDD + 0.3	V
Charge Pump – Switching Node	CP1	−0.3 to VGL + 0.3	V
Charge Pump – Pumping Node	CP2	VM − 1 to VGH + 1	V
Charge Pump – Pumping Node Peak Input Current	CP2	−0.1 to 0.1	A
Storage Temperature		−55 to 150	°C
Junction Temperature		−40 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ESD RATINGS

Parameter	Ratings	Unit
Human Body Model (HBM)	±4000	V
Charged Device Model (CDM)	±1000	V

THERMAL INFORMATION

Parameter	Pins	Ratings	Unit
Theta−JA	Junction Ambient Thermal Resistance	62.5	°C/W
Psi−JB	Junction to Board Characterization Parameter	23.0	°C/W
Psi−JT	Junction to Top Characterization Parameter	4.2	°C/W

ELECTRICAL CHARACTERISTICS

(Valid at a junction temperature range from −40°C to 150°C, for VM supply Voltage 8.0 V ≤ VM ≤ 60 V unless otherwise specified. Typical values at 25°C and VM = 24 V unless specified otherwise.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VM Supply Voltage Range		Normal mode	5	24	60 (Note 1)	V
		Full logic functionality, driver stage off	4	–	70	V
VM Supply Current		EN = H (outputs not toggling), AMP used	–	4.6	5.7	mA
VM Supply Current		EN = H (outputs not toggling), AMP disabled by tieing AMPP = VDD and AMPM = GND	–	4.1	5.2	mA

INTERNAL REGULATOR (VDD)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD Output Voltage			3.2	3.4	3.6	V
VDD External Load Current			–	–	1	mA

GATE VOLTAGES (CP1, VGH, VGL)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VGL Output Voltage		I_{VGL} < 15 mA, VM > 15 V	13	14	15	V
VGL Output Voltage		I_{VGL} < 15 mA, VM < 15 V	VM − 0.43	–	–	V
VGL Current Limit			–	23	30	mA
Charge Pump Frequency			–	125	–	kHz
Charge Pump Output Voltage		VGH − VM, I_{VGH} < 7.5 mA	VGL − 1.2	VGL − 0.75	–	V

GATE DRIVERS (GH[1−3], GL[1−3])

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GL[n], GH[n] Discharge Current to PGND	IDIS	"L" level	–	2 x ICHG	–	mA
GL[n], GH[n] Charge Current	ICHG	"H" level, VDRVcode = 15	–	5	–	mA
		"H" level, VDRVcode = 14	–	10	–	mA
		"H" level, VDRVcode = 13	–	15	–	mA
		"H" level, VDRVcode = 12	–	20	–	mA
		"H" level, VDRVcode = 11	–	25	–	mA
		"H" level, VDRVcode = 10	–	30	–	mA
		"H" level, VDRVcode = 9	–	40	–	mA
		"H" level, VDRVcode = 8	–	50	–	mA
		"H" level, VDRVcode = 7	–	60	–	mA
		"H" level, VDRVcode = 6	–	75	–	mA
		"H" level, VDRVcode = 5	–	100	–	mA
		"H" level, VDRVcode = 4	–	125	–	mA
		"H" level, VDRVcode = 3	–	150	–	mA
		"H" level, VDRVcode = 2	–	175	–	mA
		"H" level, VDRVcode = 1	–	200	–	mA
		"H" level, VDRVcode = 0	–	250	–	mA
Gate Sense Low Threshold	VGSL	GL[1−3], GH[1−3] − SH[1−3]	–	1	–	V
		Hysteresis	–	1	–	V
Cross Conduction Protection Time	t_{xcp}	See Figure 3 No Load on GL[1−3] or GH[1−3]	–	200	–	ns
Input to Output Propagation Delay	t_{prop}	See Figure 3 No Load on GL[1−3] or GH[1−3]	–	–	100	ns

ELECTRICAL CHARACTERISTICS (continued)
(Valid at a junction temperature range from −40°C to 150°C, for VM supply Voltage 8.0 V ≤ VM ≤ 60 V unless otherwise specified. Typical values at 25°C and VM = 24 V unless specified otherwise.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVERS (GH[1−3], GL[1−3])						
Pull−down Current (GH*, GL*)	IPD	VM = 5 V VDD = 0 V GH* = GL* = 2 V Applied per Table 1	500	900	1300	μA
CONFIGURABLE AMP (AMPP, AMPM, AMPO)						
AMPP, AMPM Input Current	AMPP_CUR	INPUT = 0~VDD	−1	–	1	μA
	AMPM_CUR	INPUT = 0~VDD	−1	–	1	μA
AMPO Full Scale Range_1	FS1	RL = 10 kΩ	0.1	–	VDD − 0.15	V
UGBW_1		RL = 10 kΩ to GND, CL = 60 pF At FS1	10	–	–	MHz
Open Loop Gain_1		At FS1	90	–	–	dB
AMPO Full Scale Range_2	FS2	RL = 10 kΩ	0.05	–	VDD − 0.1	V
UGBW_2		RL = 10 kΩ to GND, CL = 60 pF At FS2	8	–	–	MHz
Open Loop Gain_2		At FS2	75	–	–	dB
Slew Rate		Unity Gain, RL = 10 kΩ, CL = 60 pF	10	–	–	V/μs
Input Offset Voltage		RL = 10 kΩ	–	±0.55 (Note 3)	±4.0	mV
Common Mode Input Voltage			0	–	VDD − 1.2	V
DIGITAL INPUTS (IH[1−3], IL[1−3], EN)						
Input Frequency			–	–	30	kHz
High−level Input Voltage		VIH (Note 2)	2.1	–	5.5	V
Low−level Input Voltage		VIL (Note 2)	0	–	0.7	V
Pull−down Current			30	–	100	μA
PROTECTION LEVELS						
VM Under−voltage Lock Out	VM$_{UV}$		4.3	4.5	4.7	V
		Hysteresis	–	0.2	–	V
VGL Under−voltage Lock Out	VGL$_{UV}$		3.9	4.1	4.3	V
		Hysteresis	–	0.2	–	V
VGH Under−voltage Lock Out	VGH$_{UV}$	VGH − VM	3.0	3.2	3.45	V
		Hysteresis	–	0.2	–	V
Under−voltage Lock Out De−glitch Filter	UVFILT	VM$_{UV}$, VGL$_{UV}$, VGH$_{UV}$	–	200	–	μs
VDD POR Lock Out	VDD$_{UV}$		1.55	2.26	2.75	V
		Hysteresis	–	0.15	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. Power dissipation and temp must be accounted for when connecting to voltages > 12 V.
2. Digital inputs are 5 V tolerant.
3. Typical value is a 1 sigma number.

DETAILED FUNCTIONAL DESCRIPTON

Chip Activation, System States and Shutdown

Table 1 shows the operation modes and associated pin states.

Table 1. OPERATION MODES

State	POR (Note 4)	UV_VM (Note 3)	UV_VGL (Note 2, 3)	UV_VGH (Note 3)	Digital Inputs			Driver Outputs (Note 2)		CP1 (Note 2)
					EN	IH*	IL* (Note 1)	GH*	GL*	
POR	H	X	X	X	X	X	X	L–PD	L–PD	L
UV	L	H	X	X	X	X	X	L–PD	L–PD	L
UV	L	X	H	X	X	X	X	L–PD	L–PD	L
Charge	L	L	L	H	X	X	X	L–PD	L–PD	Active
Disable	L	L	L	L	L	X	X	L–PD	L–PD	Active
Drive	L	L	L	L	H	L	L	L	H	Active
Freewheel	L	L	L	L	H	L	H	L	L	Active
Freewheel	L	L	L	L	H	H	L	L	L	Active
Drive	L	L	L	L	H	H	H	H	L	Active

1. IL* inputs are active low.
2. Active means outputs are following the behavior of normal operation. L–PD means that pull down currents (IPD) may be active if 3 V core supply is not sufficient to drive L.
3. H = Under Voltage condition (supply voltage is less than detection levels & filter timer has expired).
4. H = Reset state (VDD voltage is less than detection level).

System Power Supplies (VM, VDD, VGL, VGH)

Internal Core Regulator (VDD)

The internal regulator is supplied by VM and regulates to 3.4 V at VDD. VDD needs to be bypassed to GND for stability. It is not intended for any external loads (other than Rdrv1/Rdrv2), but can support a load up to 1 mA, if necessary.

Gate Voltage Regulator (VGL)

The gate voltage regulator is supplied by VM and regulates to 14 V at VGL.

VGL provides the drive voltage for the low–side drivers GL[1–3] directly and for the high side drivers GH[1–3] through the charge pump circuitry. The output is current limited. The output at VGL must be bypassed with a capacitor to GND which should be at least 10 times the maximum gate capacitance of the power FETs.

Charge Pump (VGH)

An on–chip charge pump provides the gate voltage for the high–side drivers.

Motor Control Inputs (IL[1–3], IH[1–3], EN)

Once the NCD83591 is in Drive or Freewheel mode, a microcontroller can facilitate motor control via the inputs IL[1–3], IH[1–3] and EN. All pins are 5 V/3.3 V compatible. All pins have pull–down currents, so when left floating will be pulled low and cause the outputs to follow the appropriate row in Table 1.

Motor Control (IL[1–3] IH[1–3]) Drive 3 Mode

Drive 3 mode can be achieved by shorting the corresponding IL and IH pins and driving the pin combination with a single microcontroller output.

Gate Drive (GH[1–3], GL[1–3], SH[1–3])

The gate drive circuit of the NCD83591 includes 3 half–bridge drivers which control six external N–Channel FETs. The high side gate drivers GH[1–3] switch their gate connection either to VGH or the respective phase connection SH[1–3]. The low–side gate drivers GL[1–3] are switched from VGL to PGND.

Gate Drive Source/Sink Current Selection

The gate drive currents are programmable to 16 different values as defined in the Electrical Characteristics Table. The VDRVcode is achieved by configuring Rdrv1 and Rdrv2 with standard 5% resistors as described in the Application Diagram with the values that match the desired gate drive currents from Table 2.

Table 2. VDRVcode DESCRIPTION

VDRVcode	Rdrv1	Rdrv2	ICHG	IDIS
15	82k	12k	5	10
14	68k	15k	10	20
13	51k	16k	15	30
12	47k	20k	20	40
11	33k	18k	25	50
10	47k	33k	30	60
9	27k	24k	40	80
8	24k	27k	50	100
7	36k	51k	60	120
6	20k	36k	75	150
5	24k	56k	100	200
4	18k	56k	125	250
3	13k	56k	150	300
2	12k	82k	175	350
1	6.8k	91k	200	400
0	0	Open	250	500

Selected Isrc currents will typically be between 1 mA/nC and 2 mA/nC of FET total gate charge (Qg) to achieve a power stage switching net (SH[1−3]) transition times of about 50 ns. General procedure to selecting a drive current is to start low and increase until ringing on the gate nets or switching nets becomes noticeable, but is still acceptable.

Gate Sensing and Cross Conduction Protection

The gate sensing and cross conduction protection features of the NCD83591 eliminate the need for any minimum dead time control by the gate driver, or even any dead times programmed into the MCU. Corresponding IH[n] and IL[n] pins can be pulsed at the same time and can even be shorted together for motor control methods that do not require tri−stating the power stage (drive 3 mode).

The cross conduction protection feature requires one side of a given phase to be proven to be in an "off" state before the other side is allowed to be turned on to prevent any cross conduction or shoot−through current in the power stage. The diagram in Figure 3 demonstrates this behavior.

In addition, if a given side is currently in an "off" state and something external pulls it to an "on" state, the part forces the opposite side to an "off" state to again prevent shoot−through currents. Sensing a FET is in an "off" state is done through the gate sensing circuit.

The MCU can still force a controlled dead time if desired. This is considered a Drive 6 configuration where each IL[n] and IH[n] pin is driven independently, and the MCU forces a dead time between when low and high sides are active. However, the cross conduction protection will still take precedence if this MCU programmed dead time becomes too short.

The gate sensing provides yet another feature of the part in which a much stronger sinking driver is activated about 50 ns after a gate is sensed to be low. This results in a low hold−off driver resistance to further prevent self turn−on when the SH[n] net is transitioning fast.
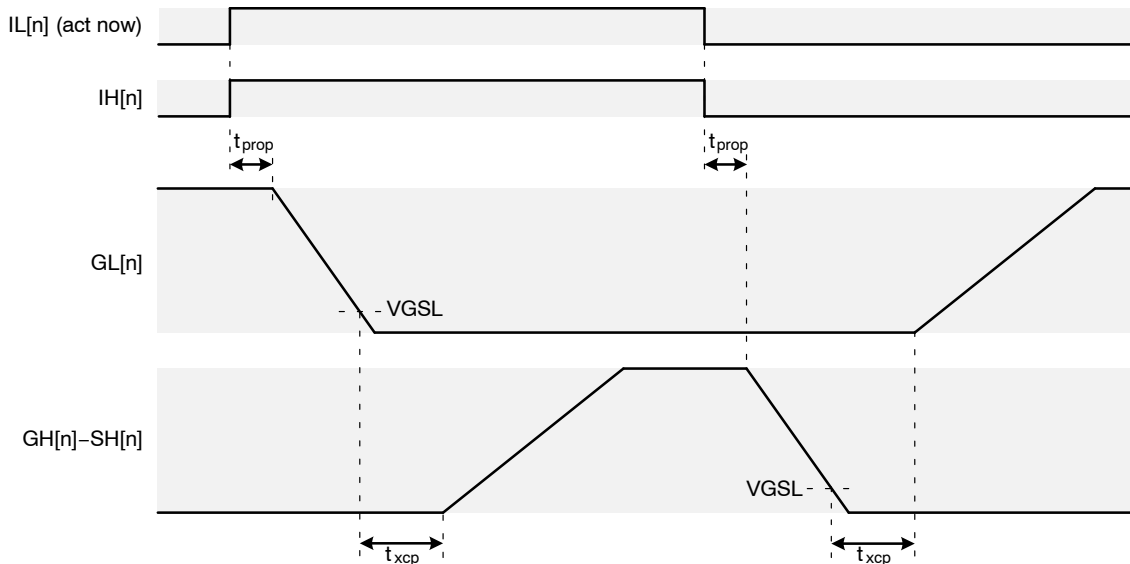
Figure 3. Gate Sensing and Dead Time Diagram

Configurable Amp (AMPP, AMPN, AMPO)

An externally configurable high performance general purpose amplifier is included. It is intended for current sensing as per the Application Diagram, but can be used in any configuration that follows the constraints outlined in the Electrical Characteristics table.

If the configurable amp is not intended to be used, about 0.5 mA of current can be saved by tieing AMPP = VDD and AMPM = GND.

NCD83591

PACKAGE DIMENSIONS
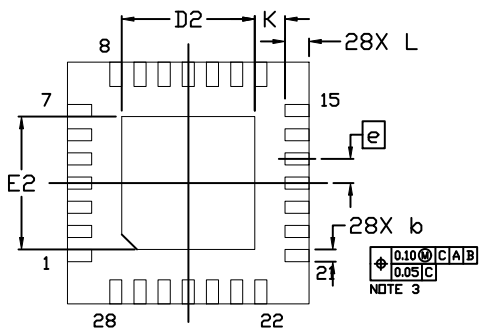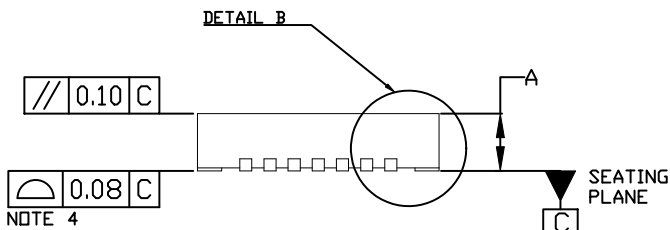
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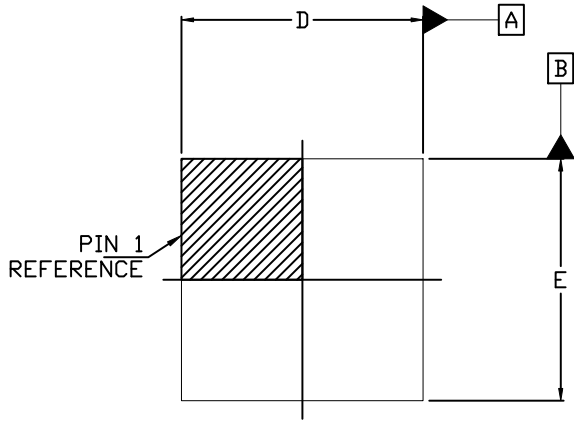
TOP VIEW

DETAIL B

SIDE VIEW

BOTTOM VIEW
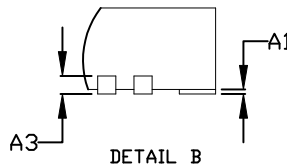
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.10	2.20	2.30
E	3.90	4.00	4.10
E2	2.10	2.20	2.30
e	0.40 BSC		
K	0.50 REF		
L	0.30	0.40	0.50

RECOMMENDED MOUNTING FOOTPRINT*
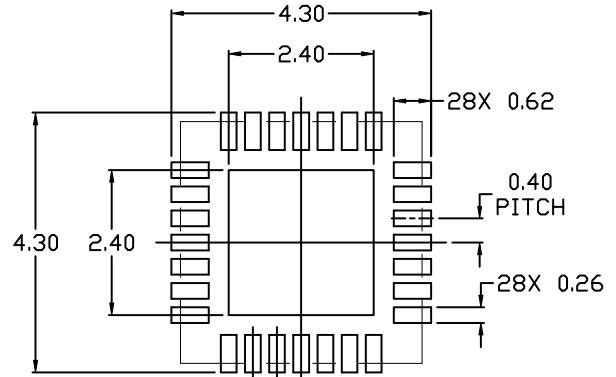
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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