# NCL30002

# Power Factor Corrected Buck LED Driver

The NCL30002 is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. The device operates as a critical conduction mode (CrM) buck controller to regulate LED current at a high power factor for a specific line voltage range. The current limit threshold is tightly trimmed allowing open loop control techniques to reduce parts count while maintaining accurate current regulation and high power factor. CrM operation is particularly suited for LED applications as very high efficiency can be achieved even at low power levels. These are important in LED lighting to comply with regulatory requirements and meet overall system luminous efficacy requirements. In CrM, the switching frequency will vary with line and load. Switching losses are low as recovery losses in the output rectifier are negligible since the current goes to zero prior to reactivating the main MOSFET switch.

The device features a programmable on time limiter, zero current detect sense block, gate driver, trans−conductance error amplifier as well as all PWM control circuitry and protection functions required to implement a CrM switch mode power supply. Moreover, for high efficiency, the device features low startup current enabling fast, low loss charging of the $V_{CC}$ capacitor. The current sense protection threshold has been set at 485 mV to minimize power dissipation in the external sense resistor. To support the environmental operation range of Solid State Lighting, the device is specified across a wide junction temperature range of −40°C to 125°C.

### Features

- Very Low 24 μA Typical Startup Current
- Cycle−by−Cycle Current Protection
- Tightly Trimmed Low Current Sense Threshold of 485 mV ±2%
- Low 2 mA Typical Operating Current
- Source 500 mA / Sink 800 mA Totem Pole Gate Driver
- Wide Operating Temperature Range
- Enable Function and Overvoltage Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

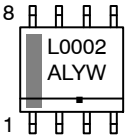
- LED Driver Power Supplies
- LED Based Bulbs
- Commercial and Residential LED Fixtures

**ON Semiconductor®**

**http://onsemi.com**

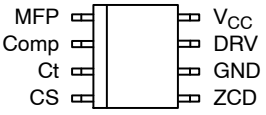

**SOIC−8**
**D SUFFIX**
**CASE 751**

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

**PIN CONNECTION**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCL30002DR2G | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

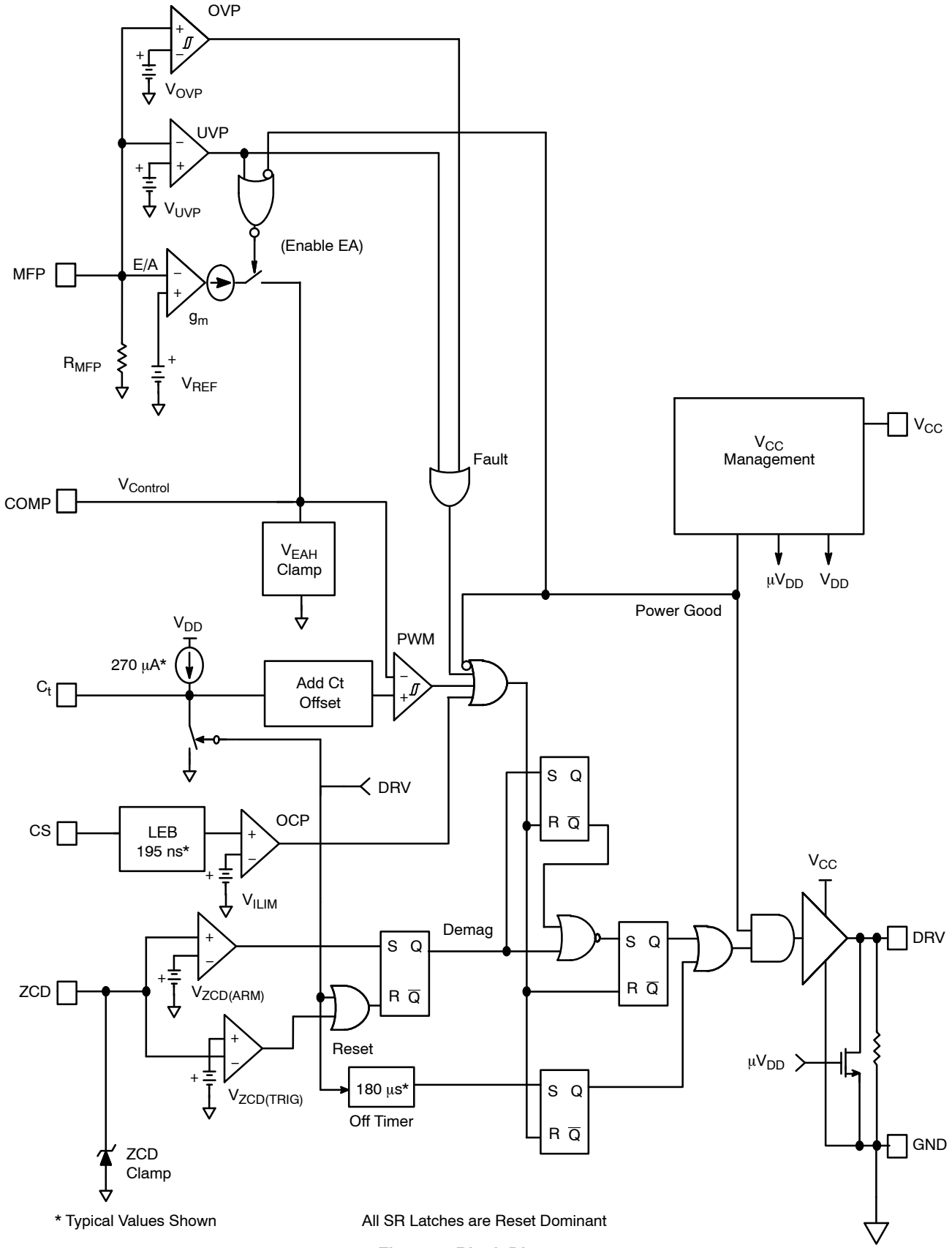



**Figure 1. Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin | Name | Function |
|---|---|---|
| 1 | MFP | The multi−function pin is connected to the internal error amplifier. By pulling this pin below the $V_{uvp}$ threshold, the controller is disabled. In addition, this pin also has an over voltage comparator which will disable the controller in the event of a fault. |
| 2 | COMP | The COMP pin is the output of the internal error amplifier. A compensation network connected between this pin and ground sets the loop bandwidth. |
| 3 | $C_t$ | The $C_t$ pin sources a regulated current to charge an external timing capacitor. The PWM circuit controls the power switch on time by comparing the $C_t$ voltage to an internal voltage derived from $V_{Control}$. The $C_T$ pin discharges the external timing capacitor at the end of the on time cycle. |
| 4 | CS | The CS input threshold is precisely trimmed to accurately sense the instantaneous switch current in the external MOSFET. This signal is conditioned by an internal leading edge blanking circuit. The current limit threshold is tightly trimmed for precise peak current control. |
| 5 | ZCD | The voltage of an auxiliary zero current detection winding is sensed at this pin. When the ZCD control block circuit detects that the winding current has gone to zero, a control signal is sent to the gate drive block to turn on the external MOSFET. |
| 6 | GND | This is the analog ground for the device. All bypassing components should be connected to the GND pin with a short trace length. |
| 7 | DRV | The high current capability of the totem pole gate drive (+0.5/−0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs. The driver stage provides both passive and active pull down circuits that force the output to a voltage less than the turn−on threshold voltage of the power MOSFET when $V_{CC(on)}$ is not reached. |
| 8 | $V_{CC}$ | This pin is the positive supply of the controller. The circuit starts to operate when $V_{CC}$ exceeds $V_{CC(on)}$, nominally 12 V and turns off when $V_{CC}$ goes below $V_{CC(off)}$, typically 9.5 V. After startup, the operating range is 10.2 V up to 20 V. |

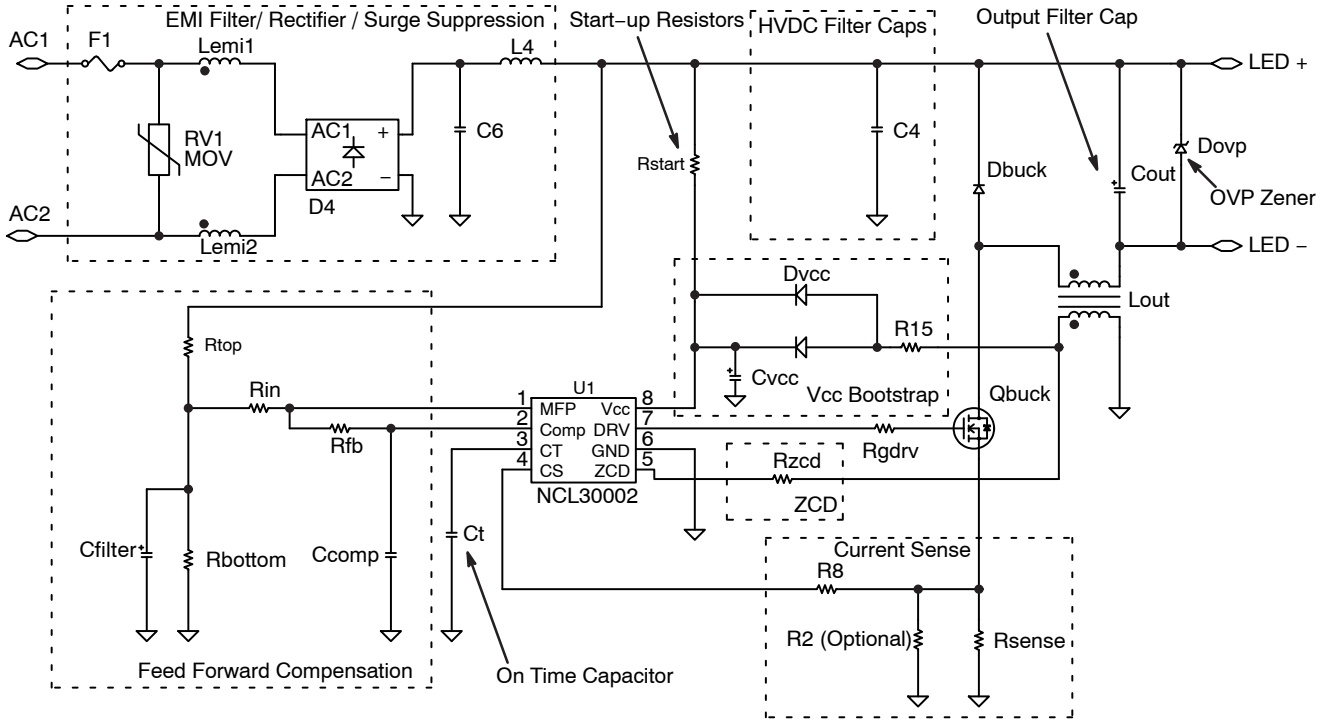



**Figure 2. Simplified PFC Buck Application**

### Overview

Figure 2 illustrates the basic NCL30002 architecture for a non-isolated low power high power factor LED driver. One of the notable features of this architecture is the open loop control. Notice that there is no direct measurement of the LED current. Tight peak current control coupled with line feed-forward compensation to vary the on-time allows for accurate LED drive current. Fortunately in the vast majority of LED bulb and luminaire applications, the LED forward voltage range is well bounded and the line voltage may be limited to one operating range. This is a huge advantage which makes the simplicity of open loop control possible.

Buck switching on the low side eliminates a floating gate drive but references the LED to the HV rail. Buck converters only produce output when the input voltage exceeds the load voltage. Consequently, the input current goes to zero near the zero crossing of the line. The exact phase angle of this event depends on the LED string voltage and the line voltage. Unlike the boost PFC, the buck PFC has increased distortion near the zero crossing. However even with cross over distortion, high power factor and acceptable harmonics can be achieved.

**Table 2. MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| MFP Voltage | $V_{MFP}$ | −0.3 to 10 | V |
| MFP Current | $I_{MFP}$ | ±10 | mA |
| COMP Voltage | $V_{Control}$ | −0.3 to 6.5 | V |
| COMP Current | $I_{Control}$ | −2 to 10 | mA |
| Ct Voltage | $V_{Ct}$ | −0.3 to 6 | V |
| Ct Current | $I_{Ct}$ | ±10 | mA |
| CS Voltage | $V_{CS}$ | −0.3 to 6 | V |
| CS Current | $I_{CS}$ | ±10 | mA |
| ZCD Voltage | $V_{ZCD}$ | −0.3 to 10 | V |
| ZCD Current | $I_{ZCD}$ | ±10 | mA |
| DRV Voltage | $V_{DRV}$ | −0.3 to $V_{CC}$ | V |
| DRV Sink Current | $I_{DRV(sink)}$ | 800 | mA |
| DRV Source Current | $I_{DRV(source)}$ | 500 | mA |
| Supply Voltage | $V_{CC}$ | −0.3 to 20 | V |
| Supply Current | $I_{CC}$ | ±20 | mA |
| Power Dissipation ($T_A$ = 70°C, 2.0 Oz Cu, 55 mm$^2$ Printed Circuit Copper Clad) | $P_D$ | 450 | mW |
| Thermal Resistance Junction−to−Ambient<br>(2.0 Oz Cu, 55 mm$^2$ Printed Circuit Copper Clad)<br>Junction−to−Air, Low conductivity PCB (Note 3)<br>Junction−to−Air, High conductivity PCB (Note 4) | <br>$R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>178<br>168<br>127 | °C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to 125 | °C |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to 150 | °C |
| Lead Temperature (Soldering, 10 s) | $T_L$ | 300 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1− 8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
3. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 80 mm$^2$ of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40 x 40 x 1.5 mm FR4 substrate with a single layer of 650 mm$^2$ of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.

**Table 3. ELECTRICAL CHARACTERISTICS**
$V_{MFP}$ = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{DRV}$ = 1 nF, $V_{CC}$ = 12 V, unless otherwise specified
(For typical values, $T_J$ = 25°C. For min/max values, $T_J$ = −40°C to 125°C, unless otherwise specified)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STARTUP AND SUPPLY CIRCUITS** | | | | | | |
| Startup Voltage Threshold | $V_{CC}$ Increasing | $V_{CC(on)}$ | 11 | 12 | 12.5 | V |
| Minimum Operating Voltage | $V_{CC}$ Decreasing | $V_{CC(off)}$ | 8.8 | 9.5 | 10.2 | V |
| Supply Voltage Hysteresis | | $H_{UVLO}$ | 2.2 | 2.5 | 2.8 | V |
| Startup Current Consumption | 0 V < $V_{CC}$ < $V_{CC(on)}$ − 200 mV | $I_{cc(startup)}$ | – | 24 | 35 | μA |
| No Load Switching Current Consumption | $C_{DRV}$ = open, 70 kHz Switching, $V_{CS}$ = 2 V | $I_{cc1}$ | – | 1.4 | 1.7 | mA |
| Switching Current Consumption | 70 kHz Switching, $V_{CS}$ = 2 V | $I_{cc2}$ | – | 2.1 | 2.6 | mA |
| Fault Condition Current Consumption | No Switching, $V_{MFP}$ = 0 V | $I_{cc(fault)}$ | – | 0.75 | 0.95 | mA |
| **OVERVOLTAGE AND UNDERVOLTAGE PROTECTION** | | | | | | |
| Overvoltage Detect Threshold | $V_{MFP}$ = Increasing | $V_{OVP}$ | 2.5 | 2.67 | 2.85 | V |
| Overvoltage Hysteresis | | $V_{OVP(HYS)}$ | 20 | 60 | 100 | mV |
| Overvoltage Detect Threshold Propagation Delay | $V_{MFP}$ = 1 V to 3 V step, $V_{MFP}$ = $V_{OVP}$ to $V_{DRV}$ = 10% | $t_{OVP}$ | – | 500 | 800 | ns |
| Undervoltage Detect Threshold | $V_{MFP}$ = Decreasing | $V_{UVP}$ | 0.25 | 0.31 | 0.4 | V |
| Undervoltage Detect Threshold Propagation Delay | $V_{MFP}$ = 2 V to 0 V step, $V_{MFP}$ = $V_{UVP}$ to $V_{DRV}$ = 10% | $t_{UVP}$ | 80 | 200 | 320 | ns |
| **ERROR AMPLIFIER** | | | | | | |
| Voltage Reference | $T_J$ = 25°C<br>$T_J$ = −40°C to 125°C | $V_{REF}$ | 2.397<br>2.359 | 2.510<br>2.510 | 2.623<br>2.661 | V |
| Voltage Reference Line Regulation | $V_{CC(on)}$ + 200 mV < $V_{CC}$ < 20 V | $V_{REF(line)}$ | −10 | – | 10 | mV |
| Error Amplifier Current Capability | $V_{MFP}$ = $V_{REF}$ + 0.11 V<br>$V_{MFP}$ = 1.08*$V_{REF}$<br>$V_{MFP}$ = 0.5 V | $I_{EA(sink)}$<br>$I_{EA(sink)OVP}$<br>$I_{EA(source)}$ | 6<br>10<br>−110 | 10<br>20<br>−210 | 20<br>30<br>−250 | μA |
| Transconductance | $V_{MFP}$ = $V_{REF}$ ± 100 mV<br>$T_J$ = 25°C<br>$T_J$ = −40°C to 125°C | gm | <br>90<br>70 | <br>110<br>110 | <br>120<br>135 | μS |
| Feedback Pin Internal Pull−Down Resistor | $V_{MFP}$ = $V_{UVP}$ to $V_{REF}$ | $R_{MFP}$ | 2 | 4.6 | 10 | MΩ |
| Feedback Bias Current | $V_{MFP}$ = 2.5 V | $I_{MFP}$ | 0.25 | 0.54 | 1.25 | μA |
| Control Bias Current | $V_{MFP}$ = 0 V | $I_{Control}$ | −1 | – | 1 | μA |
| Maximum Control Voltage | $I_{Control(pullup)}$ = 10 μA, $V_{MFP}$ = $V_{REF}$ | $V_{EAH}$ | 5 | 5.5 | 6 | V |
| Minimum Control Voltage to Generate Drive Pulses | $V_{Control}$ = Decreasing until $V_{DRV}$ is low, $V_{Ct}$ = 0 V | $Ct_{(offset)}$ | 0.37 | 0.65 | 0.88 | V |
| Control Voltage Range | $V_{EAH}$ − $Ct_{(offset)}$ | $V_{EA(DIFF)}$ | 4.5 | 4.9 | 5.3 | V |

**Table 3. ELECTRICAL CHARACTERISTICS** (Continued)
$V_{MFP}$ = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{DRV}$ = 1 nF, $V_{CC}$ = 12 V, unless otherwise specified
(For typical values, $T_J$ = 25°C. For min/max values, $T_J$ = −40°C to 125°C, unless otherwise specified)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **RAMP CONTROL** | | | | | | |
| Ct Peak Voltage | $V_{COMP}$ = open | $V_{Ct(MAX)}$ | 4.535 | 4.93 | 5.25 | V |
| On Time Capacitor Charge Current | $V_{COMP}$ = open<br>$V_{Ct}$ = 0 V to $V_{Ct(MAX)}$ | $I_{charge}$ | 240 | 270 | 292 | μA |
| Ct Capacitor Discharge Duration | $V_{COMP}$ = open<br>$V_{Ct}$ = $V_{Ct(MAX)}$ −100 mV to 500 mV | $t_{Ct(discharge)}$ | – | 50 | 150 | ns |
| PWM Propagation Delay | dV/dt = 30 V/μs<br>$V_{Ct}$ = $V_{Control}$ − $Ct_{(offset)}$<br>to $V_{DRV}$ = 10% | $t_{PWM}$ | – | 130 | 220 | ns |
| **ZERO CURRENT DETECTION** | | | | | | |
| ZCD Arming Threshold | $V_{ZCD}$ = Increasing | $V_{ZCD(ARM)}$ | 1.25 | 1.4 | 1.55 | V |
| ZCD Triggering Threshold | $V_{ZCD}$ = Decreasing | $V_{ZCD(TRIG)}$ | 0.6 | 0.7 | 0.83 | V |
| ZCD Hysteresis | | $V_{ZCD(HYS)}$ | 500 | 700 | 900 | mV |
| ZCD Bias Current | $V_{ZCD}$ = 5 V | $I_{ZCD}$ | − 2 | – | + 2 | μA |
| Positive Clamp Voltage | $I_{ZCD}$ = 3 mA | $V_{CL(POS)}$ | 9.8 | 10 | 12 | V |
| Negative Clamp Voltage | $I_{ZCD}$ = −2 mA | $V_{CL(NEG)}$ | −0.9 | −0.7 | −0.5 | V |
| ZCD Propagation Delay | $V_{ZCD}$ = 2 V to 0 V ramp,<br>dV/dt = 20 V/μs<br>$V_{ZCD}$ = $V_{ZCD(TRIG)}$ to $V_{DRV}$ = 90% | $t_{ZCD}$ | – | 100 | 170 | ns |
| Minimum ZCD Pulse Width | | $t_{SYNC}$ | – | 70 | – | ns |
| Maximum Off Time in Absence of ZCD Transition | Falling $V_{DRV}$ = 10% to<br>Rising $V_{DRV}$ = 90% | $t_{start}$ | 75 | 165 | 300 | μs |
| **DRIVE** | | | | | | |
| Drive Resistance | $I_{source}$ = 100 mA<br>$I_{sink}$ = 100 mA | $R_{OH}$<br>$R_{OL}$ | –<br>– | 12<br>6 | 20<br>13 | Ω |
| Rise Time | 10% to 90% | $t_{rise}$ | – | 35 | 80 | ns |
| Fall Time | 90% to 10% | $t_{fall}$ | – | 25 | 70 | ns |
| Drive Low Voltage | $V_{CC}$ = $V_{CC(on)}$−200 mV,<br>$I_{sink}$ = 10 mA | $V_{out(start)}$ | – | – | 0.2 | V |
| **CURRENT SENSE** | | | | | | |
| Current Sense Voltage Threshold | $T_J$ = 25°C<br>$T_J$ = −40°C to 125°C | $V_{ILIM}$ | 0.475<br>0.470 | 0.485<br>0.485 | 0.495<br>0.500 | V |
| Leading Edge Blanking Duration | $V_{CS}$ = 2 V, $V_{DRV}$ = 90% to 10% | $t_{LEB}$ | 100 | 195 | 350 | ns |
| Overcurrent Detection Propagation Delay | dV/dt = 10 V/μs<br>$V_{CS}$ = $V_{ILIM}$ to $V_{DRV}$ = 10% | $t_{CS}$ | 40 | 100 | 170 | ns |
| Current Sense Bias Current | $V_{CS}$ = 2 V | $I_{CS}$ | −1 | – | 1 | μA |

## TYPICAL CHARACTERISTICS

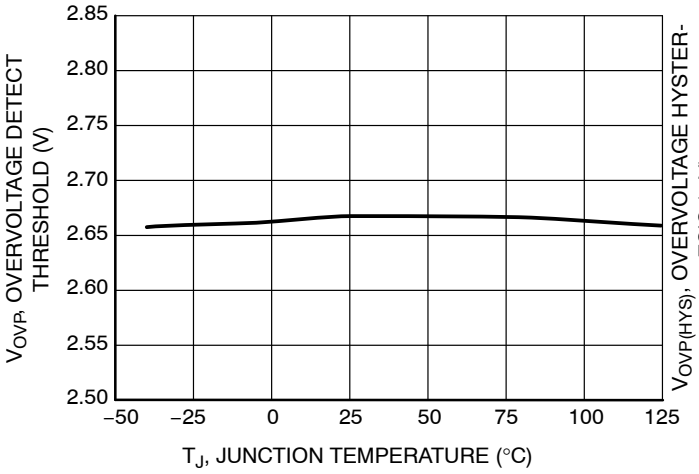



**Figure 3. Overvoltage Detect Threshold vs. Junction Temperature**

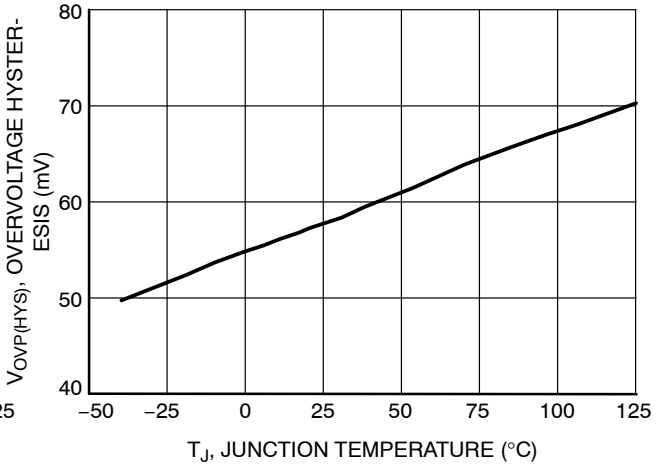



**Figure 4. Overvoltage Hysteresis vs. Junction Temperature**

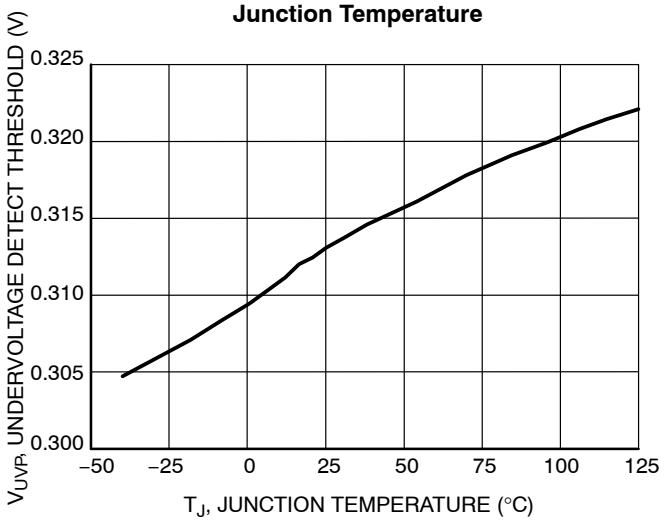



**Figure 5. Undervoltage Detect Threshold vs. Junction Temperature**

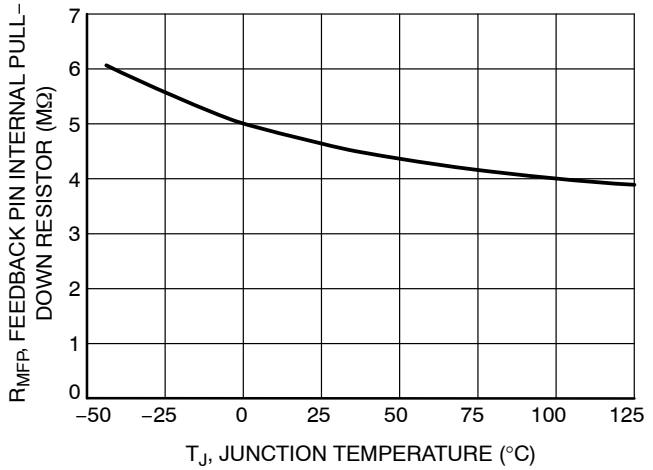



**Figure 6. MFP Pin Internal Pull−Down Resistor vs. Junction Temperature**

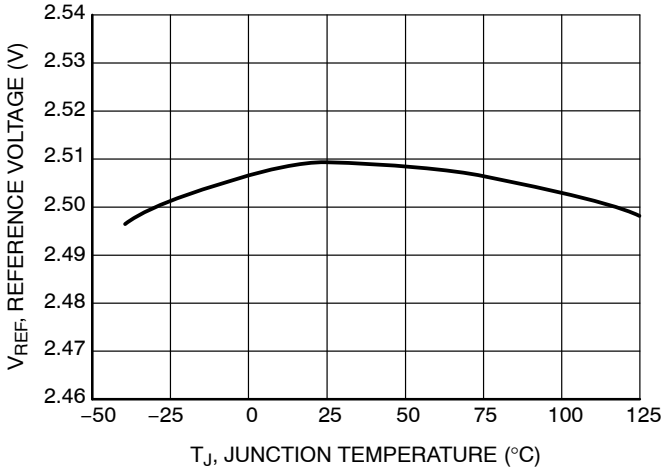



**Figure 7. Reference Voltage vs. Junction Temperature**

## TYPICAL CHARACTERISTICS

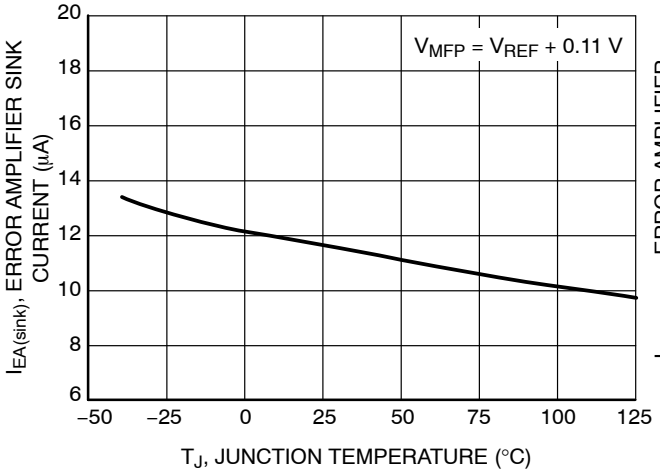



**Figure 8. Error Amplifier Sink Current vs. Junction Temperature**

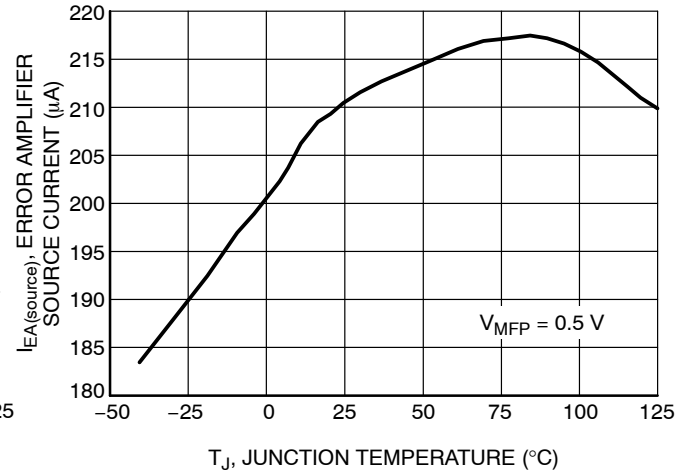



**Figure 9. Error Amplifier Source Current vs. Junction Temperature**

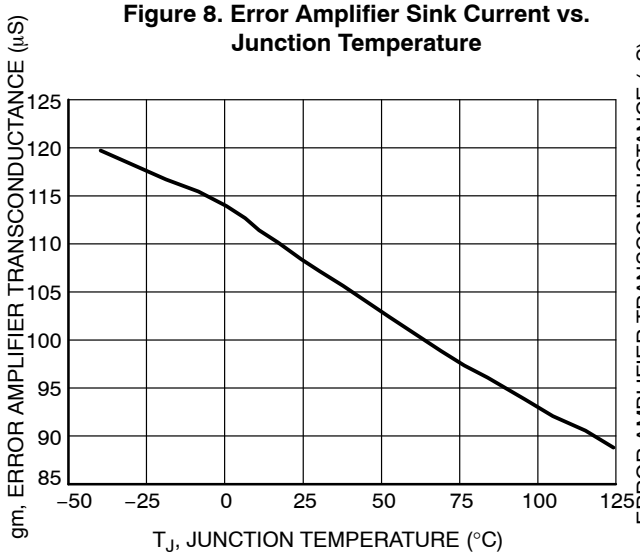



**Figure 10. Error Amplifier Transconductance vs. Junction Temperature**

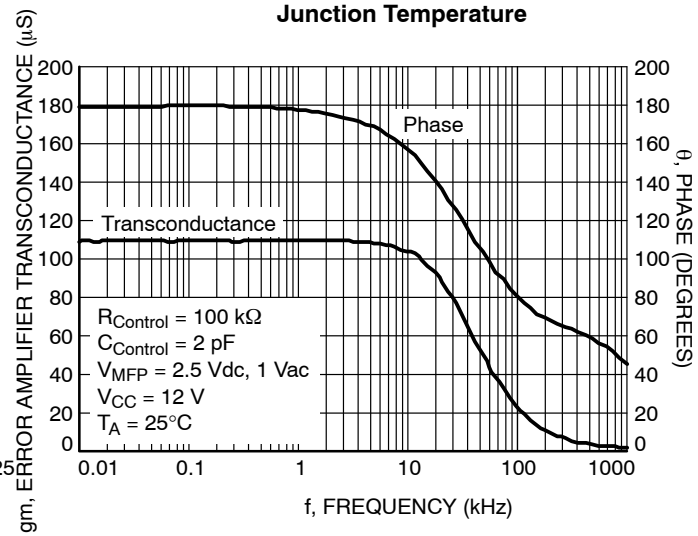



**Figure 11. Error Amplifier Transconductance and Phase vs. Frequency**

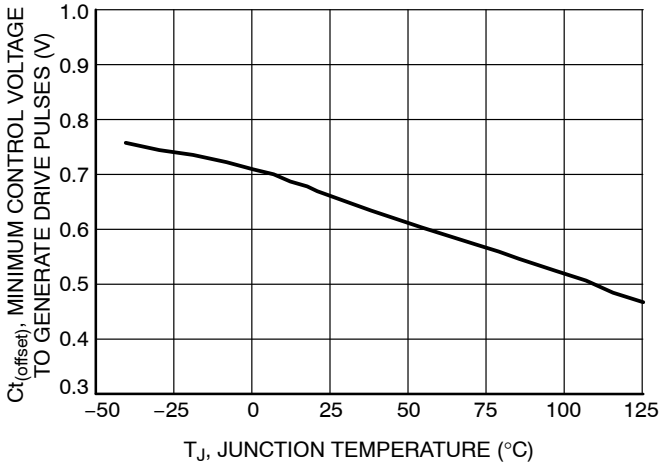



**Figure 12. Minimum Control Voltage to Generate Drive Pulses vs. Junction Temperature**

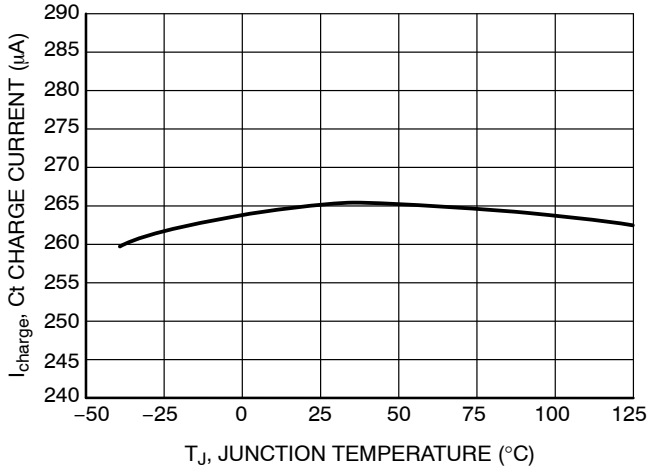



**Figure 13. On Time Capacitor Charge Current vs. Junction Temperature**

## TYPICAL CHARACTERISTICS

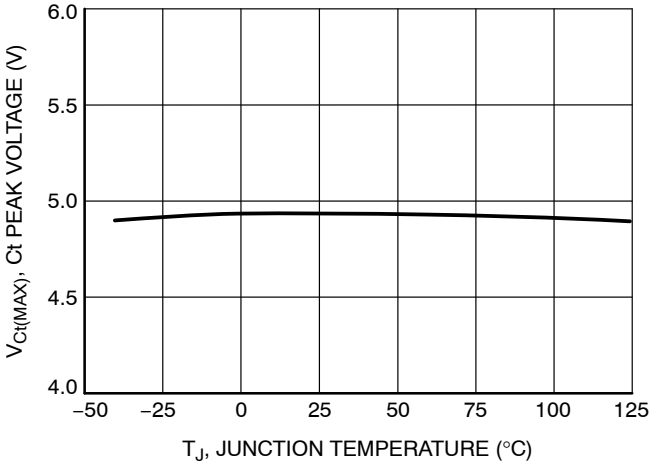



**Figure 14. Ct Peak Voltage vs. Junction Temperature**

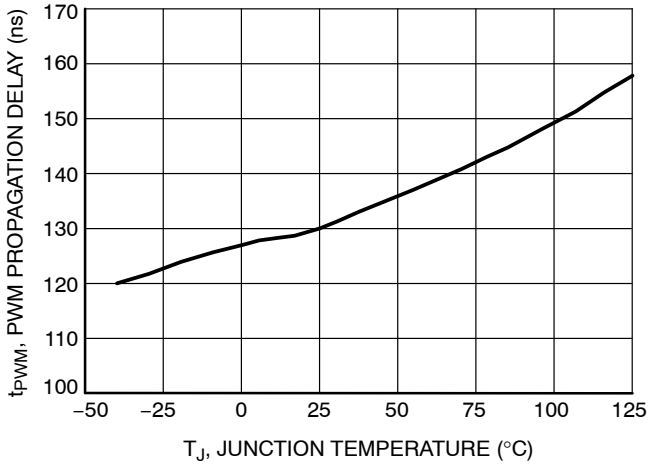



**Figure 15. PWM Propagation Delay vs. Junction Temperature**

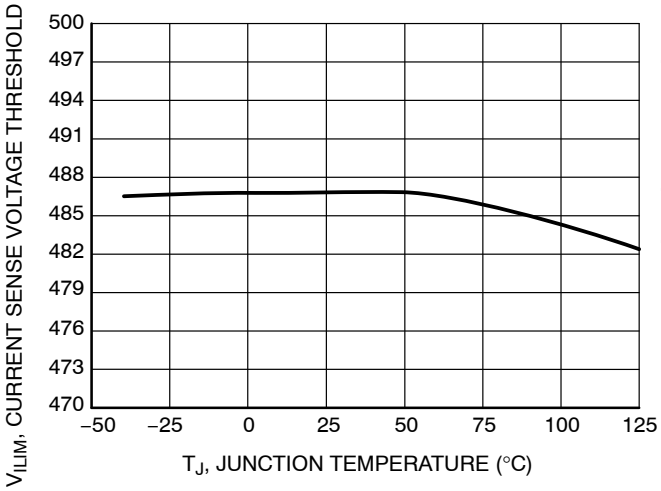



**Figure 16. Current Sense Voltage Threshold vs. Junction Temperature**

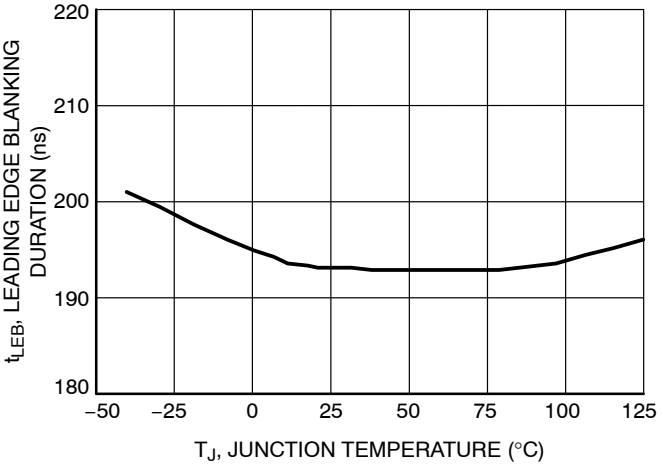



**Figure 17. Leading Edge Blanking Duration vs. Junction Temperature**

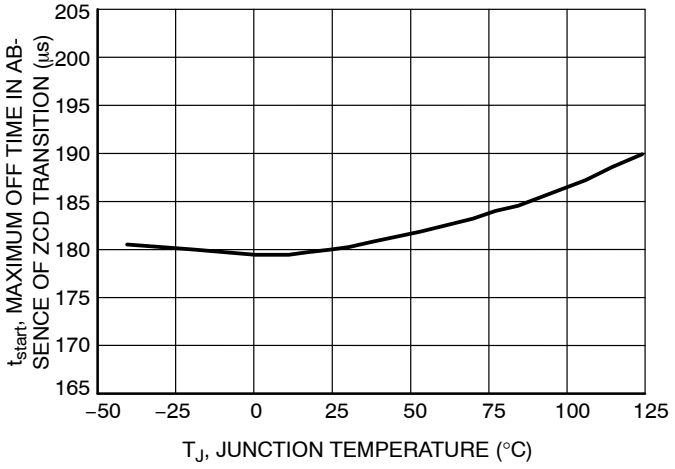



**Figure 18. Maximum Off Time in Absence of ZCD Transition vs. Junction Temperature**

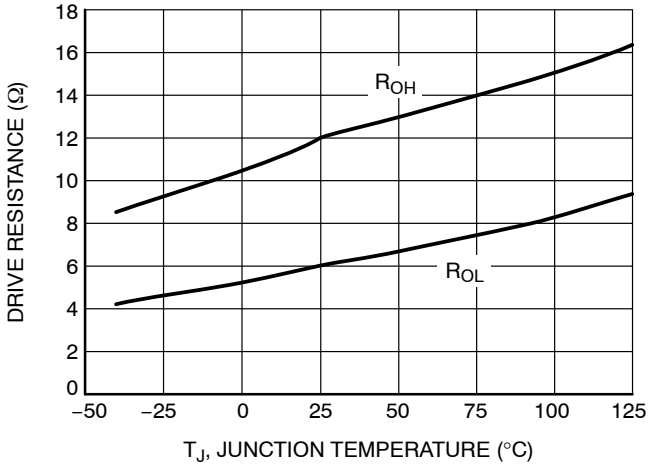



**Figure 19. Drive Resistance vs. Junction Temperature**

## TYPICAL CHARACTERISTICS

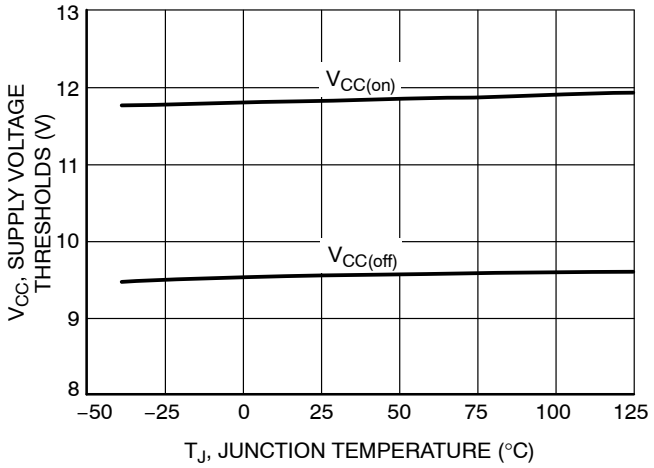



**Figure 20. Supply Voltage Thresholds vs. Junction Temperature**

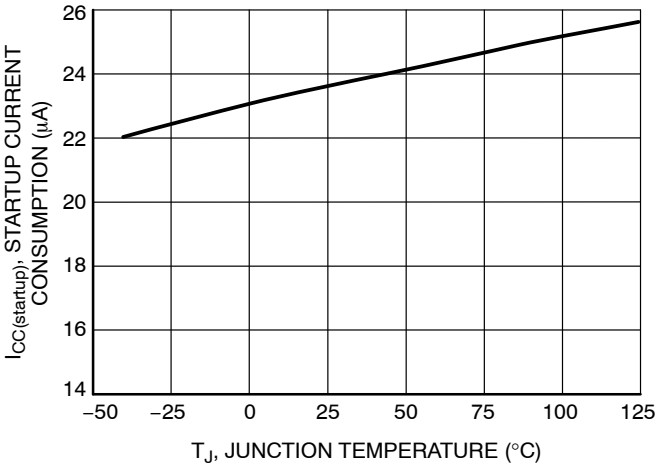



**Figure 21. Startup Current Consumption vs. Junction Temperature**

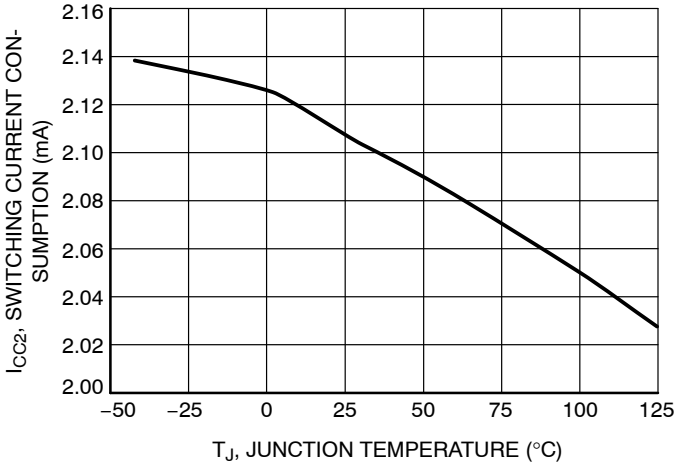



**Figure 22. Switching Current Consumption vs. Junction Temperature**

## THEORY OF OPERATION

High power factor, high efficiency, and small size are key parameters for LED drivers in the incandescent replacement market. The NCL30002 has all the features required to accomplish that is in a compact SOIC-8 package. Power factor is broadly defined as:

$$PF = \frac{P_{in}(avg)}{V_{in}(rms) \times I_{in}(rms)}$$

This differs from the classical definition where there is a phase angle difference between the input voltage and current. However, the underlying concept of optimizing power delivery by minimizing line current is the same. Ideally, current would be directly proportional to the voltage which is the case when the load is a resistor. Offline power converters are active devices which are not purely resistive, capacitive, or inductive often drawing distorted current waveforms from the power lines. This distortion reduces power factor by increasing input RMS current. Preregulators using boost converters are the most common method to correcting the distortion and making the offline power supply appear to be a resistor as far as the power line is concerned. Their performance is excellent achieving power factor greater than 0.99. Regrettably, this two stage approach negatively impacts efficiency and board area. Fortunately, power factors greater than 0.9 are acceptable in the general lighting market and in some applications like US Energystar™ Integral LED bulbs, the minimum acceptable power factor is 0.7. So a certain amount of distortion can be accepted while maintaining high power factor. This buck topology meets the requirements for PF greater than 0.9 and regulate LED current in a single power stage. Unlike the boost converter, the NCL30002 buck controller operates in several different modes over the line cycle.

### Buck Modes

1. "Zero" Input Current ($I_{in}$=0) - Buck converters cannot deliver power when Vin is less than Vout. The "dead time" where no current flows around the zero crossing is dependent on the line voltage and the load voltage.
2. Constant On-Time ($T_{on}$ = constant) - This is the same as the boost converter. Constant $T_{on}$ forces the peak current to be proportional to the input voltage which is key to improved PF.
3. Constant Peak Current ($I_{peak}$ = constant) – The NCL30002 limits the peak inductor and thus the LED current. In this region, the unique nature of the CrM buck means that the average output current is equal to half the peak current. Also the off time is fixed is this mode since the peak current and the output voltage are virtually constant.

In the example below (Figure 23) in spite of the distortion, the power factor is 0.97. The corresponding pre-filtered output current is shown in Figure 24.

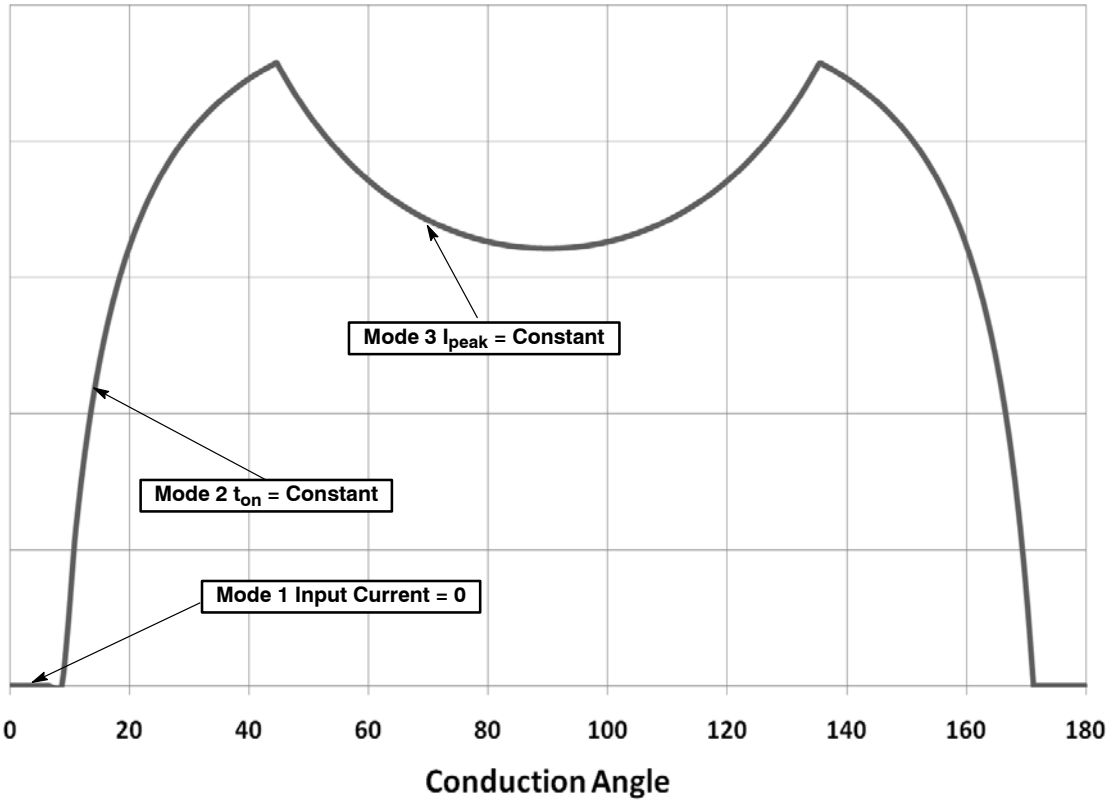



**Figure 23. Theoretical Average Input Current over one half line cycle (conduction angle)**

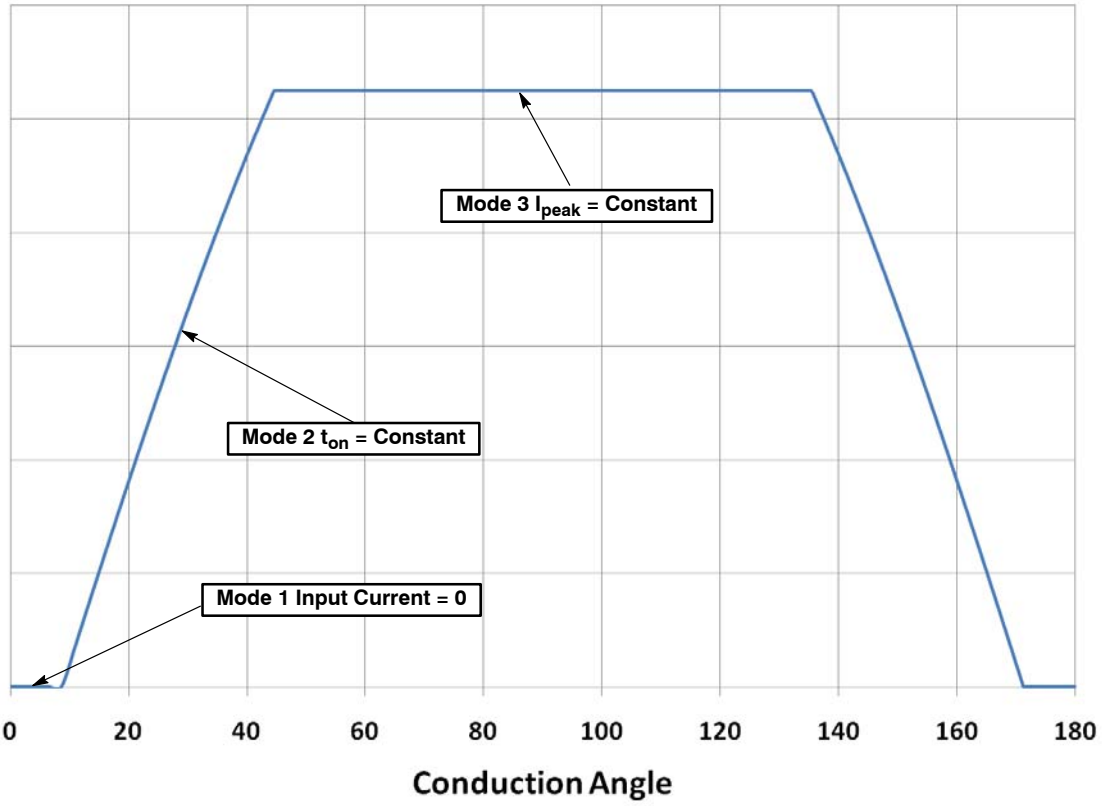



**Figure 24. Theoretical Average Output Current over one half line cycle (conduction angle)**

An output capacitor filters the output current in the LED string. The dynamic LED resistance, line frequency, and the size of the filter capacitance determine the exact LED ripple.

The NCL30002 operates as a CrM controller. The controller draws very low currents while the Vcc filter capacitor charges to the start-up threshold. Since CrM operation is not clocked at a fixed frequency and depends on the state of the power circuit to initiate a new switching cycle, a kick start timer turns on the gate driver to start a new cycle. The kick start timer will do this anytime the driver is off for more than about 180 μsec as long as none of the protection circuits are disabling the gate driver output.

The NCL30002 (refer to the block diagram − Figure 1) is composed of 4 key functional blocks along with protection circuitry to ensure reliable operation of the controller.

- On−Time Control
- Zero Current Detection Control
- MOSFET Gate Driver
- Startup and $V_{CC}$ Management

### On Time Control

The on−time control circuitry (Figure 25) consists of a precision current source which charges up an external capacitor ($C_t$) in a linear ramp. The voltage on $C_t$ (after removing an internal offset) is compared to an external control voltage and the output of the comparator is used to turn off the output driver thus terminating the switching cycle. A signal from the driver is fed back to the on−time control block to discharge the $C_t$ capacitor thus preparing the circuit for the start of the next switching cycle.

The state of $V_{control}$ is determined by the external regulation loop. The range of on−time is determined by the charging slope of the $C_t$ capacitor and is clamped at 4.93 V nominal. The $C_t$ capacitor is sized to ensure that the required on−time is reached at maximum output power and the minimum input line voltage condition.

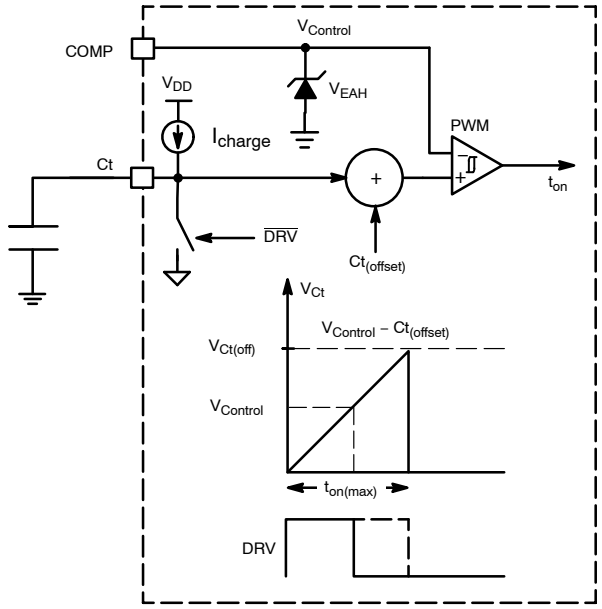



**Figure 25. On Time Control**

### Off Time Sequence

The off time is determined by the peak inductor current, the inductance and the output voltage. In mode 2, the off time is variable because the peak inductor current is not fixed. However in mode 3, the off time is constant since the peak current and the output voltage are both fixed. The auxiliary winding used to provide bias to the NCL30002 is also used to detect when the current has dropped to zero. This is illustrated in Figure 26.

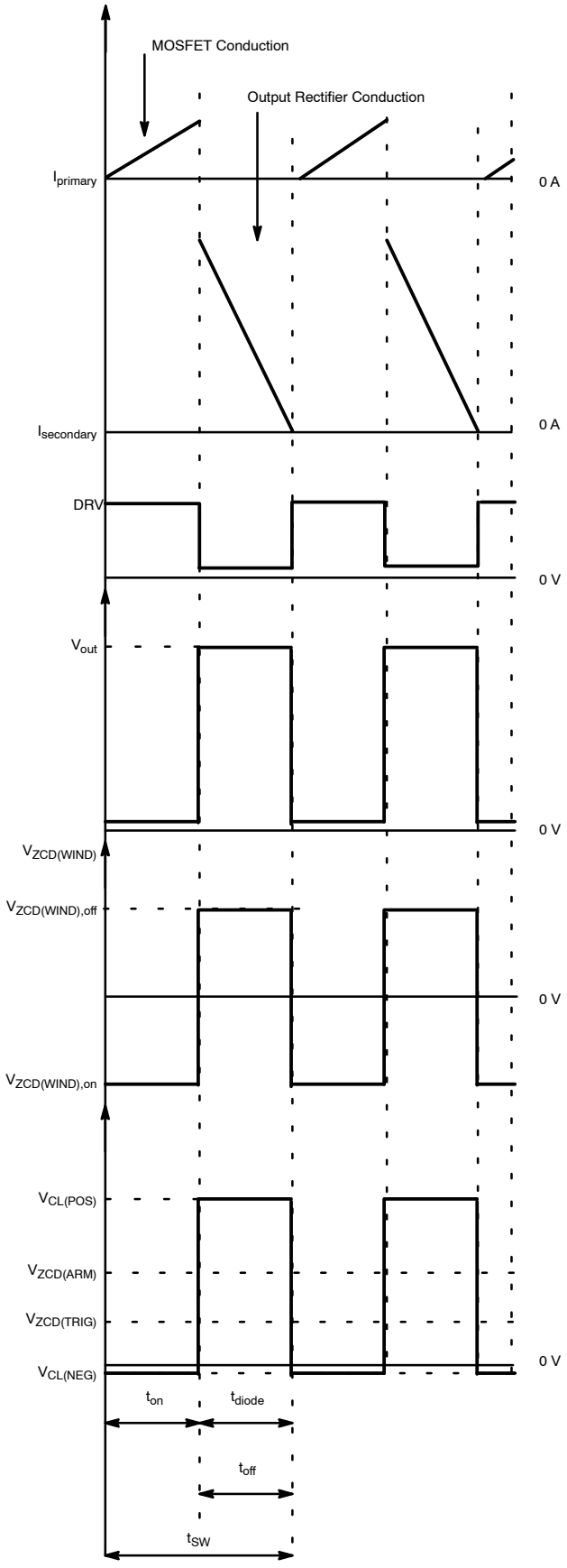



**Figure 26. Ideal CrM Waveforms with ZCD Winding**

### ZCD Detection Block

A dedicated circuit block is necessary to implement the zero current detection**.** The NCL30002 provides a separate input pin to signal the controller to turn the power switch back on just after inductor current reaches zero. When the output winding current reaches zero the winding voltage will reverse. Since all windings of the inductor reflect the same voltage characteristic this voltage reversal appears on the bias winding. Coupling the winding voltage to the ZCD input of the NCL30002 allows the controller to start the next switching cycle at the precise time. To avoid false triggering, the ZCD input has a dual comparator input structure to arm the latch when the ZCD detect voltage rises above 1.4 V (nominal) thus setting the latch. When the voltage on ZCD falls below 0.7 V (nominal) a zero current event is detected and a signal is asserted which initiates the next switching cycle. This is illustrated in Figure 27. The input of the ZCD has an internal circuit which clamps the positive and negative voltage excursions on this pin. The current into or out of the ZCD pin must be limited to ±10 mA with an external resistor.

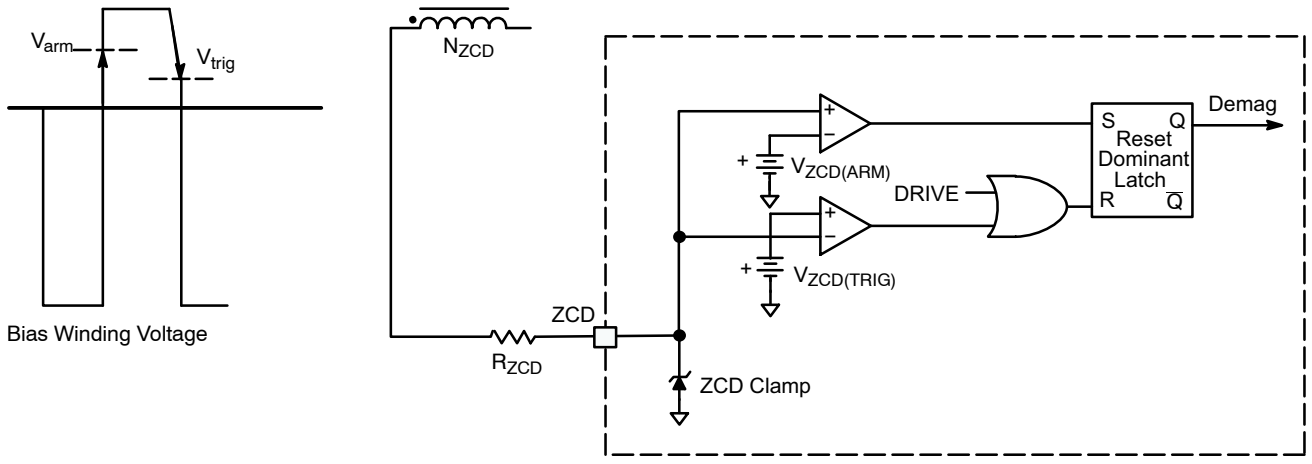



**Figure 27. ZCD Operation**

At startup, there is no energy in the ZCD winding and no voltage signal to activate the ZCD comparators. To enable the controller to start under these conditions, an internal watchdog timer is provided which initiates a switching cycle in the event that the output drive has been off for more than 180 μs (nominal).

The timer is deactivated only under an OVP or UVP fault condition which will be discussed in the next section.

### CS

The dedicated CS pin of the NCL30002 senses the current through the MOSFET switch and the output inductor. If the voltage of the CS pin exceeds $V_{ILIM}$, the internal comparator will detect the event and turn off the MOSFET. The peak switch current is calculated using Equation 1:

$$I_{SW(peak)} = \frac{V_{ILIM}}{R_{sense}} \qquad \text{(eq. 1)}$$

To avoid false detection, the NCL30002 incorporates leading edge blanking circuit (LEB) which masks the CS signal for a nominal time of 190 ns. If required, an optional RC filter can be added between $R_{sense}$ and CS to provide additional filtering. This is illustrated below.

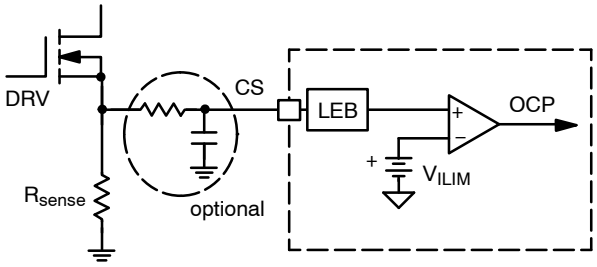



**Figure 28. CS Circuitry with Optional External RC Filter**

### MFP Input

The multi−function pin connects to the inverting terminal of the transconductance amplifier, the undervoltage and overvoltage protection comparators. This allows this pin to perform several functions. To place the device in standby, the MFP pin should be pulled below the $V_{uvp}$ threshold. This is illustrated in Figure 29. Additionally, raising the MFP pin above $V_{ovp}$ will also suspend switching activity but not place the controller in the standby mode. This can be used implement overvoltage monitoring on the bias winding and add an additional layer of fault protection.

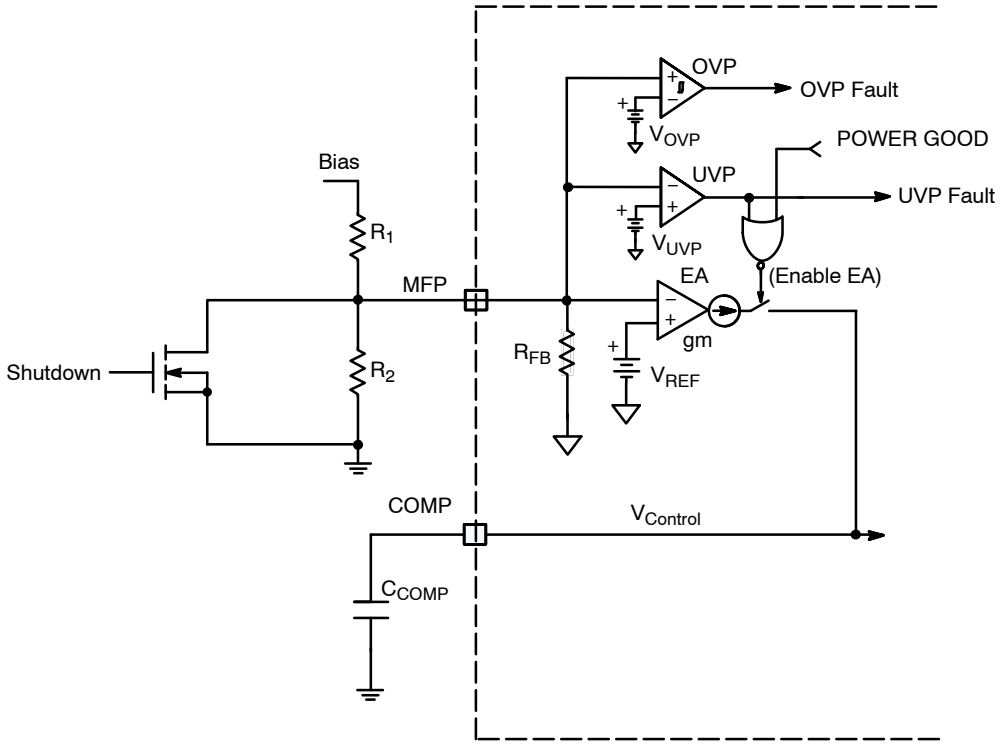



**Figure 29. Multi−Function Pin Operation**

The positive input of the transconductance amplifier is connected to a 2.51 V (nominal) reference. A filtered line feed-forward signal (see Figure 2) is connected to the negative input of the error amplifier and used to control the on-time of controller.

### $V_{CC}$ Management

The NCL30002 incorporates a supervisory circuitry to manage the startup and shutdown of the circuit. By managing the startup and keeping the initial startup current at less than 35 μA, a startup resistor connected between the rectified ac line and $V_{CC}$ charges the $V_{CC}$ capacitor to $V_{CC(on)}$. Turn on of the device occurs when the startup voltage has exceeded 12 V (nominal) when the internal reference and switching logic are enabled. A UVLO comparator with a hysteresis of 2.5 V nominal gives ample time for the device to start switching and allow the bias from the auxiliary winding to supply $V_{CC}$.

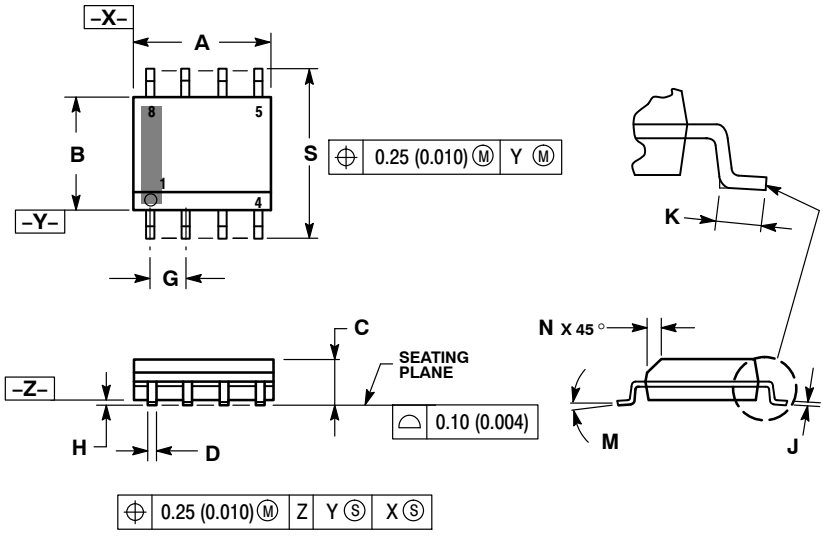
### Design Tool

The NCL30002 implements a unique control method to achieve high power and superior current regulation even though the average current is not directly sensed. There are a number of design tradeoffs that can be made between peak switch current, inductor size, and desired power factor that can impact the current regulation accuracy, efficiency, and physical size. These tradeoffs can be made by adjusting the amount of line feed forward applied, selecting the amount of time where the controller is operating in mode 2 and 3, as well as factoring in the LED forward voltage range. To simplify the component selection process and allow the designer to interactively make these tradeoffs, ON Semiconductor has developed an EXCEL™ based Design Guide which allows step-by-step analysis. This tool is available at onsemi.com along with a supporting application note that illustrates a complete design and provides typical application performance.

SCALE 1:1

**SOIC−8 NB**
CASE 751−07
ISSUE AK

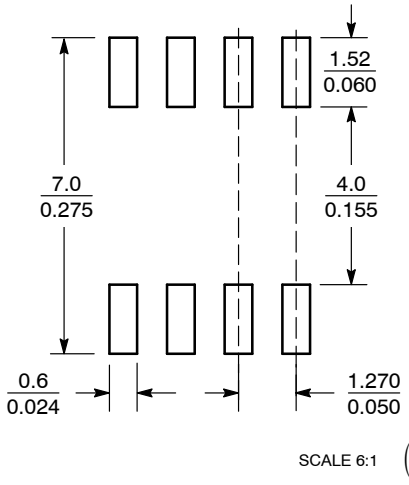
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

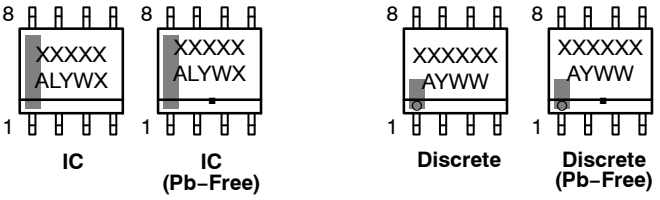
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.


**STYLES ON PAGE 2**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOIC−8 NB** | **PAGE 2 OF 2** |

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** LED Lighting Drivers ***category:***

***Click to view products by*** ON Semiconductor ***manufacturer:***

Other Similar products are found below :

LV5235V-MPB-H MB39C602PNF-G-JNEFE1 MIC2871YMK-T5 AL1676-10BS7-13 AL1676-20AS7-13 AP5726WUG-7 ICL8201 IS31BL3228B-UTLS2-TR IS31BL3506B-TTLS2-TR AL3157F-7 AP5725FDCG-7 AP5726FDCG-7 LV52204MTTBG AP5725WUG-7 STP4CMPQTR NCL30086BDR2G CAT4004BHU2-GT3 LV52207AXA-VH AP1694AS-13 TLE4242EJ AS3688 IS31LT3172-GRLS4-TR TLD2311EL KTD2694EDQ-TR KTZ8864EJAA-TR IS32LT3174-GRLA3-TR MP2488DN-LF-Z NLM0010XTSA1 AL1676-20BS7-13 ZXLD1370QESTTC MPQ7220GF-AEC1-P MPQ7220GR-AEC1-P MPQ4425BGJ-AEC1-P MPQ7220GF-AEC1-Z MPQ7220GR-AEC1-Z MPQ4425BGJ-AEC1-Z NCL30486A2DR2G IS31FL3737B-QFLS4-TR IS31FL3239-QFLS4-TR KTD2058EUAC-TR KTD2037EWE-TR DIO5662ST6 IS31BL3508A-TTLS2-TR KTD2026BEWE-TR MAX20052CATC/V+ MAX25606AUP/V+ BD6586MUV-E2 BD9206EFV-E2 BD9416FS-E2 LYT4227E