# NCN1154MUTGEVB

# NCN1154 DP3T USB 2.0 High Speed Audio Switch Evaluation Board User's Manual

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**EVAL BOARD USER'S MANUAL**

## OVERVIEW

The NCN1154 is a DP3T switch for combined true−ground audio, USB 2.0 high speed data, and UART applications. It allows portable systems to use a single port to pass either USB data or audio signals from an external headset. The switch is capable of passing signals with negative voltages as low as 2 V below ground.

The NCN1154 features shunt resistors on the audio ports. These resistors are switched in when the audio channel is off and provide a safe path to ground for any charge that may build up on the audio lines.

This reduces Pop & Click noise in the audio system. The device has an extended $V_{CC}$ range which can operate off $V_{CC}$ up to 4.2 V while passing true ground audio signals down to −2 V.

The NCN1154 is housed in a space saving, ultra low profile 1.7 x 2.0 x 0.5 mm 12 pin DFN package.

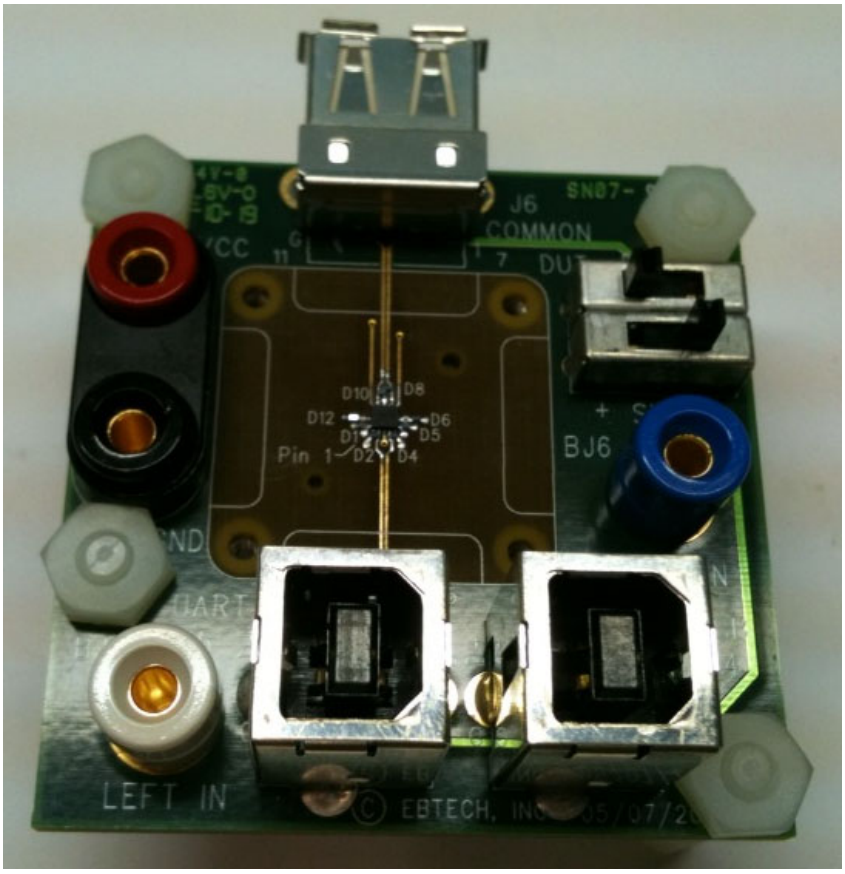


**Figure 1. Board Picture**

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## NCN1154 – BOARD SCHEMATIC

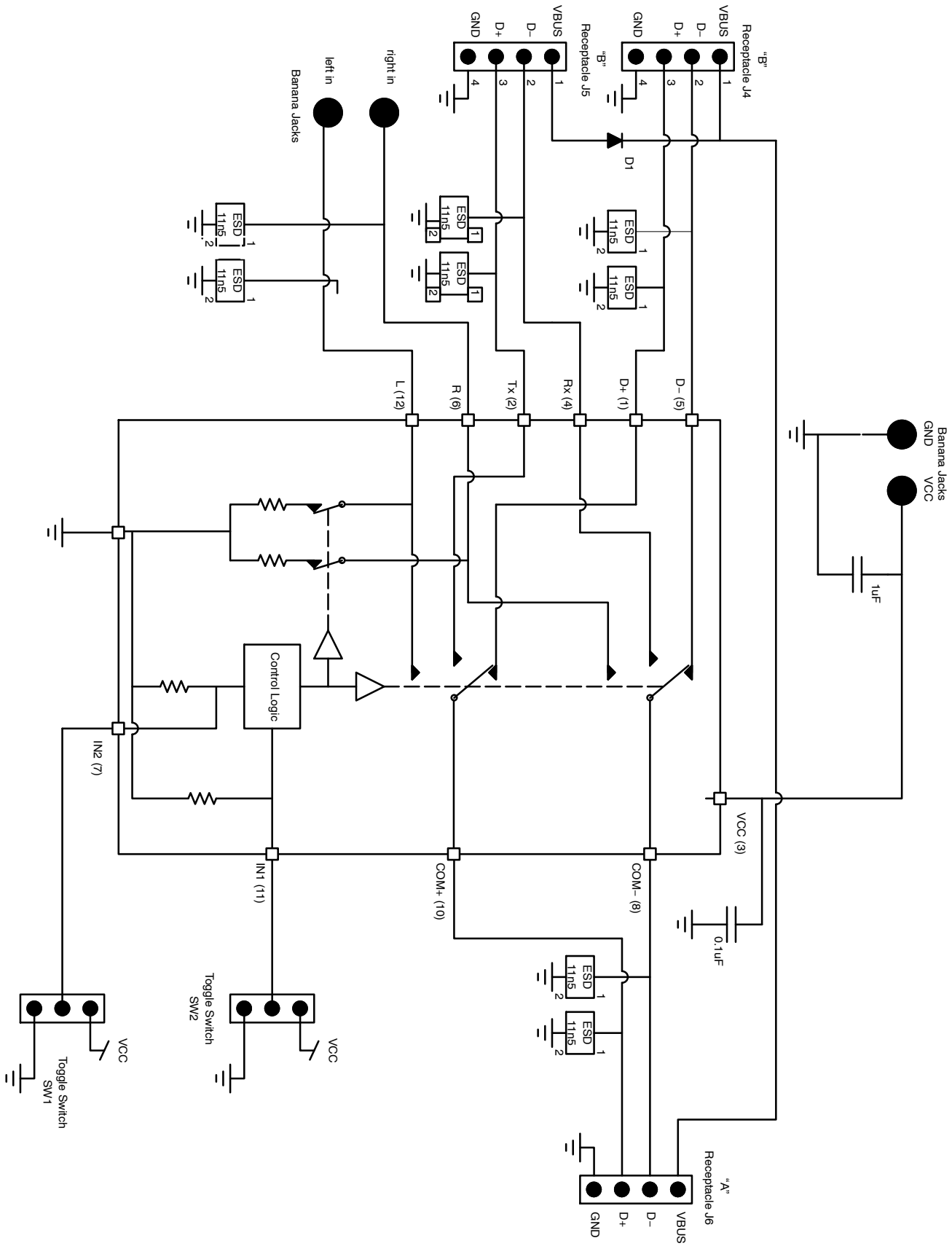


**Figure 2. Board Schematic**

## NCN1154 – BOARD CONNECTIONS

### SUPPLY

| Symbol | Description |
|---|---|
| VCC, GND | This is the positive and the return connection for power supply (Pins 3 and 9). |

### SETUP

| Symbol | Description |
|---|---|
| SW1 | This is the toggle switch for IN2 (Pin 7). |
| SW2 | This is the toggle switch for IN1 (Pin 11). |

### SIGNALS

| Symbol | Description |
|---|---|
| COMMON | This standard USB connector is the common data and audio lines (Pins 8 and 10). |
| USB | This USB connector Male A type is the high speed USB signaling path (Pins 1 and 5). |
| UART | This USB connector Male B type is dedicated for Tx and Rx data lines for UART signals (Pins 2 and 4). |
| LEFT IN | This connector is the left audio signal (Pin 12). |
| RIGHT IN | This connector is the right audio signal (Pin 6). |

## NCN1154 – TEST PROCEDURE

**Equipment needed**

- Power Supply
- Digital Ohm Meter
- Desktop or Laptop with Windows XP or higher
- USB Key
- USB Headset

### BACKGROUND: IN1 & IN2 TRUTH TABLE

| IN1 | IN2 | D+, D– | $R_X$, $T_X$ | L, R | L, R SHUNT |
|---|---|---|---|---|---|
| 0 | 0 | Hi Z | Hi Z | Hi Z | ON |
| 0 | 1 | ON | Hi Z | Hi Z | ON |
| 1 | 0 | Hi Z | Hi Z | ON | OFF |
| 1 | 1 | Hi Z | ON | Hi Z | ON |

**Test**

1. Connect the power supply at 3.6 V from $V_{CC}$ to GND. The supply current should be less than 35 μA.
2. Turn SW1 and SW2 to G (ground) position
   The impedance measured from COM+ to D+, Tx and L is over 10 MΩ.
   The impedance measured from COM− to D−, Rx and R is over 10 MΩ.
   The impedance measured from L & R to GND is closed to 118 Ω.
3. Turn SW1 to + ($V_{CC}$) and keep SW2 to G (ground)
   The impedance measured from COM+ to D+ is closed to 5.5 Ω.
   The impedance measured from COM− to D− is closed to 5.5 Ω.
   The impedance measured from COM+ to Tx and L is over 10 MΩ.
   The impedance measured from COM− to Rx and R is over 10 MΩ.
   The impedance measured from L & R to GND is closed to 118 Ω.
4. Place a USB key connected to COMMON terminal (J6) and connect the USB terminal (J4) to the laptop or desktop.
   The device is being recognized.
   Remove both USB cable and USB key for next measurement.
5. Keep SW1 to + (Vcc) and turn SW2 to + (Vcc)
   The impedance measured from COM+ to Tx is closed to 5.5 Ω.
   The impedance measured from COM− to Rx is closed to 5.5 Ω.
   The impedance measured from COM+ to D+ and L is over 10 MΩ.
   The impedance measured from COM− to D− and R is over 10 MΩ.
   The impedance measured from L & R to GND is closed to 118 Ω.
6. Place a USB key connected to COMMON terminal (J6) and connect the UART terminal (J5) to the laptop or desktop.
   The device is being recognized.
   Remove both USB cable and USB key for next measurement
7. Turn SW1 to G (ground) and keep SW2 to + (Vcc)
   The impedance measured from COM+ to L is closed to 3 Ω.
   The impedance measured from COM− to R is closed to 3 Ω.
   The impedance measured from COM+ to D+ and Tx is over 5 MΩ.
   The impedance measured from COM− to D− and Rx is over 5 MΩ.
   The impedance measured from L & R to GND is over 5 MΩ.

## NCN1154 – COMPONENTS SELECTION

### Input Capacitor

A 0.1 μF X5R ceramic capacitor or larger must bypass Vcc input to the ground. This capacitor should be placed as close as possible to this input.

### ESD Diode

These devices have limited built−in ESD protection, an external bi−directional ESD / IEC diode is recommended on COM+ and COM− pin. The demoboard includes six additional ESD diodes for test purpose which are not required by the application. The ESD11N is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

### NCN1154 – BILL OF MATERIAL

| Designator | Qty | Description | Value | Tolerance | Footprint | Manufacturer | Manufacturer Part Number |
|---|---|---|---|---|---|---|---|
| U1 | 1 | IC, High Speed Switches | NA | NA | UDFN−12 | ON Semiconductor | NCN1154 |
| D1, D2, D4, D5, D6, D8, D10, D12 | 8 | ESD Diode | NA | NA | 0.6 x 0.3 mm | ON Semiconductor | ESD11N5.0ST5G |
| C1, C3 | 1 | Ceramic capacitor | 10 nF | ±20% | 0402 | AVX Corporation | 04023C103KAT2A |
| C2 | 1 | Ceramic capacitor | 1 μF | ±20% | 0603 | Murata | GRM188R61C105 |
| J6 | 1 | USB Connector Male ANG Receptable | NA | NA | A Type | Mill−Max | 896−43−004−90−000000 |
| J4, J5 | 2 | USB Connector Male VERT Receptable | NA | NA | B Type | Molex/Waldom | 67265−2001 |
| BJ6 | 1 | Single Banana | NA | NA | NA | Pomona Electronics | 2142−6 |
| BJ12 | 1 | Single Banana | NA | NA | NA | Pomona Electronics | 2142−9 |
| BJ | 1 | Double Banana | NA | NA | NA | Pomona Electronics | 2143−0 |
| SW1, SW2 | 2 | Switch | NA | NA | NA | ITT CANNON | OS103011MS8QP1 |
| PCB | 1 | 5.0 x 5.0 x 0.25 mm 2 Layers | NA | NA | NA | Any | EBT1745−01 REV: A |

## NCN1154 – PCB LAYOUT GUIDELINES

### Electrical Layout Considerations

Implementing a high speed USD device requires paying attention on USB lines and traces to preserve signal integrity. The demonstration board serves as layout example and can support the design engineers to preserve high speed performances. Electrical layout guidelines are:

- The bypass capacitor must be placed as close as possible to the Vcc input pin for noise immunity.
- The characteristic impedance of each High Speed USB segment must be 45 Ω.
- All corresponding D+ / D− line segment pairs must be the same length.
- The use of vias to route these signals should be avoided.
- The use of turns or bends to route these signal should be avoided.
- The ground plane of the PCB will be used to determine the characteristics impedance of each line.

## NCN1154 – DEMOBOARD PCB LAYOUT

**Board Reference:** EBT1745−01 REV: A

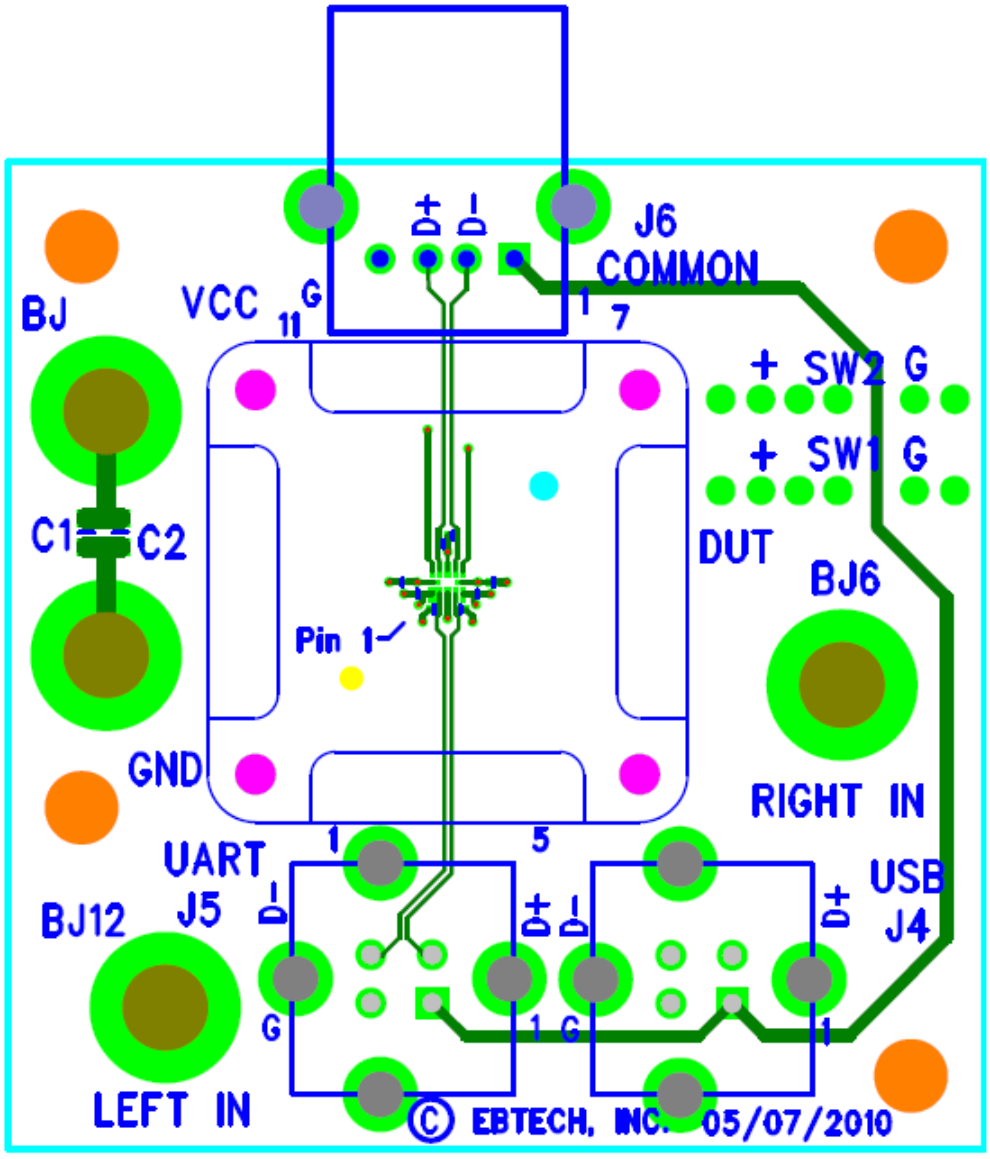


Figure 3. Top Layer Routing

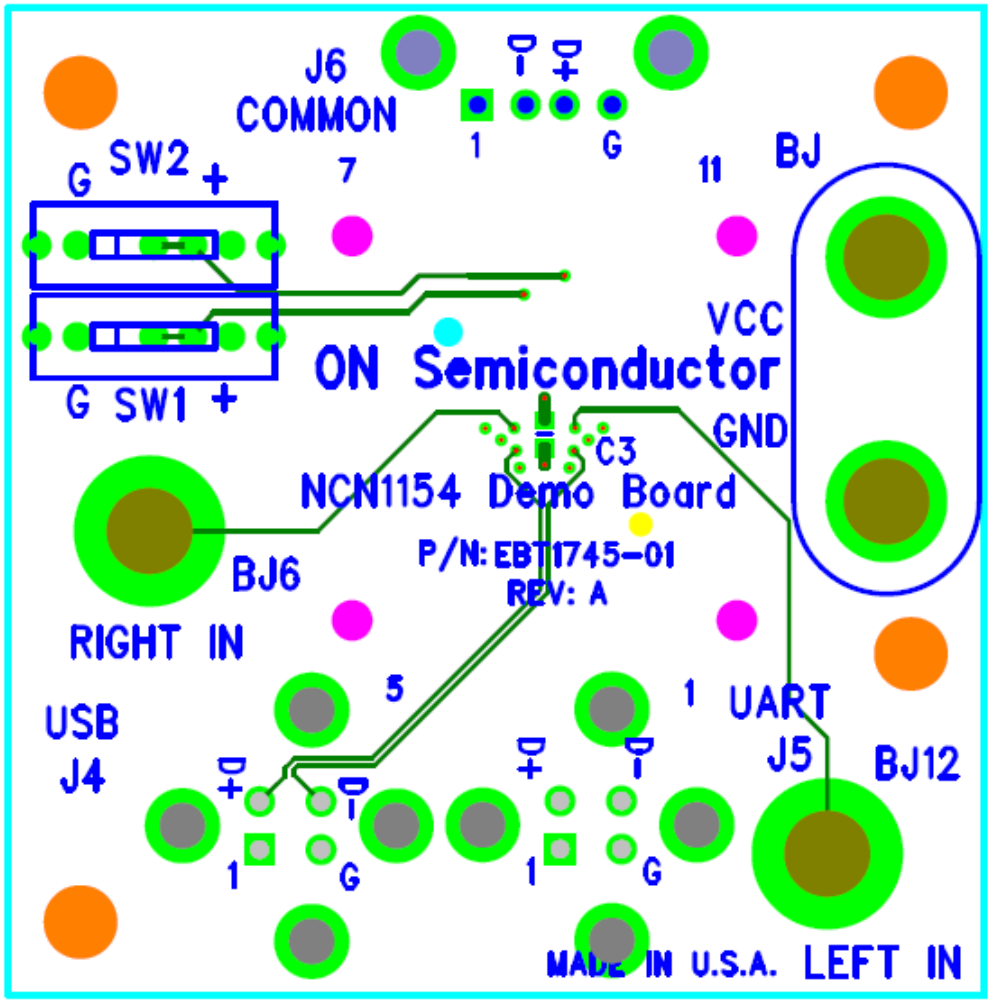


Figure 4. Bottom Layer Routing

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