NCN49597

Power Line Communication Modem

The NCN49597 is a powerful spread frequency shift keying (S−FSK) communication system−on−chip (SoC) designed for communication in hostile environments.

It combines a low power ARM Cortex M0 processor with a high precision analogue front end. Based on 4800 baud S−FSK dual−channel technology, it offers an ideal compromise between speed and robustness.

Pin−compatible with its predecessor, the AMIS−49587, this new generation chip extends the communication frequency range to cover all CENELEC bands for use in applications such as e−metering, home automation and street lighting. The NCN49597 benefits for more than 10 years of field experience in e−metering and delivers innovative features such as a smart synchronization and in−band statistics.

Fully reprogrammable, the modem firmware can be updated in the field. Multiple royalty−free firmware options are available from ON Semiconductor; refer to the separate datasheets for details. The configurable GPIOs allow connecting peripherals such as LCDs or metering ICs.

Features

- Power Line Communication (PLC) Modem for 50 Hz, 60 Hz and DC Mains
- Embedded ARM Cortex M0 Processor
- 10 General Purpose IOs Controllable by Software
- Embedded 32 kB RAM
- Embedded 2 kB ROM Containing Boot Loader
- Hardware Compliant with CENELEC EN 50065−1 and EN 50065−7 Half Duplex S−FSK Channel, Data Rate Selectable:
  300 – 600 – 1200 – 2400 – 4800 baud (@ 50 Hz);
  360 – 720 – 1440 – 2880 – 5760 baud (@ 60 Hz)
- Programmable Carrier Frequencies in CENELEC A, B, C and D Band
- UART for Interfacing with an Application Microcontroller
- Power Supply 3.3 V
- Wide Junction Temperature Range: −40°C to +125°C

Available Firmware Options

- ON−PL110 − Mesh Networking with Collision Avoidance and Error Correction
- Complete Handling of Protocol Layers (physical, MAC, LLC)

Typical Applications

- AMR: Remote Automated Meter Reading
- Building Automation
- Solar Power Control and Monitoring
- Street Light Control and Monitoring
- Transmission of Alerts (fire, gas leak, water leak)

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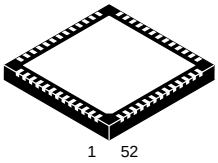
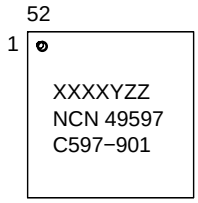


QFN52 8x8, 0.5P
CASE 485M

MARKING DIAGRAM



XXXX = Date Code
Y = Plant Identifier
ZZ = Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

APPLICATION

Application Example

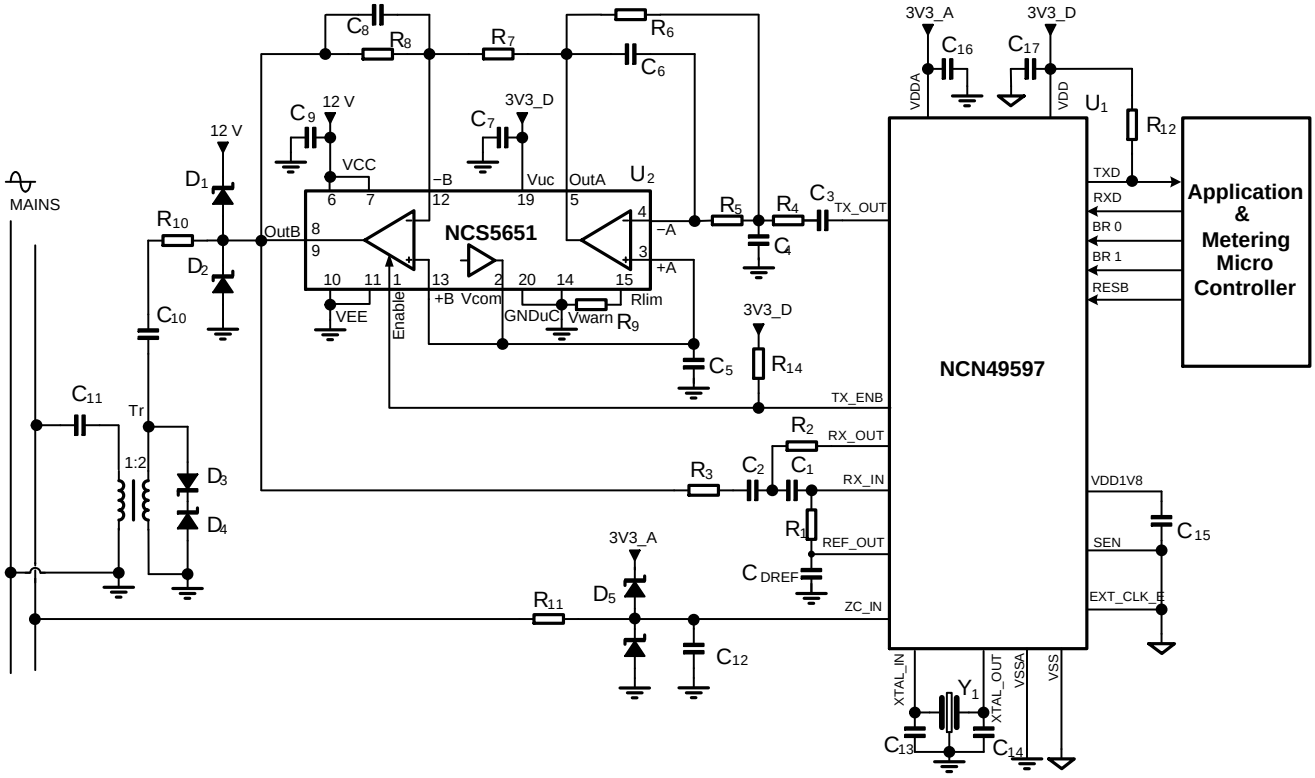


Figure 1. Typical Application for the NCN49597 S−FSK Modem

Figure 1 shows an S−FSK PLC modem built around the NCN49597. The design is a good starting point for a CENELEC. EN 50065−1−compliant system; for further information refer to the referenced design manual.

This design is not galvanically isolated; safety must be considered when interfacing to a microcontroller or a PC.

For synchronization the mains is coupled in via a 1 MΩ resistor; the Schottky diode pair D_5 clamps the voltage within the input range of the zero crossing detector.

In the receive path a 2nd order high pass filter blocks the mains frequency. The corner point − defined by C_1, C_2, R_1 and R_2 − is designed at 10 kHz. In the transmit path a 3th order low pass filter built around the NCS5651 power operational amplifier suppresses the 2nd and 3rd harmonics to be in line with the CENELEC EN50065−1 specification. The filter components are tuned for a space and mark frequency of 63.3 and 74 kHz respectively. The output of the amplifier is coupled through DC blocking capacitor C_{10} to a 2:1 transformer Tr. The high voltage capacitor C_{11} couples the secondary of this transformer to the mains. High−energetic transients from the mains are clamped by the protection diode combination D_3, D_4, together with D_1, D_2.

Table 1. EXTERNAL COMPONENTS LIST AND DESCRIPTION

Component	Function and Remarks	Value	Tolerance	Unit
C_1, C_2	High pass receive filter	1.5	±10%	nF
C_5, C_{DREF}	V_{COM} & V_{REF_OUT} ceramic decoupling	1	−20 +80%	μF
C_7, C_9, C_{16}, C_{17}	Supply decoupling	100	−20 +80%	nF
C_3	TX_OUT signal coupling	470	±20%	nF
C_4	Low pass transmit filter	470	±10%	pF
C_6	Low pass transmit filter	68	±10%	pF
C_8	Low pass transmit filter	3	±10%	pF
C_{10}	Transmission signal coupling cap; 1 A_{RMS} ripple @ 70 kHz	10	±20%	μF
C_{11}	High voltage coupling; 630 VDC	220	±20%	nF
C_{12}	Zero crossing noise suppression	100	±20%	pF
C_{13}, C_{14}	Crystal load capacitor	22	±20%	pF
C_{15}	Internal 1.8 V supply decoupling; ceramic	1	−20 +80%	μF
R_1	High pass receive filter	22	±1%	kΩ
R_2	High pass receive filter	11	±1%	kΩ
R_3	High pass receive filter	10	±1%	kΩ
R_9	Line driver current limitation setting	10	±1%	kΩ
R_4	Low pass transmit filter	3.3	±1%	kΩ
R_5	Low pass transmit filter	10	±1%	kΩ
R_6	Low pass transmit filter	8.2	±1%	kΩ
R_7	Low pass transmit filter	500	±1%	Ω
R_8	Low pass transmit filter	3	±1%	kΩ
R_{10}	Line transients protection; 0.5 W	0.47	±10%	Ω
R_{11}	Zero crossing coupling	1	±10%	MΩ
R_{12}, R_{13}	Pull up	10	±10%	kΩ
D_1, D_2	High−current Schottky clamp diodes	MBRA340		
D_3, D_4	Unidirectional TVS	P6SMB6.8AT3G		
D_5	Dual low−current Schottky clamp diode	BAS70−04		
Y1	Crystal	48 MHz	50 ppm	
Tr	2:1 signal transformer			
U1	PLC modem	NCN49597		
U2	Power operational amplifier	NCS5651		

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
POWER SUPPLY PINS VDD, VDDA, VSS, VSSA				
Absolute max. digital power supply	V_{DD_ABSM}	V_{SS} − 0.3	3.9	V
Absolute max. analog power supply	V_{DDA_ABSM}	V_{SSA} − 0.3	3.9	V
Absolute max. difference between digital and analog power supply	$V_{DD} - V_{DDA\_ABSM}$	−0.1	0.1	V
Absolute max. difference between digital and analog ground	$V_{SS} - V_{SSA\_ABSM}$	−0.1	0.1	V
CLOCK PINS XIN, XOUT				
Absolute maximum input for the clock input pin (Note 1)	V_{XIN_ABSM18}	V_{SS} − 0.2	V_{DD18} + 0.2	V
Absolute maximum voltage at the clock output pin (Note 1)	V_{XOUT_ABSM18}	V_{SS} − 0.2	V_{DD18} + 0.2	V
NON 5 V SAFE PINS: TX_OUT, ALC_IN, RX_IN, RX_OUT, REF_OUT, ZC_IN, TDO, SCK, SDO, SCB				
Absolute maximum input for normal digital inputs and analog inputs	V_{N5VSIN_ABSM}	V_{SS} − 0.3	V_{DD} + 0.3	V
Absolute maximum voltage at any output pin	$V_{N5VSOUT\_ABSM}$	V_{SS} − 0.3	V_{DD} + 0.3	V
Maximum peak input current at the zerocrossing input pin	Imp_{ZC_IN}	−20	20	mA
Maximum average input current at the zerocrossing input pin (1 ms)	$Imavg_{ZC\_IN}$	−2	2	mA
5 V SAFE PINS: TX_ENB, TXD, RXD, BR0, BR1, IO0..IO9, RESB, TDI, TCK, TMS, TRSTB, TEST, SDI				
Absolute maximum input for digital 5 V safe pins configured as input (Note 2)	V_{5VSIN_ABSM}	V_{SS} − 0.3	5.5	V
Absolute maximum voltage at 5 V safe pin configured as output (Note 2)	V_{5VSOUT_ABSM}	V_{SS} − 0.3	V_{DD} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The upper maximum voltage rating on the clock pins XIN and XOUT is specified with respect to the output voltage of the internal core voltage regulator. The tolerance of this voltage regulator must be taken into account. In case an external clock is used, care must be taken not to damage the XIN pin.
2. The direction (input or output) of configurable pins (IO0…IO9) depends on the firmware.

Normal Operating Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in the Electrical Characteristics section and for the reliability specifications.

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1 percent of the useful life.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Power supply voltage range (VDDA and VDD pins)	V_{DD}, V_{DDA}	3.0	3.6	V
Junction Temperature Range	T_J	−40	125	°C
Ambient Temperature Range	T_A	−40	115	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

PIN DESCRIPTION − QFN Package

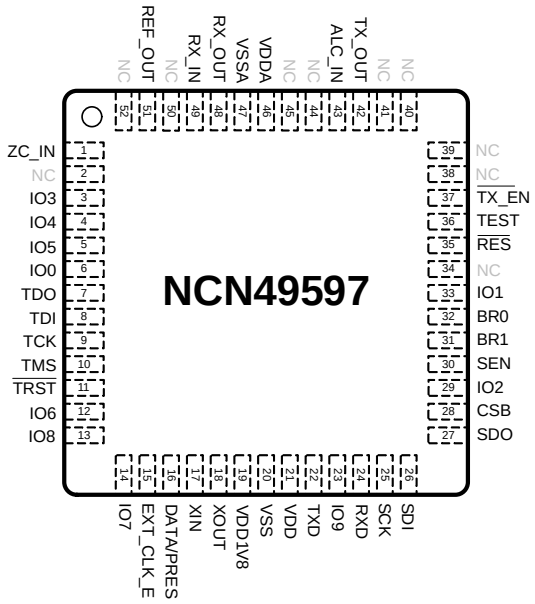


Figure 2. QFN Pin−out of NCN49597 (top view)

Table 4. NCN49597 QFN PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	I/O	Type	Description
1	ZC_IN	In	A	50/60 Hz input for mains zero crossing detection
3..5, 12..14	IO3..IO7	In/Out	D, 5VS, ST	General purpose I/O's (Note 3)
6, 33	IO0, IO1	In/Out	D, 5VS, ST	General purpose I/O's (Notes 3 and 4)
13, 23	IO8, IO9	In/Out	D, 5VS, ST, PD	General purpose IO (Notes 3 and 9)
7	TDO	Out	D	JTAG test data output
8	TDI	In	D, 5VS, PD, ST	JTAG test data input (Note 7)
9	TCK	In	D, 5VS, PD	JTAG test clock (Note 7)
10	TMS	In	D, 5VS, PD	JTAG test mode select (Note 7)
11	TRSTB	In	D, 5VS, PD, ST	JTAG test reset (active low) (Note 8)
15	EXT_CLK_E	In	D, 5VS, PD, ST	External clock enable input
16	DATA/PRES	Out	D, 5VS, OD	Output of transmitted data (DATA) or PRE_SLOT signal (PRES)
17	XIN	In	A, 1.8 V	Crystal oscillator input
18	XOUT	Out	A, 1.8 V	Crystal oscillator output (output must be left floating when XIN is driven by an external clock)
19	VDD1V8		P	1.8 V regulator output. A decoupling capacitor of at least 1 μF is required for stability
20	VSS		P	Digital ground
21	VDD		P	3.3 V digital supply

3. The direction and function of the general−purpose I/O's is controlled by the firmware. Depending on the firmware behavior, a general−purpose IO (GPIO) used as an output may appear as an open−drain, push−pull or open−source pin. Refer to the firmware documentation for details.
4. During boot (i.e., before firmware has been uploaded) this pin is an output and indicates the status of the boot loader. Once firmware has been loaded, the pin is available as a GPIO.
5. During normal operation, this pin *must* be tied to ground (recommended) or left open.
6. If the modem is not loading the firmware from an external SPI memory, it is recommended that this pin is tied to ground or Vdd.
7. During normal operation, it is recommended that this pin is tied to ground.
8. During normal operation, this pin must be tied to Vdd.
9. If a general purpose IO is configured as an output, the pull−down resistor is disconnected.

Table 4. NCN49597 QFN PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	I/O	Type	Description
22	TXD	Out	D, 5VS, OD	UART transmit output
24	RXD	In	D, 5VS, ST	UART receive input
25	SCK	Out	D, 5VS	SPI interface to external Flash: clock
26	SDI	In	D, 5VS, ST	SPI interface to external Flash: serial data input (Note 6)
27	SDO	Out	D, 5VS	SPI interface to external Flash: serial data output
28	CSB	Out	D, 5VS	SPI interface to external Flash: chip select
29	IO2	In/Out	D, 5VS, ST	Must be kept low while firmware is loaded over the serial interface; available as a normal GPIO afterwards (Note 3)
30	SEN	In	D, 5VS, PD, ST	Boot mode selection (refer to Boot Loader section)
31	BR1	In	D, 5VS	UART baud rate selection
32	BR0	In	D, 5VS	UART baud rate selection
35	RESB	In	D, 5VS, ST	Reset (active low)
36	TEST	In	D, 5VS, PD, ST	Production hardware test enable (Note 5)
37	TX_ENB	Out	D, 5VS, OD	Transmit enable (active low)
42	TX_OUT	Out	A	Transmitter output
43	ALC_IN	In	A	Automatic level control input
46	VDDA		P	3.3 V analog supply
47	VSSA		P	Analog ground
48	RX_OUT	Out	A	Output of receiver operational amplifier
49	RX_IN	In	A	Non−inverting input of receiver operational amplifier
51	REF_OUT	Out	A	Internal voltage reference. A decoupling capacitor of at least 1 μF is required for stability
2, 34, 38..41, 44, 45,50, 52	NC			These pins are not connected and must be connected to ground (recommended) or left open

3. The direction and function of the general−purpose I/O's is controlled by the firmware. Depending on the firmware behavior, a general−purpose IO (GPIO) used as an output may appear as an open−drain, push−pull or open−source pin. Refer to the firmware documentation for details.
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6. If the modem is not loading the firmware from an external SPI memory, it is recommended that this pin is tied to ground or Vdd.
7. During normal operation, it is recommended that this pin is tied to ground.
8. During normal operation, this pin must be tied to Vdd.
9. If a general purpose IO is configured as an output, the pull−down resistor is disconnected.

P:	Power pin	5VS:	5 V safe; pin that supports the presence of 5 V if used as input or as open−drain output
A:	Analog pin	Out:	Output signal
D:	Digital pin	In:	Input signal
PD:	Internal Pull Down resistor (Note 9)	ST:	Schmitt trigger input.
OD:	Open Drain Output	1.8V:	The maximal voltage on this pin is 1.8 V

Table 5. ELECTRICAL CHARACTERISTICS
All parameters are valid for T_J = −40°C to 125°C, V_{DD} = 3.3 V, f_{CLK} = 48 MHz ± 50 ppm unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INTERNAL VOLTAGE REGULATOR: PIN VDD1V8 (power supply and voltage reference)						
V_{DD} and V_{DDA} current consumption		V_{DD18}	1.62	1.80	1.98	V
	During reception (Note 10)	I_{RX}		40	60	mA
	During transmission (Note 10)	I_{TX}		40	60	mA
	RESB = 0	I_{RESET}			4	mA
OSCILLATOR: PIN XIN, XOUT (Note 11)						
Duty cycle with quartz connected			35		65	%
Start−up time		$T_{startup}$			15	ms
Load capacitance external crystal		C_L			18	pF
Series resistance external crystal		R_S	1	6	60	Ω
Maximum Capacitive load on XOUT	XIN used as clock input	CL_{XOUT}			15	pF
Low input threshold voltage	XIN used as clock input	VIL_{XOUT}	0.3 V_{DD18}			V
High input threshold voltage	XIN used as clock input	VIH_{XOUT}			0.7 V_{DD18}	V
Low output voltage	XIN used as clock input, XOUT = 2 mA	VOL_{XOUT}			0.3	V
High input voltage	XIN used as clock input	VOH_{XOUT}			V_{DD18} − 0.3	V
Rise and fall time on XIN	XIN used as clock input	t_{rXIN_EXT}			1.5	ns
ZERO CROSSING DETECTOR AND 50/60 HZ PLL: PIN ZC_IN						
Mains voltage input range	With protection resistor at ZC_IN (Note 12)	V_{MAINS}	90		550	V_{PK}
Rising threshold level		VIR_{ZC_IN}			1.9	V
Falling threshold level		VIF_{ZC_IN}	0.85			V
Hysteresis		VHY_{ZC_IN}	0.4			V
Lock range (Note 13)	R_CONF[0] = 0 (50 Hz)	$Flock_{50Hz}$	45		55	Hz
	R_CONF[0] = 1 (60 Hz)	$Flock_{60Hz}$	54		66	Hz
Lock time (Note 13)	R_CONF[0] = 0 (50 Hz)	$Tlock_{50Hz}$			15	s
	R_CONF[0] = 1 (60 Hz)	$Tlock_{60Hz}$			20	s
Frequency variation without going out of lock (Note 13)	R_CONF[0] = 0 (50 Hz)	DF_{60Hz}			0.1	Hz/s
Frequency variation without going out of lock (Note 13)	R_CONF[0] = 1 (60 Hz)	DF_{50Hz}			0.1	Hz/s
Jitter of CHIP_CLK (Note 13)		$Jitter_{CHIP\_CLK}$			25	μs

10. With typical firmware. The exact value depends on the firmware variant loaded and the firmware configuration.
11. In production the actual oscillation of the oscillator and duty cycle will not be tested. The production test will be based on the static parameters and the inversion from XIN to XOUT in order to guarantee the functionality of the oscillator.
12. This parameter is not tested in production.
13. These parameters will not be measured in production as the performance is determined by a digital circuit. Correct operation of this circuit will be guaranteed by the digital test patterns.

Table 5. ELECTRICAL CHARACTERISTICS
All parameters are valid for T_J = −40°C to 125°C, V_{DD} = 3.3 V, f_{CLK} = 48 MHz ± 50 ppm unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
TRANSMITTER EXTERNAL PARAMETERS: PIN TX_OUT, ALC_IN, TX_ENB						
AC output level	f_{TX_OUT} = 23 – 75 kHz (Note 14) f_{TX_OUT} = 148.5 kHz (Note 14)	V_{TX_OUT}	0.85 0.76		1.15 1.22	V_{PK}
DC output level		V_{TX_OUT}		1.65		V
Second order harmonic distortion	f_{TX_OUT} = 148.5 kHz (Note 14)	HD2			−55	dB
Third order harmonic distortion	f_{TX_OUT} = 148.5 kHz (Note 14)	HD3			−57	dB
Transmitted carrier frequency resolution		Rf_{TX_OUT}	11.44		11.44	Hz
Transmitted carrier frequency accuracy	(Note 15)	Df_{TX_OUT}			30	Hz
Capacitive output load at pin TX_OUT	(Note 15)	CL_{TX_OUT}			20	pF
Resistive output load at pin TX_OUT		RL_{TX_OUT}	5		5	kΩ
Turn off delay of TX_ENB output		Td_{TX_ENB}	0.25		0.5	ms
Automatic level control attenuation step		ALC_{step}	2.9		3.1	dB
Maximum attenuation		ALC_{range}	20.3		21.7	dB
Low threshold level on ALC_IN	With DC bias equal to V_{REF_OUT}	VTL_{ALC_IN}	0.34		0.46	V_{PK}
High threshold level on ALC_IN	With DC bias equal to V_{REF_OUT}	VTH_{ALC_IN}	0.54		0.72	V_{PK}
Input impedance of ALC_IN pin		R_{ALC_IN}	111		189	kΩ
Power supply rejection ratio of the transmitter section	f = 50 Hz (Note 16) f = 10 kHz (Note 16)	$PSRR_{TX\_OUT}$	32 10			dB
Transmit cascade gain (Note 17)	f = 10 kHz f = 148.5 kHz f = 195 kHz f = 245 kHz f = 500 kHz f = 1 MHz f = 2 MHz	$V_{TX\_PF\_10kHz}$ $V_{TX\_LPF\_148kHz5}$ $V_{TX\_LPF\_195kHz}$ $V_{TX\_LPF\_245kHz}$ $V_{TX\_LPF\_500kHz}$ $V_{TX\_LPF\_1000kHz}$ $V_{TX\_LPF\_2000kHz}$	−0.5 −1.3 −4.5	 −36 −50	0.5 0.5 −1.5 −3 −18	dB

14. With the level control register set for maximal output amplitude. Tested with low pass filter tuned for CENELEC D−band.
15. This parameter will not be tested in production.
16. A sinusoidal signal of 100 mVpp is injected between VDDA and VSSA while the digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.
17. The cascade of the digital−to−analog converter (DAC), low−pass filter (LPF), and transmission amplifier is production tested and must have a frequency characteristic between the limits listed. The level is specified relative to the level at DC; the absolute output level will depend on the operating condition.
    This test is done with the low−pass filter (LPF) tuned to include the CENELEC D−band. In production the measurement will be done for relative to DC with a signal amplitude of 100 mV.

Table 5. ELECTRICAL CHARACTERISTICS
All parameters are valid for T_J = −40°C to 125°C, V_{DD} = 3.3 V, f_{CLK} = 48 MHz ± 50 ppm unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RECEIVER EXTERNAL PARAMETERS: PIN RX_IN, RX_OUT, REF_OUT						
Input offset voltage	AGC gain = 42 dB	$V_{OFFS\_RX\_IN}$			5	mV
	AGC gain = 0 dB	$V_{OFFS\_RX\_IN}$			50	mV
Max. peak input voltage (corresponding to 62.5% of the ADC full scale)	AGC gain = 0 dB (Note 18)	$V_{MAX\_RX\_IN}$	0.85		1.15	V_{PK}
Input referred noise of the analog receiver path	AGC gain = 42 dB (Notes 18 and 19)	NF_{RX_IN}			150	nV/√Hz
Input leakage current of receiver input		$I_{LE\_RX\_IN}$	−1		1	μA
Max. current delivered by REF_OUT		$I_{Max\_REF\_OUT}$	−300		300	μA
Power supply rejection ratio of the receiver input section	f = 50 Hz (Note 20)	$PSRR_{LPF\_OUT}$	35			dB
	f = 10 kHz (Note 20)		10			dB
AGC gain step		AGC_{step}	5.3		6.7	dB
AGC range		AGC_{range}	39.9		44.1	dB
Analog ground reference output voltage	Load current ±300 μA	V_{REF_OUT}	1.52	1.65	1.78	V
Signal to noise ratio (Notes 18 and 20)	Signal amplitude of 62.5% of the full scale of the ADC	SN_{AD_OUT}	54			dB
Clipping level at the output of the gain stage (RX_OUT)		$V_{CLIP\_AGC\_IN}$	1.05		1.65	V_{PK}
Receive cascade gain (Note 22)	f = 10 kHz, A = 250 mVpk f = 148.5 kHz, A = 250 mVpk f = 195 kHz, A = 250 mVpk f = 245 kHz, A = 250 mVpk f = 500 kHz, A = 250 mVpk f = 1 MHz f = 2 MHz	$V_{RX\_LPF\_10kHz}$ $V_{RX\_LPF\_148.5kHz}$ $V_{RX\_LPF\_195kHz}$ $V_{RX\_LPF\_245kHz}$ $V_{RX\_LPF\_500kHz}$ $V_{RX\_LPF\_1000kHz}$ $V_{RX\_LPF\_2000kHz}$	−0.5 −1.3 −4.5	0 −36 −50	0.5 0.5 −1 −3 −18	dB
POWER−ON−RESET (POR)						
POR threshold (Note 23)	V_{DD} and V_{DDA} rising	V_{PORH}			2.7	V
	V_{DD} and V_{DDA} falling	V_{PORL}	2.1			
Power supply rise time	0 to 3 V on both V_{DD} and V_{DDA}	T_{RPOR}	1			ms
DIGITAL OUTPUTS: TDO, SCK, SDO, CSB, IO0..IO9						
Low output voltage (Note 24)	I_{XOUT} = 4 mA	V_{OL}			0.4	V
High output voltage (Note 24)	I_{XOUT} = −4 mA	V_{OH}	0.85 V_{DD}			V
DIGITAL OUTPUTS WITH OPEN DRAIN: TX_ENB, TXD, DATA/PRES						
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V
DIGITAL INPUTS: BR0, BR1						
Low input level		V_{IL}			0.2 V_{DD}	V
High input level	0 to 3 V	V_{IH}	0.8 V_{DD}			V
Input leakage current		I_{LEAK}	−2		2	μA

18. Input at RX_IN, no other external components.
19. Characterization data only. Not tested in production.
20. A sinusoidal signal of 100 mVpp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT and REF_OUT output is measured to determine the parameter. The AGC gain is fixed at 42 dB.
21. These parameters will be tested in production with an input signal of 95 kHz and 1 V_{PK} by reading out the digital samples at the output of the ADC. The AGC gain is switched to 0 dB.
22. The cascade of the receive low−pass filter (LPF), AGC and low noise amplifier is production tested and must have a frequency characteristic between the limits listed. The level is specified relative to the level at DC; the absolute output level will depend on the operating condition. This test is done with the low−pass filter (LPF) tuned to include the CENELEC D−band.
23. The nominal voltage on the pins VDD and VDDA (the digital and analog power supply) must be equal; both supply rail must be switched together.
24. For IO0..IO9, this parameter only applies if the pin is configured as output pin by the firmware.

Table 5. ELECTRICAL CHARACTERISTICS
All parameters are valid for T_J = −40°C to 125°C, V_{DD} = 3.3 V, f_{CLK} = 48 MHz ± 50 ppm unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DIGITAL INPUTS WITH PULL−DOWN: TDI, TMS, TCK, TRSTB, TEST, SEN, IO8, IO9						
Low input level (Note 25)		V_{IL}			0.2 V_{DD}	V
High input level (Note 25)		V_{IH}	0.8 V_{DD}			V
Pull−down resistor (Note 25)	Measured at V_{Pin} = V_{DD} / 2	R_{PU}	35	100	170	kΩ
DIGITAL SCHMITT TRIGGER INPUTS: RXD, RESB, IO0..IO7, SDI						
Rising threshold level (Note 26)		V_{T+}			0.80 V_{DD}	V
Falling threshold level (Note 26)		$V_{T−}$	0.2 V_{DD}			V
Input leakage current (Note 26)		I_{LEAK}	−2		2	μA
BOOT LOADER TIMING (Parameters are valid for a baud rate of 115'200) (Note 27)						
IO2 setup time to falling edge of RESB	(Note 28)	t_{2s}	5			μs
Boot loader startup time	(Notes 28 and 29)	t_{stx}		135	200	ms
Inter−byte timeout sent to modem	(Note 28)	t_{IB}			20	ms
Boot loader acknowledgement after last byte correctly received	(Note 28)	t_{ACK}		3.6	12	ms
IO2 hold time after start of acknowl-edgement byte transmission	(Note 28)	t_{2h}	36			μs

25. For IO8 and IO9, this parameter only applies if the pin is configured as input pin by the firmware.
26. For IO0…IO7, this parameter only applies if the pin is configured as input pin by the firmware.
27. The timing constraints governing the boot loader when uploading firmware over the serial interface are illustrated in Figure 3.
28. These parameters will not be measured in production as the performance is determined by a digital circuit.
29. This parameter is specified with the oscillator stable. Refer to $T_{startup}$ for oscillator startup information.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

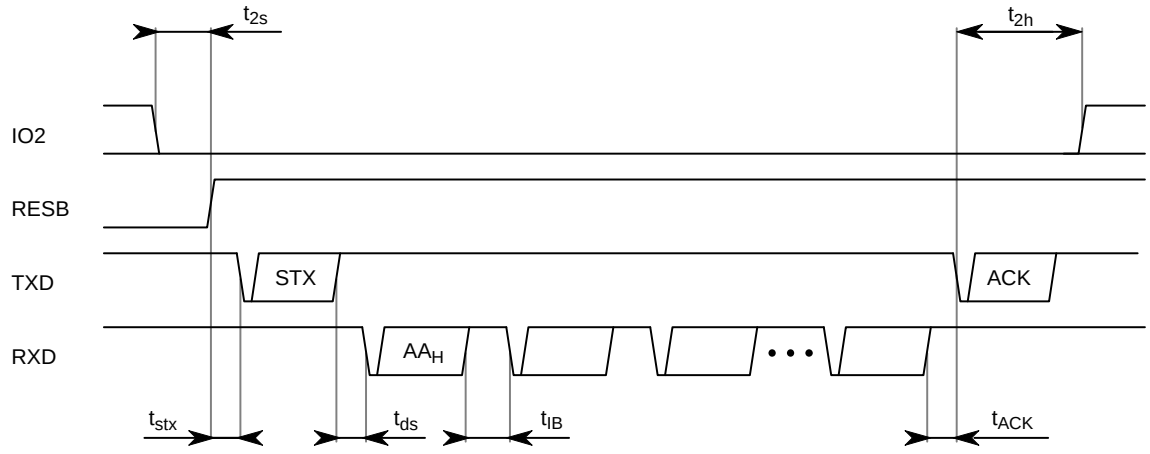

Figure 3. Timing Constraints for Uploading the Firmware over the Serial Communication Interface (SCI)

Typical Performance Characteristics

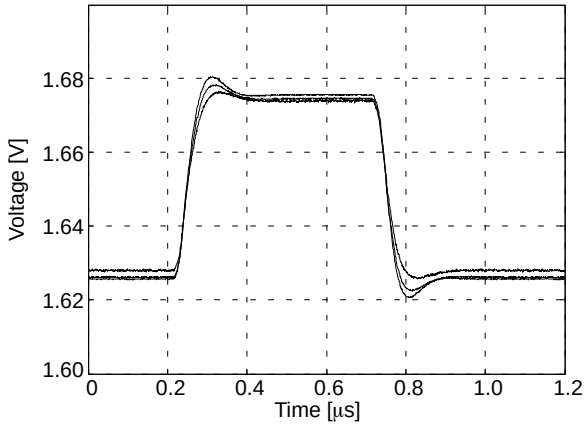

Figure 4. Receiver Opamp — Small signal transient response for (top to center) no load, 10 kΩ load, 3.6 kΩ load

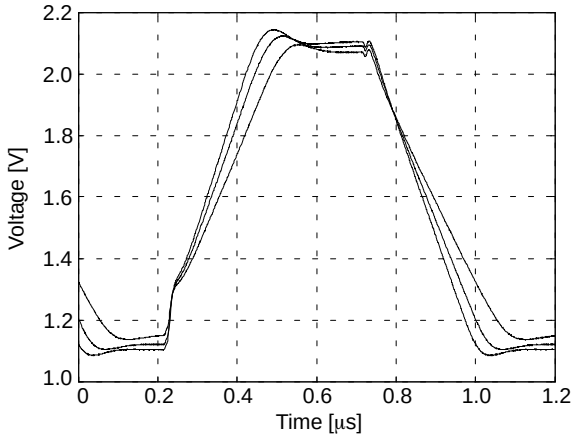

Figure 5. Receiver Opamp — Large signal transient response for (top to center) no load, 10 kΩ load, 3.6 kΩ load

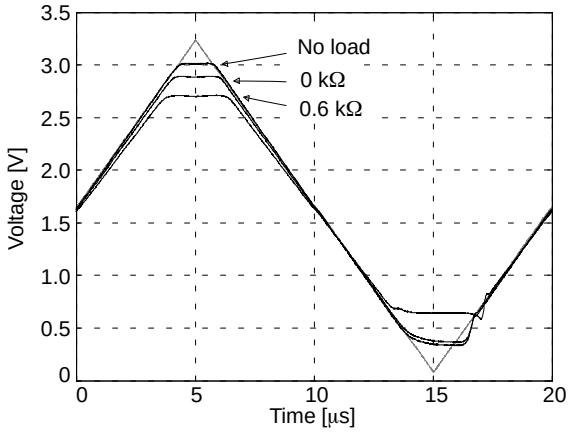

Figure 6. Receiver Opamp — Output overdrive recovery behavior. The input signal is shown in grey

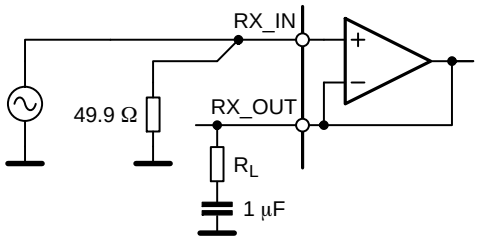

Figure 7. Test Circuit for Figures 4–6

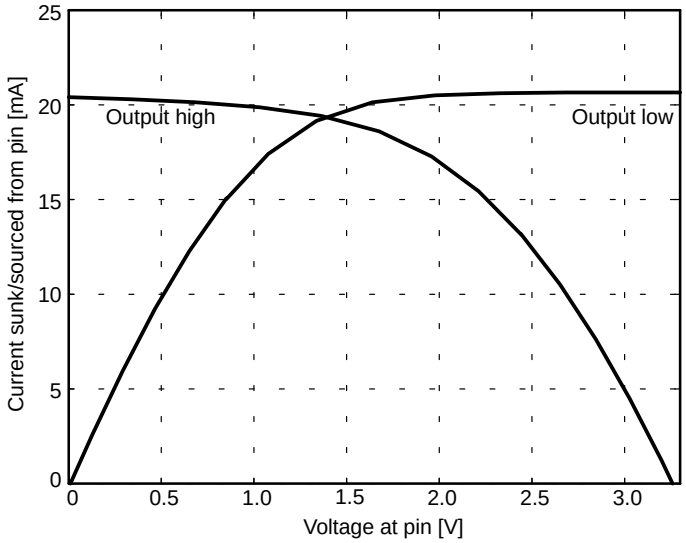

Figure 8. GPIO Current Sourcing and Sinking Capability

General Description

The NCN49597 is a single chip half duplex S−FSK modem designed for hostile communication environments with very low signal−to−noise ratio (SNR) and high interference. It is particularly suited for power line carrier (PLC) data transmission on low−or medium−voltage power lines.

Together with firmware, the device handles of the lower layers of communication protocols. Firmware solutions are provided by ON Semiconductor royalty−free for the ON−PL110 protocol. It handles the physical, Media Access Control (MAC) and Logical Link Control (LLC) layers on−chip. For more information, refer to the dedicated software datasheet.

Because the lower layers are handled on−chip, the NCN49597 provides an innovative architectural split. The user benefits from a higher level abstraction. Compared to a low−level interface, the NCN49597 allows faster development of applications: the user just needs to send the raw data to the NCN49597 and no longer has to take care of the details of the transmission over the specific medium. The latter part easily represents half of the software development cost.

Figure 9 shows the building blocks of the NCN49597. Refer to the sections below for a detailed description.

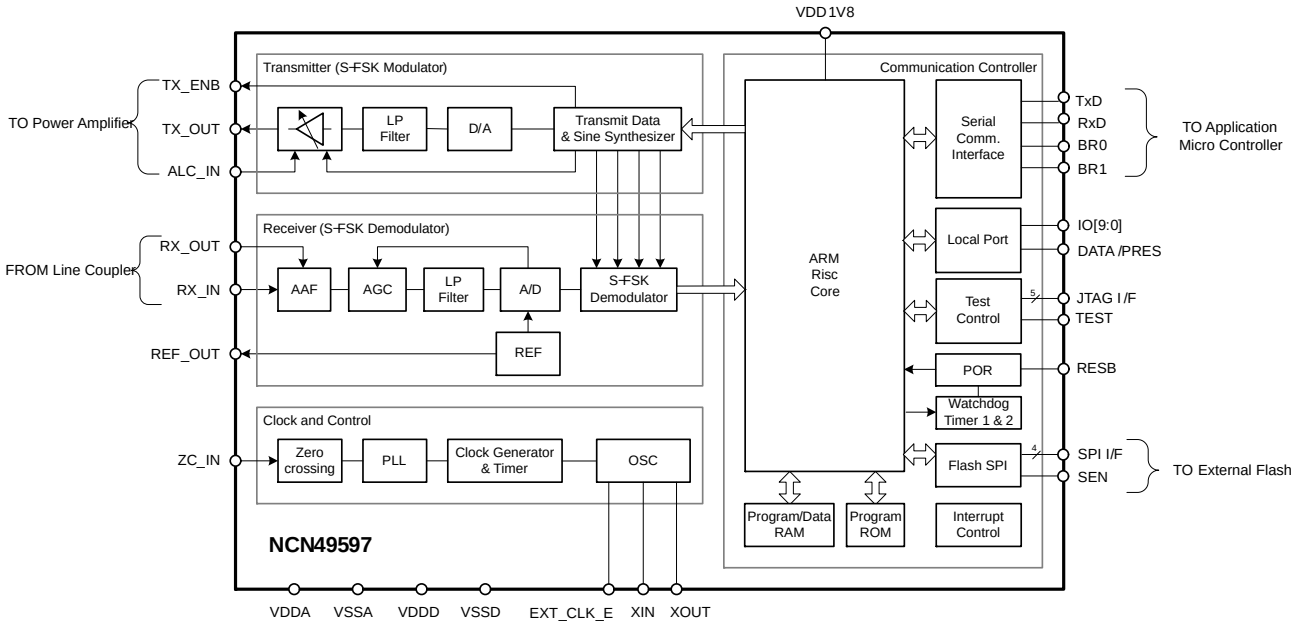

Figure 9. Block Diagram of the NCN49597 S−FSK Modem

NCN49597 complies with the CENELEC EN 50065−1 and EN 50065−7 standards. It operates from a single 3.3 V power supply and is interfaced to the power line by an external line driver and transformer. An internal PLL is locked to the mains frequency and is used to synchronize the data transmission at data rates of 300, 600, 1200, 2400 and 4800 baud for a 50 Hz mains frequency, or 360, 720, 1440, 2880 and 5760 baud for a 60 Hz mains frequency. In both cases this corresponds to 3, 6, 12 or 24 data bits per half cycle of the mains period.

S−FSK is a modulation and demodulation technique that combines some of the advantages of a classical spread spectrum system (e.g. immunity against narrow band interferers) with the advantages of the classical FSK system (low complexity). The transmitter assigns the space frequency f_S to “data 0” and the mark frequency f_M to “data 1”. In contrast to classical FSK, the modulation carriers f_S and f_M used in S−FSK are placed well apart. As interference and signal attenuation seen at the carrier frequencies are now less correlated, this results in making their transmission quality independent from each other. Thus, more robust communication is possible in interference−prone environments. The frequency pairs supported by the NCN49597 are in the range of 9–150 kHz with a typical separation of 10 kHz.

The conditioning and conversion of the signal is performed at the analog front−end of the circuit. All further processing of the signal and the handling of the protocol is fully digital. The digital processing of the signal is partitioned between hardwired blocks and a microprocessor block. Where timing is most critical, the functions are implemented with dedicated hardware. For the functions where the timing is less critical − typically the higher level functions − the circuit makes use of an integrated ARM microprocessor core. An internal random−access memory (RAM) stored the firmware and the working data.

After the modem has been reset, the user must upload the firmware into the modem memory. This may be done over

the asynchronous serial interface (discussed below); alternatively, the modem can autonomously retrieve the firmware from an attached SPI memory. For details, refer to the Boot Loader section.

The modem communicates to the application microcontroller over a Serial Communication Interface (SCI), a standard asynchronous serial link, which allows interfacing with any microcontroller with a free UART. The SCI works on two wires: TXD and RXD. The baud rate is programmed by setting two pins (BR0, BR1).

The NCN49597, together with an NCS5651 line driver, is functionally equivalent to the NCN49599 modem. Thus, the same user software works equally well with the NCN49597 as with the NCN49599.

Converting AMIS−49587−based Designs to NCN49597

The NCN49597 is designed to allow easy adaptation of printed circuit board designs using the AMIS−49587. All connected pins of the latter (QFN package) are present in the same location in the NCN49597.

Four important hardware changes must be noted.

Most of the not−connected (NC) pins of the AMIS−49587 are functional in the NCN49597. If these pins were previously connected to ground (a commendable practice) this must be taken into account. IO4–IO10 are usually configured as inputs and can therefore be grounded safely. However, it must be considered that some NC pins of AMIS−49587 are outputs in the NCN49597. These include pins SDO, SCK and, CSB. IO0 and IO1 are used typically used by the firmware as status indicators. IO3 is used by the ON PL110 firmware for controlling the amplifier enable signal.

Secondly, the NCN49597 incorporates an internal 1.8 V regulator to power the digital core. For stability, a 1 μF capacitor to ground must be connected on pin 19 (VDD1V8).

In addition, the lowest baud rate setting of the AMIS−49587 serial interface (BR0 & BR1 pulled low; 4800 baud) has been replaced by 115200 baud. All other BR0 and BR1 settings will result in the same baud rate.

Finally, a 48 MHz crystal is required for the NCN49597; the AMIS−49587 used a 24 MHz crystal.

The firmware running on the modem has been updated substantially compared to the AMIS−49587. As a result, the interface protocol between the user microcontroller and the modem is completely different. Refer to the firmware datasheet for details.

Detailed Hardware Description

Clock and Control

The clock and control block (Figure 10) provides the modem with the clock and synchronization signals required for correct data transmission and reception. It is composed of the zero−crossing detector, phase locked loop (PLL), oscillator and clock generator.

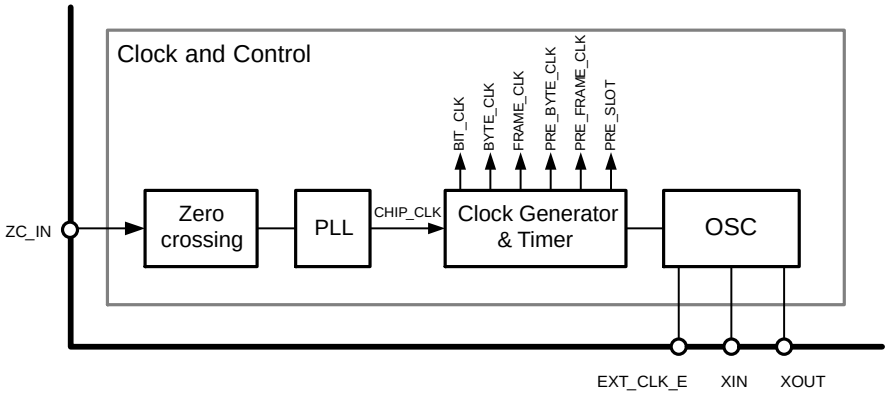

Figure 10. Clock and Control Block

Oscillator

The NCN49597 may be clocked from a crystal with the built−in oscillator or from an external clock. XIN is the input to the oscillator inverter gain stage; XOUT the output. XOUT cannot be used directly as a clock output as no additional loading is allowed on the pin due to the limited voltage swing. This applies both to operation with a crystal and an external oscillator.

If an external clock of 48 MHz is to be used, the pin EXT_CLK_E must be pulled to V_{DD} and the clock signal connected to XIN. Note that the high level on XIN must not exceed the voltage of the internal voltage regulator (V_{DD18}, or about 1.8 V). The output must be floating.

If a crystal is to be used, the pin EXT_CLK_E should be strapped to V_{SSA} and the circuit illustrated in Figure 11 should be employed.

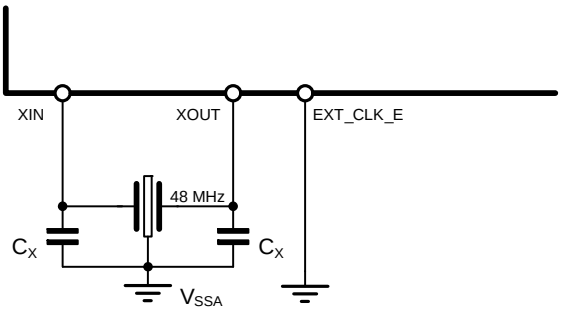

Figure 11. Clocking the NCN49597 with a Crystal

Correct operation is only possible with a parallel resonance crystal of 48 MHz. A crystal with a load capacitance C_L of 18 pF is recommended.

The load capacitance is the circuit capacitance appearing between the crystal terminals; it must be within the range specified by the crystal manufacturer for correct operation at the desired frequency. C_L is determined by the external capacitors C_X and stray capacitance (C_{STRAY}):

$C_L = C_X / 2 + C_{STRAY}$

Stray capacitance typically ranges from 2 to 5 pF. This results in a typical C_X value of 33 pF.

The printed circuit board should be designed to minimize stray capacitance and capacitive coupling to other parts by keeping traces as short as possible. The quality of the ground plane below the oscillator components is critical.

To guarantee startup, the series loss resistance of the crystal must be smaller than 60 Ω.

The oscillator output f_{CLK} (48 MHz) is the base clock for the entire modem. The microcontroller clock, f_{ARM}, is taken directly from f_{CLK}. The clock for the transmitter, f_{TX_CLK}, is equal to f_{CLK} / 4 or 12 MHz; the master receiver clock, f_{RX_CLK}, equals f_{CLK} / 8 or 6 MHz. All the internal clock signals of the transmitter and the receiver will be derived from f_{TX_CLK} resp. f_{RX_CLK}.

Zero Crossing Detector

Depending on the standard and the application, synchronization with the mains zero crossing may be required.

In order to recover this timing information, a zero cross detection of the mains is performed.

Recommended circuits for the detection of the mains zero crossing appear in the Application Note “Mains synchronization for PLC modems”. In case of the modem is not isolated from the mains a series resistor of 1 MΩ in combination with two external Schottky clamp diodes is recommended (Figure 12). This will limit the current flowing through the internal protection diodes.

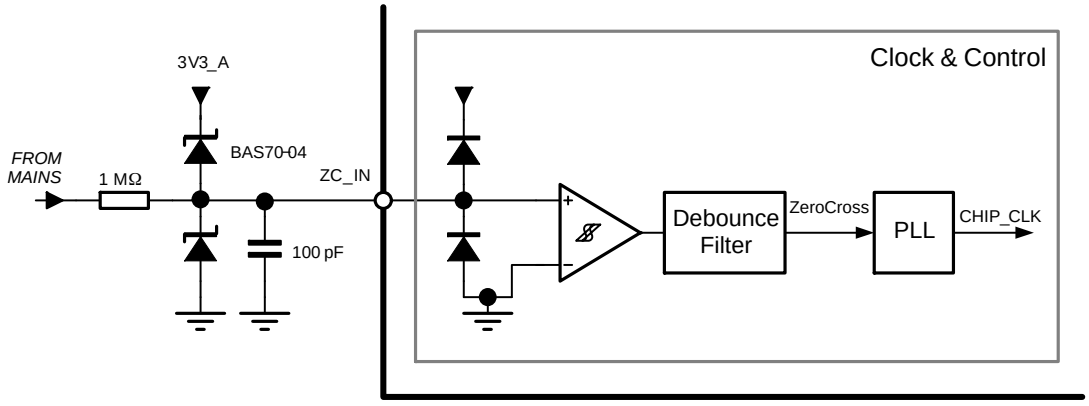

Figure 12. Zero Crossing Detector with Falling−edge De−bounce Filter

ZC_IN is the mains frequency sense pin. A comparator with Schmitt trigger ensures a signal with edges, even in the presence of noise. In addition, the falling edges of the detector output are de−bounced with a delay of 0.5–1 ms. Rising edges are not de−bounced.

Because the detector threshold is not 0 V but slightly positive, the rising edge of the output is delayed compared to the actual rising mains zero crossing (Figure 13).

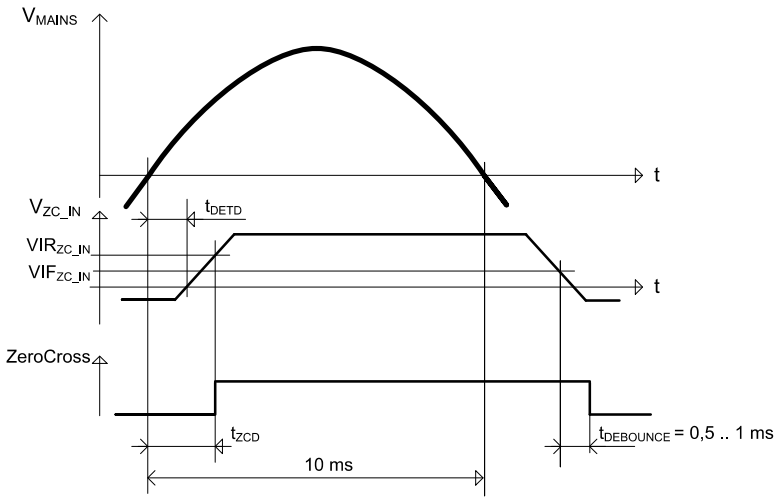

Figure 13. Zero Crossing Detector Signals and Timing (example for 50 Hz)

Phase Locked Loop (PLL)

A phase−locked loop (PLL) structure converts the signal at the ZC_IN comparator output to the chip clock (CHIP_CLK). This clock is used for modulation and demodulation and runs 8 times faster than the bit rate; as a result, the chip clock frequency depends on the mains frequency and the baud rate.

The filters of the PLL are dependent on the baud rate and the mains frequency. They must be correctly configured using the register R_CONF. The bit R_CONF[0] specifies the mains frequency, with a cleared bit (0) corresponding to 50 Hz; a set bit (1) to 60 Hz. The bits R_CONF[2:1] control the number of data bits per mains period. The values 00b, 01b, 10b and 11b correspond to 6, 12, 24 and 48 bits per mains period of 20 ms (50 Hz) or 16.7 ms (60 Hz).

Together this results in the baud rates and chip clock frequencies shown in Table 6.

Table 6. CHIP_CLK IN FUNCTION OF SELECTED BAUD RATE AND MAINS FREQUENCY

R_CONF[0]	Mains frequency	R_CONF[2:1]	Baudrate	CHIP_CLK
0	50 Hz	00b	300 bps	2400 Hz
		01b	600 bps	4800 Hz
		10b	1200 bps	9600 Hz
		11b	2400 bps	19200 Hz
1	60 Hz	00b	360 bps	2880 Hz
		01b	720 bps	5760 Hz
		10b	1440 bps	11520 Hz
		11b	2880 bps	23040 Hz

The PLL significantly reduces the clock jitter. This makes the modem less sensitive to timing variations; as a result, a cheaper zero crossing detector circuit may be used.

The PLL input is only sensitive to rising edges.

If no zero crossings are detected, the PLL freezes its internal timers in order to maintain the CHIP_CLK timing.

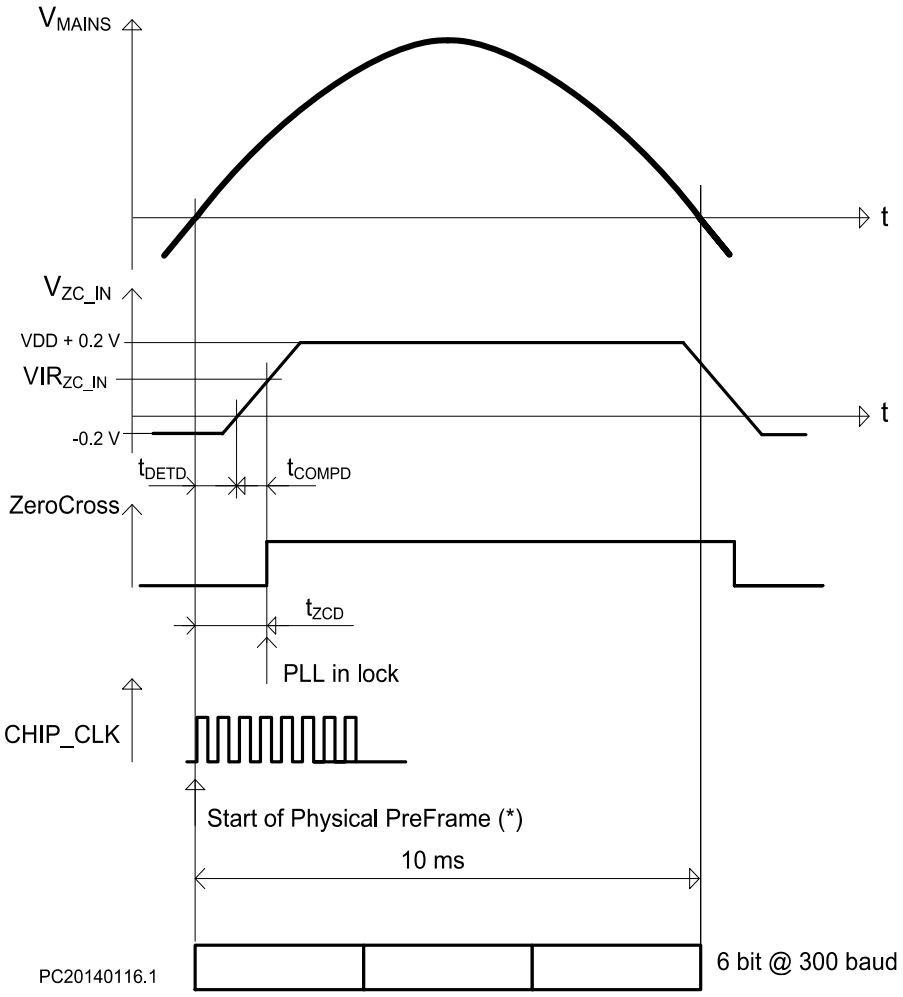

Figure 14. Using the ZC_ADJUST Register to Compensate for Zero Crossing Delay (example for 50 Hz)

The PLL ensures the generated chip clock is in phase with the rising edge of comparator output. However, these edges are not precisely in phase with the mains.

Inevitably, the external zero crossing detector circuit suffers from a delay t_{DETD} (e.g. caused by an optocoupler). In addition, the comparator threshold is not zero (VIR_{ZC_IN} = 1.9 V); this results in a further delay, t_{COMP0} between the rising edge of the signal on pin ZC_IN and the rising edge on the comparator output (as noted before, the PLL takes only the rising edge into account).

The combination of these delays would cause the modem to emit and receive data frames too late.

Therefore, the PLL allows tuning the phase difference between its input and the chip clock. The CHIP_CLK may be brought forward by setting the register R_ZC_ADJUST. The adjustment period or granularity is 13 μs, with a maximum adjustment of 255 x 13 μs = 3.3 ms, corresponding with a sixth of the 50 Hz mains sine period.

This is illustrated in Figure 9. The “physical frame” (i.e., the modulated signal appearing on the mains) starts earlier with R_ZC_ADJUST[7:0] x 13 μs to compensate for the zero cross delay.

The delay corresponding with the value of R_ZC_ADJUST is also listed in Table 7.

Table 7. ZERO CROSSING DELAY COMPENSATION

R_ZC_ADJUST[7:0]	Compensation
0000 0000	0 μs (reset value)
0000 0001	13 μs
0000 0010	26 μs
0000 0011	39 μs
...	...
1111 1111	3315 μs

Clock Generator and Timer

The timing generator (Figure 10, center) is responsible for all synchronization signals and interrupts related to S−FSK communication.

The timing is derived from the chip clock (CHIP_CLK, generated by the PLL) and the main oscillator clock f_{CLK}. The timing has a fixed repetition rate, corresponding to the length of a physical subframe (see reference [1]).

When the NCN49597 switches between receive and transmit mode, the chip clock counter value is maintained. As a result, the same timing is maintained for reception and transmission. Seven timing signals are defined:

- **CHIP_CLK** is the output of the PLL and the input of the timing generator. It runs 8 times faster than the bit rate on the physical interface.
- **BIT_CLK** is only active at chip clock counter values that are multiples of 8 (0, 8, .., 2872). It indicates the start of the transmission of a new bit.
- **BYTE_CLK** is only active at chip clock counter values that are multiples of 64 (0, 64, .., 2816). It indicates the start of the transmission of a new byte.
- **FRAME_CLK** is only active at counter value 0; it indicates the transmission or reception of a new frame.
- **PRE_BYTE_CLK** follows the same pattern as BYTE_CLK, but precedes it by 8 chip clocks. It can be used as an interrupt for the internal microcontroller and indicates that a new byte for transmission must be generated.
- **PRE_FRAME_CLK** follows the same pattern at FRAME_CLK, but precedes it by 8 chip clocks. It can be used as an interrupt for the internal microcontroller and indicates that a new frame will start at the next FRAME_CLK.
- **PRE_SLOT** is active between the rising edge of PRE_FRAME_CLK and the rising edge of FRAME_CLK. This signal can be provided at the digital output pin DATA/PRES when R_CONF[7] = 0. Thus, the external host controller may synchronize its software with the internal FRAME_CLK of the NCN49597. Refer to the SCI section and Table 11 for details.

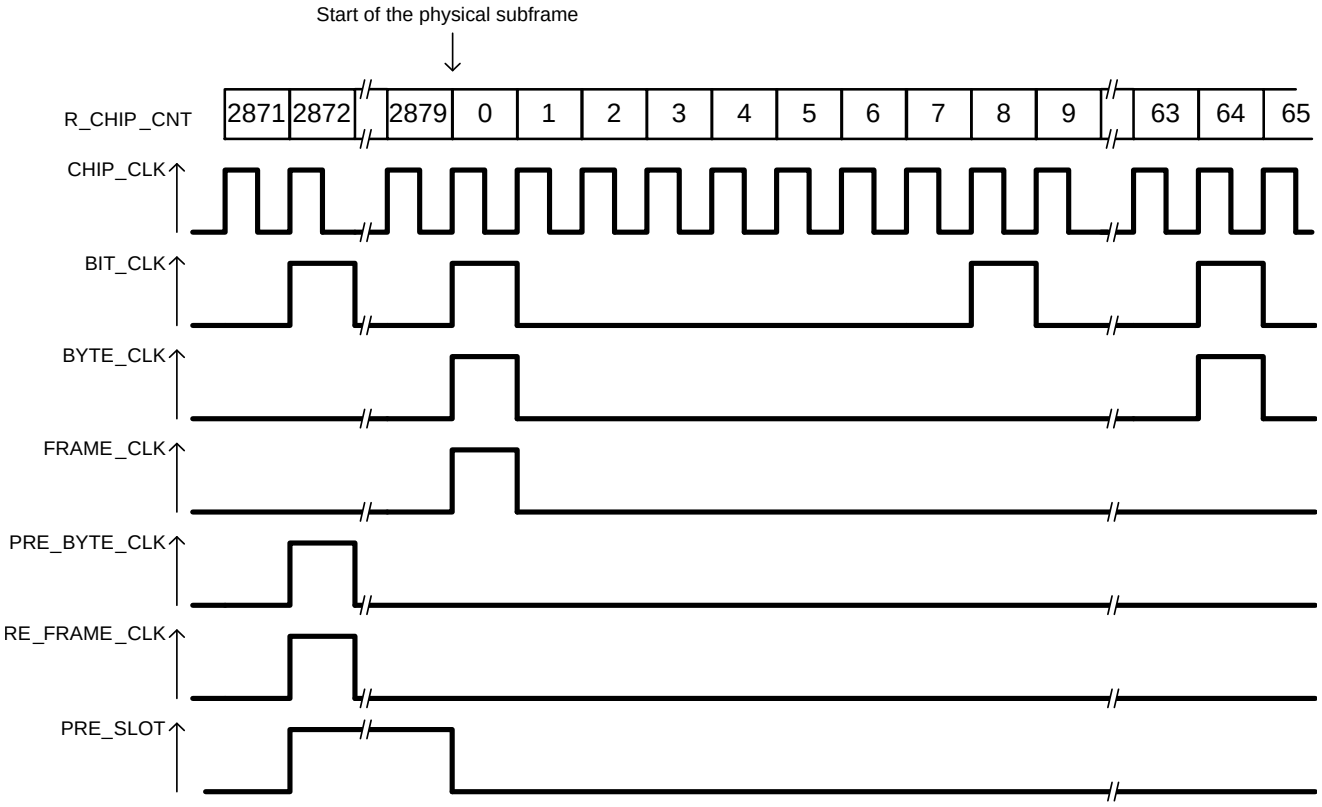

Figure 15. Timing Signals

Transmitter Path Description (S−FSK Modulator)

The NCN49597 transmitter block (Figure 16) generates the signal to be sent on the transmission channel. Most commonly, the output is connected to a power amplifier which injects the output signal on the mains through a line−coupler.

As the NCN49597 is a half−duplex modem, this block is not active when the modem is receiving.

The transmitter block is controlled by the microcontroller core, which provided the bit sequence to be transmitted. Direct digital synthesis (DDS) is employed to synthesize the modulated signal; after a conditioning step, this signal is converted to an analogue voltage. Finally, an amplifier with variable gain buffers the signal and outputs it on pin TX_OUT.

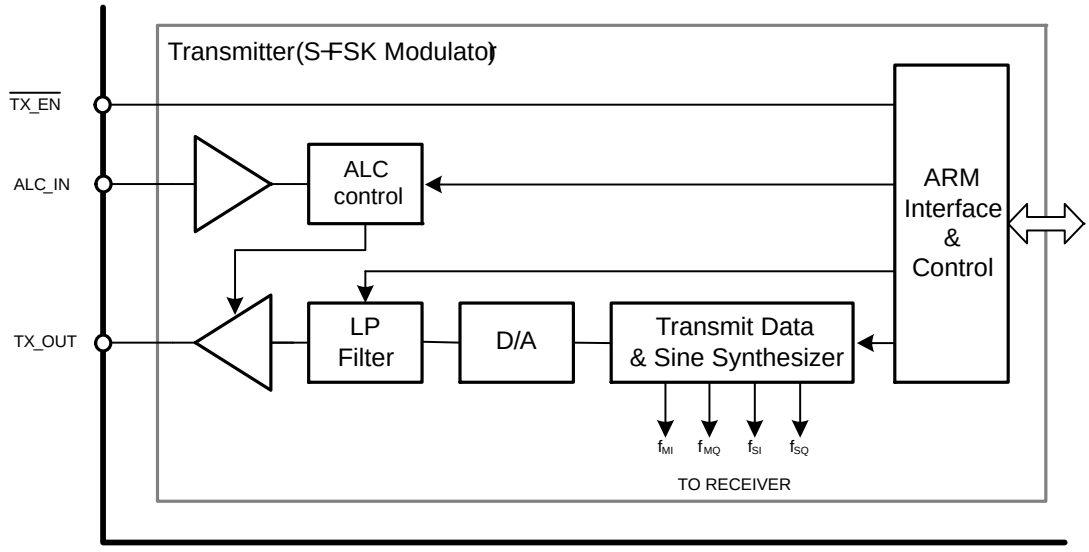

Figure 16. Transmitter Block Diagram

Microcontroller Interface & Control

The interface with the internal ARM microcontroller consists of an 8−bit data register R_TX_DATA, 2 control registers R_TX_CTRL and R_ALC_CTRL, a flag TX_RXB defining the operating mode (a high level corresponding to transmit mode; low to receive) and the frequency control registers. All these registers are memory mapped; most can be accessed through the firmware: refer to the specific firmware documentation for details.

Sine Wave Generator

The direct digital synthesizer (DDS) generates a sinusoidal signal alternating between the space frequency (f_S, data 0) and the mark frequency (f_M, data 1) as required to modulate the desired bit pattern. Two 16−bit wide frequency step registers, R_FM and R_FS, control the steps used by the DDS and thus the frequencies.

The space and mark frequency can be calculated using

$$f_S = R\_FS[15:0]\_dec \bullet f_{DDS}/2^{18}$$

$$f_M = R\_FM[15:0]\_dec \bullet f_{DDS}/2^{18}$$

Equivalently, values for R_FS[15:0] and R_FM[15:0] may be calculated from the desired carrier frequencies

$$R\_FS[15:0]\_dec = [2^{18} \bullet f_S/f_{DDS}]$$

$$R\_FM[15:0]\_dec = [2^{18} \bullet f_M/f_{DDS}]$$

With f_{DDS} = 3 MHz the direct digital synthesizer clock frequency and [*x*] equal to *x* rounded to the nearest integer.

At the start of the transmission the DDS phase accumulator starts at 0, resulting in a 0 V output level. Switching between f_M and f_S is phase−continuous. Upon switching to receive mode the DDS completes the active sine period. These precautions minimize spurious emissions.

DA Converter and Anti−aliasing Filter

A digital to analogue ΣΔ converter converts the sine wave digital word to a pulse density modulated (PDM) signal. The PDM stream is converted to an analogue signal with a first order switched capacitor filter.

A 3rd order continuous time low pass filter in the transmit path filters the quantization noise and noise generated by the ΣΔ DA converter.

The −3 dB frequency of this filter can be set to 130 kHz for applications using the CENELEC A band. In this configuration, the response of the filter is virtually flat up to 95 kHz. Alternatively a −3 dB frequency of 195 kHz can be selected yielding a flat response for the entire CENELEC A to D band (i.e., up to 148.5 kHz). Refer to the documentation of the firmware for more information.

The low pass filter is tuned automatically to compensate for process variation.

Amplifier with Automatic Level Control (ALC)

The analogue output of the low−pass filter is buffered by a variable gain amplifier; 8 attenuation steps from 0 to −21 dB (typical) with steps of 3 dB are provided.

The attenuation can be fixed by setting the bit R_ALC_CTRL[3]. The embedded microcontroller can then set the attenuation using register ALC_CTRL[2:0]. This register is usually made available by the firmware to the application microcontroller. The attenuations corresponding to R_ALC_CTRL[2:0] values are given in Table 8.

Table 8. FIXED TRANSMITTER OUTPUT ATTENUATION

ALC_CTRL[2:0]	Attenuation
000	0 dB
001	−3 dB
010	−6 dB
011	−9 dB
100	−12 dB
101	−15 dB
110	−18 dB
111	−21 dB

Alternatively, automatic level control (ALC) may be used by clearing the bit R_ALC_CTRL[3].

In this mode, the signal on the analogue input pin ALC_IN controls the transmitter output level. First, peak detection is performed. The peak value is then compared to two thresholds levels VTL_{ALC_IN} and VTH_{ALC_IN}. Depending on the value of the measured peak level on ALC_IN the attenuation is updated using

$Vp_{ALC\_IN} < VTL_{ALC}$: increase the level with one 3 dB step

$VTL_{ALC} \leq Vp_{ALC\_IN} \leq VTH_{ALC}$: do not change the attenuation

$Vp_{ALC\_IN} > VTH_{ALC}$: decrease the level with one 3 dB step

The gain changes in the next chip clock. Therefore, an evaluation phase and a level adjustment phase take two CHIP_CLK periods. ALC operation is enabled only during the first 16 CHIP_CLK cycles after switching to transmit mode.

Following reset, the level is set at minimum level (maximum attenuation). When switching to reception mode the last level is kept in memory. As a result the next transmit frame starts with the old level.

Note that the DC level on the ALC_IN pin is fixed internally to 1.65 V. As a result, a coupling capacitor is usually required.

If the automatic level control feature is not used, the pin ALC_IN may be left floating (not recommended) or tied to ground.

Transmitter Output TX_OUT

The transmitter output is DC coupled to the TX_OUT pin. Because the entire analogue part of the NCN49597 is referenced to the analogue reference voltage REF_OUT (about 1.65 V), a decoupling capacitor (C_1 in Figure 17) is usually required.

To suppress the second and third order harmonic of the generated S−FSK signal it is recommended to use a low pass filter. Figure 17 illustrates an MFB topology of a 2nd order filter.

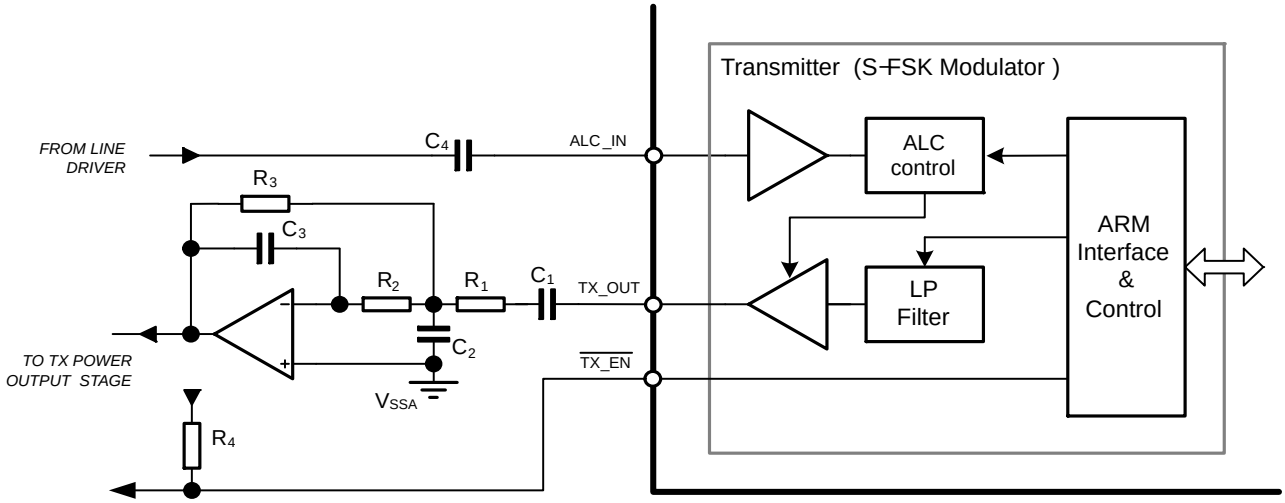

Figure 17. TX_OUT Filter

The modem indicates whether it is transmitting or receiving on the digital output pin TX_ENB. This is driven low when the transmitter is activated. The signal can be used to turn on an external line driver.

TX_ENB is a 5 V safe with open drain output; an external pull−up resistor must be added (Figure 17, R_4).

When the modem switches from transmit to receive mode, TX_ENB is kept active (i.e., low) for a short period t_{dTX_ENB} (Figure 13).

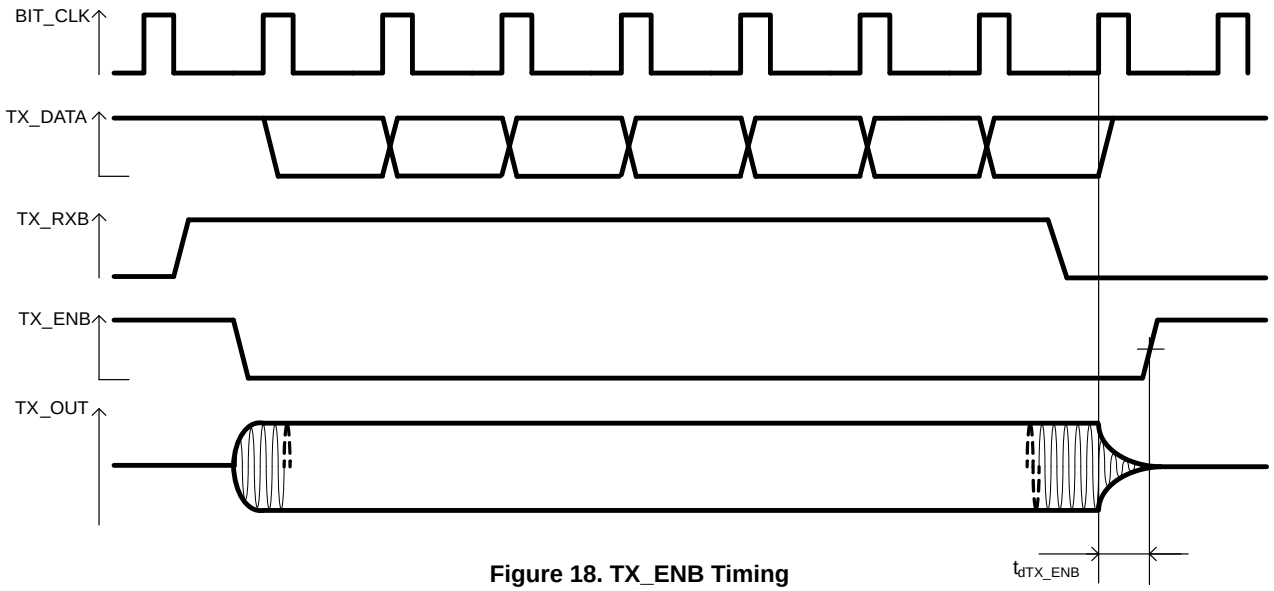

Figure 18. TX_ENB Timing

Receiver Path Description

The receiver demodulates the signal on the communication channel.

Typically, an external line coupling circuit is required to filter out the frequencies of interest on the communication channel.

The modem receiver block (Figures 19 and 22) filter, digitalizes and partially demodulates the output signal of the coupling circuit. Subsequently, the embedded microcontroller core will demodulate the resulting digital stream. The demodulation is described in the fact sheets of the various firmware solutions.

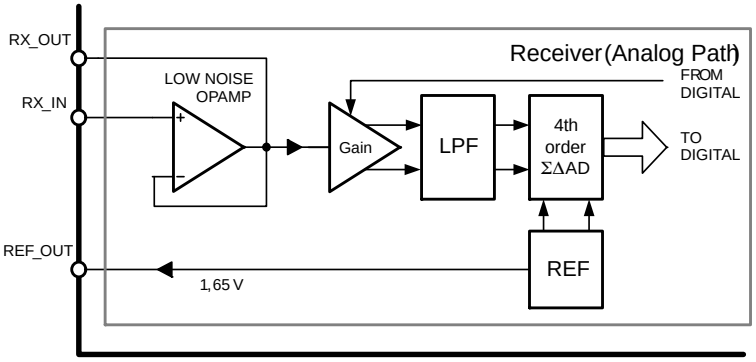

Figure 19. Analog Path of the Receiver Block

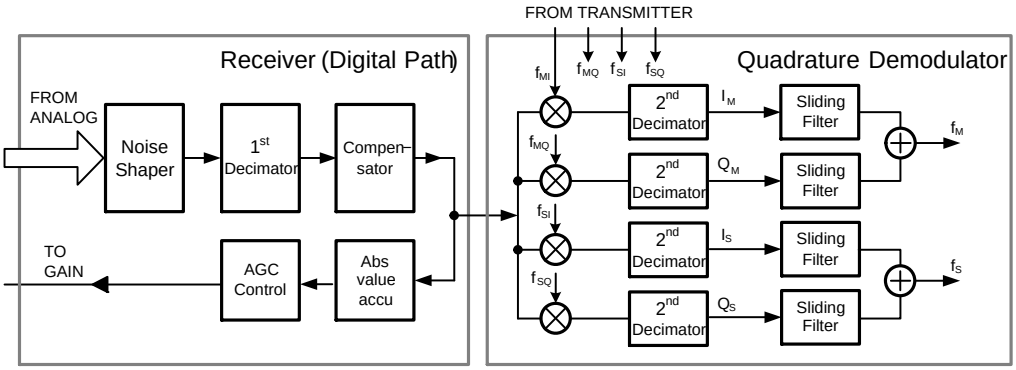

Figure 20. Digital Path of the Receiver Block

The receiver block is composed of an operation amplifier provided for filtering, a variable gain amplifier, an anti−aliasing low pass filter and analogue to digital convertor (ADC), and a digital quadrature downmixer.

When the modem is transmitting, the receive blocks are disabled to save power. The only exception is the low−pass filter, which is shared between receiver and transmitter and therefore remains active.

50/60 Hz Suppression Filter

The line coupler − external to the modem and not described in this document − couples the communication channel to the low−voltage signal input of the modem. Ideally the signal produced by the line coupler would only contain the frequency band used by the S−FSK modulation. For the common case of communication over an AC power line, a substantial 50 or 60 Hz residue is still present after the line coupler. This residue − typically much larger than the received signal − can easily overload the modem.

To improve communication performance, the NCN49597 provides a low−noise operational amplifier in a unity−gain configuration which can be used to make a 50/60 Hz suppression filter with only four external passive components. Pin RX_IN is the non−inverting input and RX_OUT is the output of the amplifier.

The internal reference voltage (described below) of 1.65 V is provided on REF_OUT and can be used for this purpose. The current drawn from this pin should be limited to 300 μA; in addition, adding a ceramic decoupling capacitor of at least 1 μF is recommended.

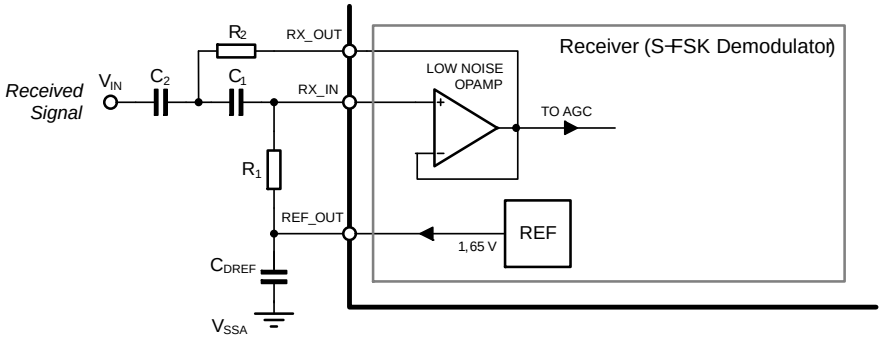

Figure 21. External Component Connection for 50/60 Hz Suppression Filter

The recommended topology is shown in Figure 20 and realizes a second order filter. The filter characteristics are determined by external capacitors and resistors. Typical values are given in Table 9 for carrier frequencies of 63.3 and 74.5 kHz; the resulting frequency response is shown in Figure 22. With a good layout, suppressing the residual mains voltage (50 or 60 Hz) with 60 dB is feasible. To design a filter for other frequencies, consult the design manual.

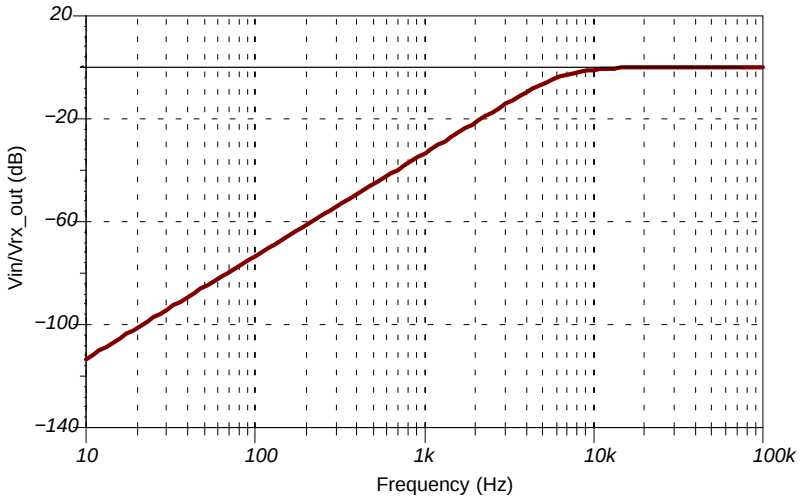

Figure 22. Transfer Function of the 50 Hz Suppression Circuit shown in Figure 17

Table 9.
VALUE OF THE RESISTORS AND CAPACITORS

Component	Value	Unit
C_1	1.5	nF
C_2	1.5	nF
C_{DREF}	1	μF
R_1	22	kΩ
R_2	11	kΩ

It is important to note that the analog part of NCN49597 is referenced to the internal analogue reference voltage REF_OUT, with a nominal value of 1.65 V. As a result, the DC voltage on pin RX_IN must be 1.65 V for optimal dynamic range. If the external signal has a substantially different reference level capacitive coupling must be used.

Automatic Gain Control (AGC)

In order to extend the range of the analogue−to−digital convertor, the receiver path contains a variable gain amplifier. The gain can be changed in 8 steps from 0 to −42 dB.

This amplifier can be used in an automatic gain control (AGC) loop. The loop is implemented in digital hardware. It measures the signal level after analogue−to−digital conversion. The amplifier gain is changed until the average digital signal is contained in a window around a percentage of the full scale. An AGC cycle takes two chip clocks: a measurement cycle at the rising edge of the CHIP_CLK and an update cycle starting at the next chip clock.

Low Noise Anti Aliasing Filter and ADC

The receiver has a 3rd order continuous time low pass filter in the signal path. This filter is in fact the same block as in the transmit path which can be shared because NCN49597 works in half duplex mode. The same choice of −3 dB frequency can be selected between 130 kHz (virtually flat up to 95 kHz) or 195 kHz (flat up to 148.5 kHz).

The output of the low pass filter is input for an analog 4th order sigma−delta converter. The DAC reference levels are supplied from the reference block. The digital output of the converter is fed into a noise shaping circuit blocking the quantization noise from the band of interest, followed by decimation and a compensation step.

Quadrature Demodulator

The quadrature demodulation block mixes the digital output of the ADC with the local oscillators. Mixing is done with the in−phase and quadrature phase of both the f_S and f_M carrier frequencies. Thus, four down−mixed (baseband) signals are obtained.

After low−pass filtering, the in−phase and quadrature components of each carrier are combined. The resulting two signals are a measure of the energy at each carrier frequency.

These energy levels are further processed in the firmware.

Communication Controller

The Communication Controller block includes the micro−processor and its peripherals (refer to Figure 23 for an overview).

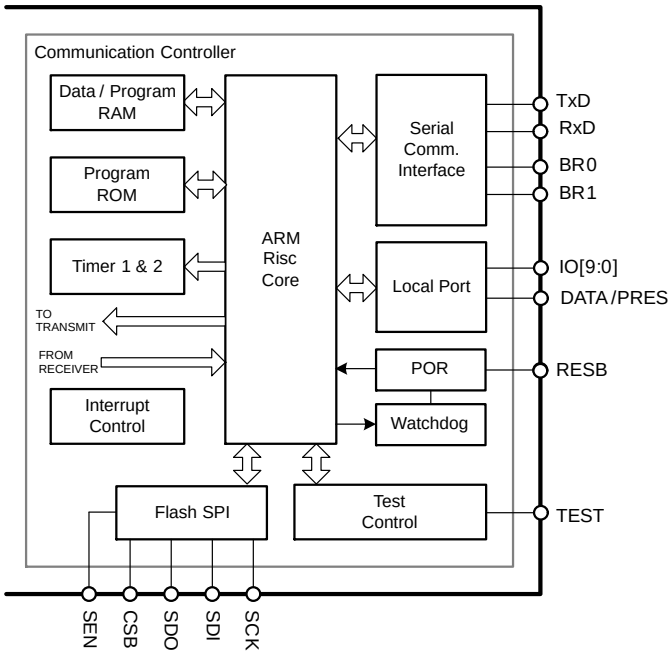

Figure 23. The Communication Controller is Based on a Standard ARM Corex M0 Core

The processor is an ARM Cortex M0 32−bit core with a reduced instruction set computer (RISC) architecture, optimized for IO handling. Most instructions complete in a single clock cycle, including byte multiplication. The peripherals include a watchdog, test and debug control, RAM, ROM containing the boot loader, UART, two timers, an SPI interface to optional external memory, I/O ports and the power−on reset. The microcontroller implements interrupts.

The 32 kB RAM contains the necessary space to store the firmware and the working data. A full−duplex serial communication block allows interfacing to the application microcontroller.

Local Port

Ten bidirectional general purpose input/output (GPIO) pins (IO0..IO9) are provided. All general purpose IO pins can be configured as an input or an output. In addition, the firmware can emulate open−drain or open−source pins. All pins are 5 V tolerant.

When the modem is booting, IO2 is configured as an input and must be pulled low to enable uploading firmware over the serial interface. At the same time, IO0 and IO1 are configured as outputs and show the status of the boot loader. A LED may be connected to IO0 to help with debugging. After the firmware has been loaded successfully, IO0..IO2 become available as normal IOs.

Typically, the firmware provides status indication on some IO pins; other IO pins remain available to the application microcontroller as IO extensions.

The application microcontroller has also low−level access to internal timing of the modem through the digital output DATA/PRES pin. The function of this pin depends on the register bit R_CONF[7].

If the bit is cleared (0), the preslot synchronization signal (PRE_SLOT) appears on the pin.

If the bit is set (1), the modem outputs the baseband, unmodulated, data. Thus, DATA/PRES is driven high when a space symbol is being transmitted (i.e., the space frequency f_S appears on pin TX_OUT); it is driven low when a mask symbol is transmitted (f_M on TX_OUT).

Testing

A JTAG debug interface is provided for development, debugging and production test. An internal pull−down resistor is provided on the input pins (TDI, TCK, TMS, and TRSTB).

In practice, the end user of the modem will not need this interface; this input pins may be tied to ground (recommended) or left floating; TDO should be left floating.

The pin TEST enables the internal hardware test mode when driven high. During normal operation, it should be tied to ground (recommended) or left floating.

Serial Communication Interface (SCI)

The Serial Communication Interface allows asynchronous communication with any device incorporating a standard Universal Asynchronous Receiver Transmitter (UART).

The serial interface is full−duplex and uses the standard NRZ format with a single start bit, eight data bits and one stop bit (Figure 24). The baud rate is programmable from 9600 to 115200 baud through the BR0 and BR1 pins.

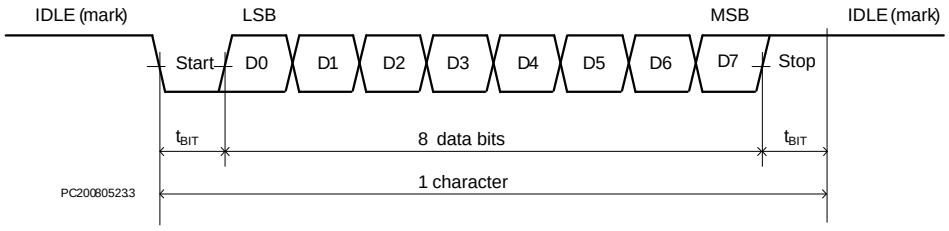

Figure 24. Data Format of the Serial Interface

Serial data is sent from the NCN49597 to the application microcontroller on pin TxD; data is received on pin RxD. Both pins are 5 V tolerant, allowing communication with both 3.3 V−and 5 V−powered devices.

On the open−drain output pin TxD an external pull−up resistor must be provided to define the logic high level (Figure 25). A value of 10 kΩ is recommended. Depending on the application, an external pull−up resistor on RxD may be required to avoid a floating input.

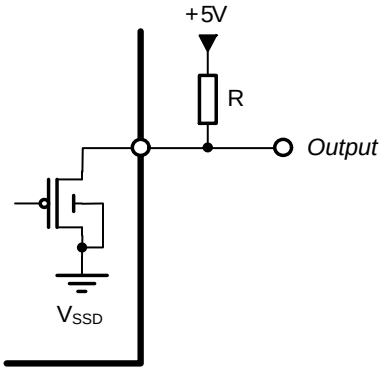

Figure 25. Interfacing to 5 V Logic using a 5 V Safe Output and a Pull−up Resistor

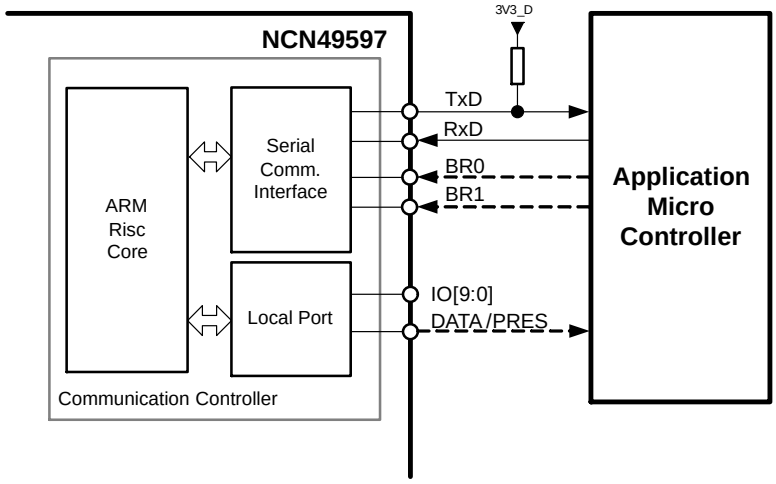

Figure 26. Connection to the Application Microcontroller

The baud rate of the serial communication is controlled by the pins BR0 and BR1. After reset, the logic level on these pins is read and latched; as a result, modification of the baud rate during operation is not possible. The baud rate derived from BR0 and BR1 is shown in Table 10.

Table 10. BR1, BR0 BAUD RATES

BR1	BR0	SCI Baud Rate
0	0	115200
0	1	9600
1	0	19200
1	1	38400

BR0 and BR1 are 5 V safe, allowing direct connection to 5 V−powered logic.

Watchdog

A watchdog supervises the ARM microcontroller. In case the firmware does not periodically signal the watchdog it is alive, it is assumed an error has occurred and a hard reset is generated.

Configuration Registers

The behavior of the modem is controlled by configuration registers. Some registers can be accessed by the user through the firmware. Table 11 gives an overview of some commonly exposed registers.

Table 11. NCN49597 CONFIGURATION REGISTERS

Register	Reset Value	Function
R_CONF[7]	0	Pin DATA/PRES mode selection
R_CONF[2:1]	00b	Baud rate selection
R_CONF[0]	0	Mains frequency
R_FS[15:0]	0000h	Step register for the space frequency fS
R_FM[15:0]	0000h	Step register for the mark frequency fM
R_ZC_ADJUST[7:0]	02h	Fine tuning of phase difference between CHIP_CLK and rising edge of mains zero crossing
R_ALC_CTRL[3]	0	Automatic level control (ALC) enable
R_ALC_CTRL[2:0]	000b	Automatic level control attenuation

Reset and Low Power

NCN49597 has two reset modes: hard reset and soft reset.

The hard reset re−initializes the complete IC (hardware and ARM) excluding the data RAM for the ARM. This guarantees correct start−up of the hardware and the microcontroller.

The modem is kept in hard reset as long as pin RESB is pulled low or the power supply $V_{DD} < V_{POR}$ (See Table 11). When switching on the power supply the output of the crystal oscillator is disabled until a few thousand clock pulses have been detected; this allows sufficient time for oscillator start−up.

When the pin RESB is pulled low the power consumption drops significantly. Power is drawn only to maintain the bias of some analogue functions and the oscillator cell.

Boot Loader

During operation, the modem firmware is stored in the internal random access memory (RAM). As this memory is volatile, the firmware must be uploaded after reset.

The NCN49597 provides two mechanisms to achieve this: the firmware may be stored in an external SPI memory or it may be uploaded over the serial communication interface.

Booting from External Memory

During reset, the boot loader module in the modem can retrieve the firmware from an attached memory.

To enable this mode, the boot control pin SEN must be driven high and IO2 must be driven low; subsequently the modem must be reset.

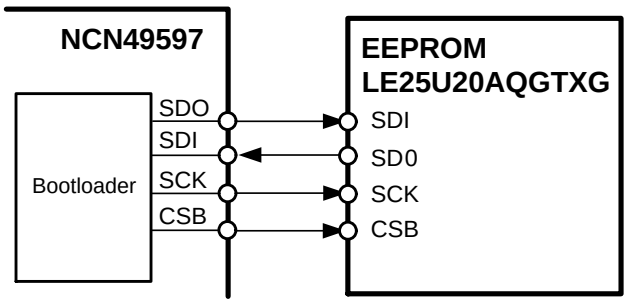

Figure 27. Connecting an External SPI Memory to the Modem

The memory must be connected to the pins of the dedicated serial peripheral interface (SPI), as shown in Figure 27. Any non−volatile memory with the standard command set and three bytes addressing is supported; is recommended.

The user must program the firmware into the external memory starting from address 0. Four bytes must be added at the end of the lowest 256−byte sector that can fit them, i.e. either the sector containing the last byte of the firmware or the next sector. These four bytes contain the checksum, the number of sectors used, and the magical numbers $A5_H$ and $5A_H$. The checksum must be computed over the entire binary.

Between the four metadata bytes and the firmware, zero−padding must be written.

This is illustrated in Table 12.

Table 12. REQUIRED CONTENTS OF AN EXTERNAL BOOTABLE SPI MEMORY FOR A BINARY FIRMWARE FILE OF LENGTH N BYTES

Address	Content
0	Firmware binary
...	
N	
N + 1	Zero padding, if required
...	
$100_H \cdot S + FB_H$	
$100_H \cdot S + FC_H$	Checksum
$100_H \cdot S + FD_H$	S, the number of sectors used
$100_H \cdot S + FE_H$	Magical number: $A5_H$
$100_H \cdot S + FF_H$	Magical number: $5A_H$
Where S is the numbers of sectors used: $S = \left\lfloor \frac{N + 4}{100_H} \right\rfloor$	

The tool PlcEepromGenerator.exe, provided by ON Semiconductor, may be used to convert a binary firmware file into a file that follows these requirements. The latter can be written directly in the external memory.

As an example, if the firmware binary size is 618 bytes, the first two 256−byte sector will be filled completely. The last 106 bytes of the firmware binary will be written to the third sector, followed by zero padding (256 − 106 − 4 = 146 bytes), followed by four bytes: checksum, 03_H, $A5_H$ and $5A_H$.

Once the boot loader has finished copying the firmware to the internal memory, the checksum is calculated and compared to the stored checksum. If both match, the processor is released from reset and the firmware starts executing. IO2 subsequently becomes available as a normal GPIO.

Firmware Upload over the Serial Communication Interface

During reset, the boot loader module in the modem can receive the firmware over the serial interface.

To enable this mode, the IO2 and the boot control pin SEN must be driven low; subsequently the modem must be reset. IO2 must remain low during the entire boot process; if driven high during boot the boot loader terminates immediately. To restart the boot loader, reset the modem.

As soon as the reset of the modem is released, the boot loader process starts. When it is ready to receive the firmware from the external microcontroller, the boot loader will send a 02_H (STX) byte.

Upon receiving this byte the user must send the byte sequence specified in Table 13. The sequence contains a checksum to verify correctness of the received binary image. The CRC must be calculated over the firmware binary only (excluding the magical number and the size). The program crc.exe, provided by ON Semiconductor, can be used for this calculation.

Table 13. BYTE SEQUENCE to be transmitted by the application microcontroller during firmware upload

Value	Description
[CE_H]	Should only be sent to restart the boot loader process, in response to a NAK character received from the modem
AA_H	Magical number
Size (LSB)	The size of the entire firmware binary, including the four bytes for the CRC at the end
Size (MSB)	
Binary, first byte	Contents of the firmware binary
...	
Binary, last byte	
CRC (LSB)	CRC, as calculated on the binary only
CRC (MSB)	

Data transmission must start only after receiving the STX byte. In addition, the first byte must be sent within 350 ms. If these timing constraints are not satisfied the boot loader will send a 15_H (NAK) character and will reject any data received until the application microprocessor stops sending bytes for at least 100 ms. The pause will restart the boot loader, and a new STX character will be sent to the application microcontroller to indicate this.

Once transmission has started, the maximal delay between consecutive bytes is 20 ms. If this timing constraints is not met, or if the checksum is incorrect, the boot loader will send a 15_H (NAK) character. This error also occurs when the user attempts to upload a binary exceeding the maximal size of $7F00_H$ (32512) bytes. When the application microcontroller receives this NAK, it should transmit a CE_H (mnemonic for “clear error”) byte. This informs the boot loader that the application microcontroller understood the problem. Following the CE_H byte, the microcontroller may restart.

The timing constraints are illustrated in Figure 3.

Application Information

For a system−level overview of power line communication, refer to [4]. For more information on how to design with the NCN49597 modem, refer to the design manual available from your sales representative [1]. This section gives a few hints.

Supplies and Decoupling

For optimal stability and noise rejection, all power supplies must be decoupled as physically close to the device as possible.

The analogue and digital blocks are powered through independent power supply pins (VDDA resp. VDD); the nominal supply voltage is 3.3 V. On both pins, decoupling must be provided with at least a ceramic capacitor of 100 nF between the pin and the corresponding ground (VSSA resp. VSS). The connection path of these capacitors on the printed circuit board (PCB) should be kept as short as possible in order to minimize the parasitic inductance.

It is recommended to tie both analogue and digital ground pins to a single, uninterrupted ground plane.

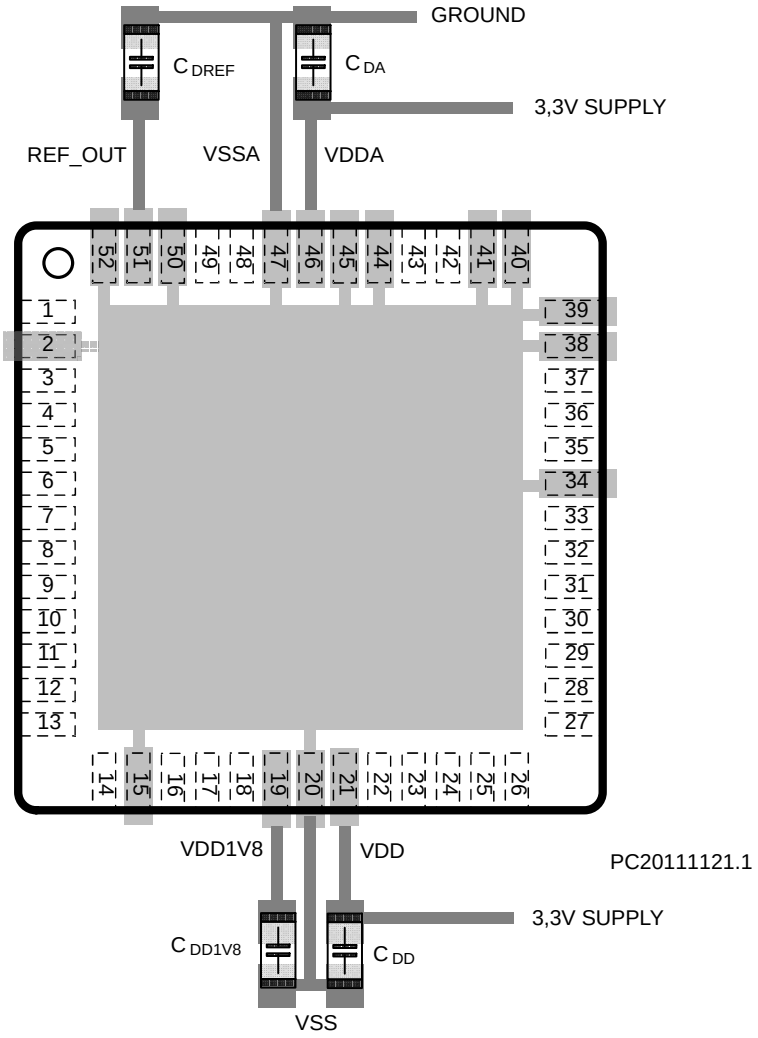

Figure 28. Recommended Layout of the Placement of Decoupling Capacitors (bottom ground plane not shown)

Internal Voltage Reference

REF_OUT is the analog output pin which provides the voltage reference used by the A/D converter. This pin must be decoupled to the analog ground by a 1 μF ceramic capacitance C_{DREF}. The connection path of this capacitor to the VSSA on the PCB should be kept as short as possible in order to minimize the serial inductance.

Internal Voltage Regulator

An internal linear regulator provides the 1.8 V core voltage for the microcontroller. This voltage is connected to pin VDD1V8. A ceramic decoupling capacitor of 1 μF to ground must be connected as close as possible to this pin (Figure 28).

The internal regulator should not be used to power other components.

References

In this document references are made to:

1. ON Semiconductor, *Design Manual NCN495979/9*, 2016−08−23. The latest version is available from your sales representative.
2. CENELEC. EN 50065−1: *Signaling on low−voltage electrical installations in the frequency range 3 kHz to 148,5 kHz*. 2011−04−22. Online at http://www.cenelec.eu/dyn/www/f?p=104:110:1022556227334229::::FSP_ORG_ID,FSP_PROJECT,FSP_LANG_ID:821,22484,25
3. ON Semiconductor. *Mains synchronization for PLC modems (application note)*. 2015−08−19. The latest version is available from your sales representative.
4. ON Semiconductor. AND9165/D. Getting started with power line communication (application note). 2016−05−01. Online at http://www.onsemi.com/pub_link/Collateral/AND9165−D.PDF

Table 14. ORDERING INFORMATION

Part Number	Temperature Range	Package Type	Shipping†
NCN49597MNG	−40°C – 125°C	QFN−52 (Pb−Free)	Tube
NCN49597MNRG	−40°C – 125°C	QFN−52 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

QFN52 8x8, 0.5P
CASE 485M−01
ISSUE C

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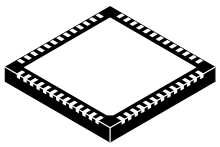
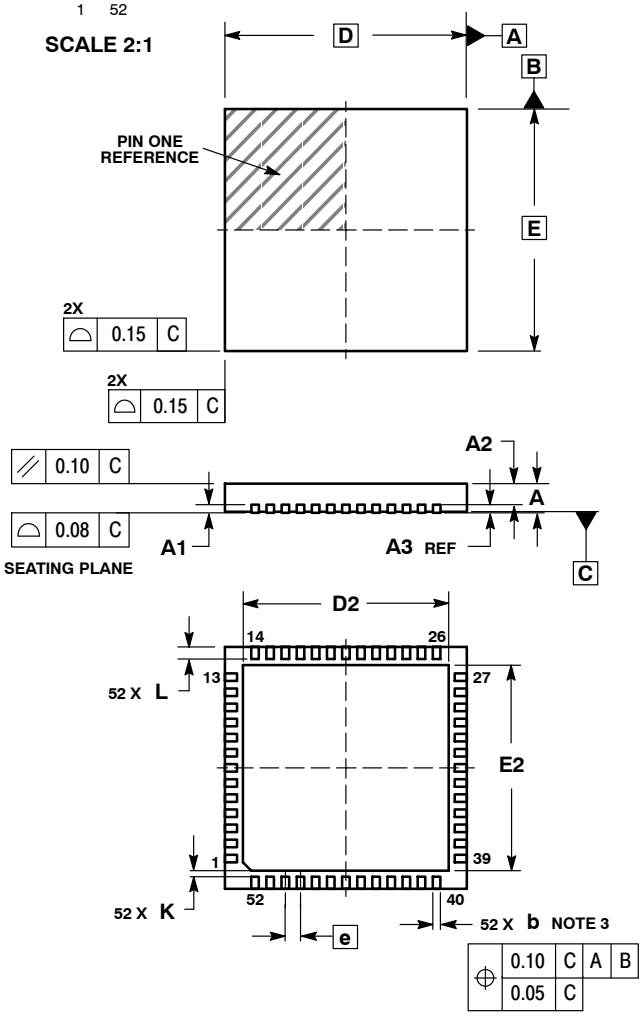


SCALE 2:1



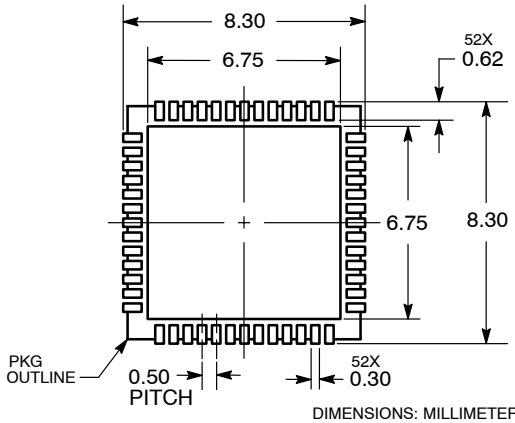
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

GENERIC MARKING DIAGRAM

XXXXXXXXX	= Device Code
A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

RECOMMENDED SOLDERING FOOTPRINT



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