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NCP1351

Variable Off Time PWM Controller

The NCP1351 is a current−mode controller targeting low power off−line flyback Switched Mode Power Supplies (SMPS) where cost is of utmost importance. Based on a fixed peak current technique (quasi−fixed T_{ON}), the controller decreases its switching frequency as the load becomes lighter. As a result, a power supply using the NCP1351 naturally offers excellent no−load power consumption, while optimizing the efficiency in other loading conditions. When the frequency decreases, the peak current is gradually reduced down to approximately 30% of the maximum peak current to prevent transformer mechanical resonance. The risk of acoustic noise is thus greatly diminished while keeping good standby power performance.

An externally adjustable timer permanently monitors the feedback activity and protects the supply in presence of a short−circuit or an overload. Once the timer elapses, NCP1351 stops switching and stays latched for version A, and tries to restart for version B.

Versions C and D include a dual overcurrent protection trip point, allowing the implementation of the controller in peak−power requirements applications such as printers and so on. When the fault is acknowledged, C version latches−off whereas D version auto−recovers.

The internal structure features an optimized arrangement which allows one of the lowest available startup current, a fundamental parameter when designing low standby power supplies.

The negative current sensing technique minimizes the impact of the switching noise on the controller operation and offers the user to select the maximum peak voltage across his current sense resistor. Its power dissipation can thus be application optimized.

Finally, the bulk input ripple ensures a natural frequency smearing which smooths the EMI signature.

Features

- Quasi−fixed T_{ON}, Variable T_{OFF} Current Mode Control
- Extremely Low Current Consumption at Startup
- Peak Current Compression Reduces Transformer Noise
- Primary or Secondary Side Regulation
- Dedicated Latch Input for OTP, OVP
- Programmable Current Sense Resistor Peak Voltage
- Natural Frequency Dithering for Improved EMI Signature
- Easy External Over Power Protection (OPP)
- Undervoltage Lockout
- Very Low Standby Power via Off−time Expansion
- SOIC−8 Package
- Standard Overcurrent Protection, Latched or Auto−Recovery, A & B Versions
- Dual Trip Point Overcurrent Protection, Latched or Auto−Recovery, C & D Versions
- These are Pb−Free Devices

Typical Applications

- Auxiliary Power Supply
- Printer, Game Stations, Low−Cost Adapters
- Off−line Battery Charger

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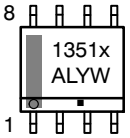
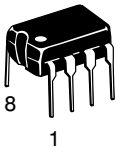
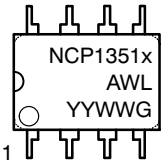
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751





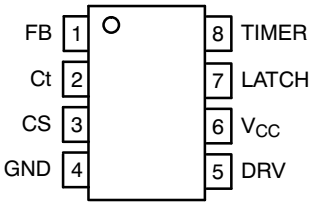
PDIP−8
P SUFFIX
CASE 626



x = A, B, C, or D Options
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
▪ or G = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

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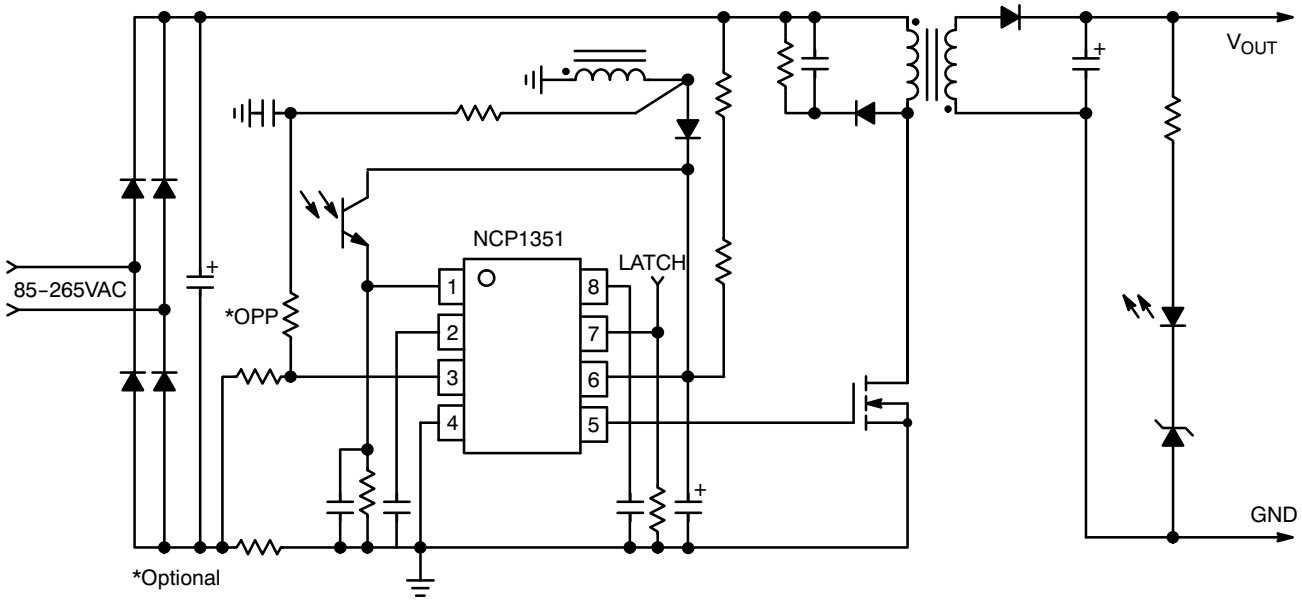


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	FB	Feedback Input	Injecting Current in this Pin Reduces Frequency
2	Ct	Oscillator Frequency	A capacitor sets the maximum switching frequency at no feedback current
3	CS	Current Sense Input	Senses the Primary Current
4	GND	–	–
5	DRV	Driver Output	Driving Pulses to the Power MOSFET
6	V_{CC}	Supply Input	Supplies the controller up to 28 V
7	Latch	Latchoff Input	A positive voltage above V_{LATCH} fully latches off the controller
8	Timer	Fault Timer Capacitor	Sets the time duration before fault validation

OVERCURRENT PROTECTION ON NCP1351 VERSIONS:

NCP1351	Auto−recovery	Latched	Dual level
A		x	
B	x		
C		x	x
D	x		x

INTERNAL CIRCUIT ARCHITECTURE

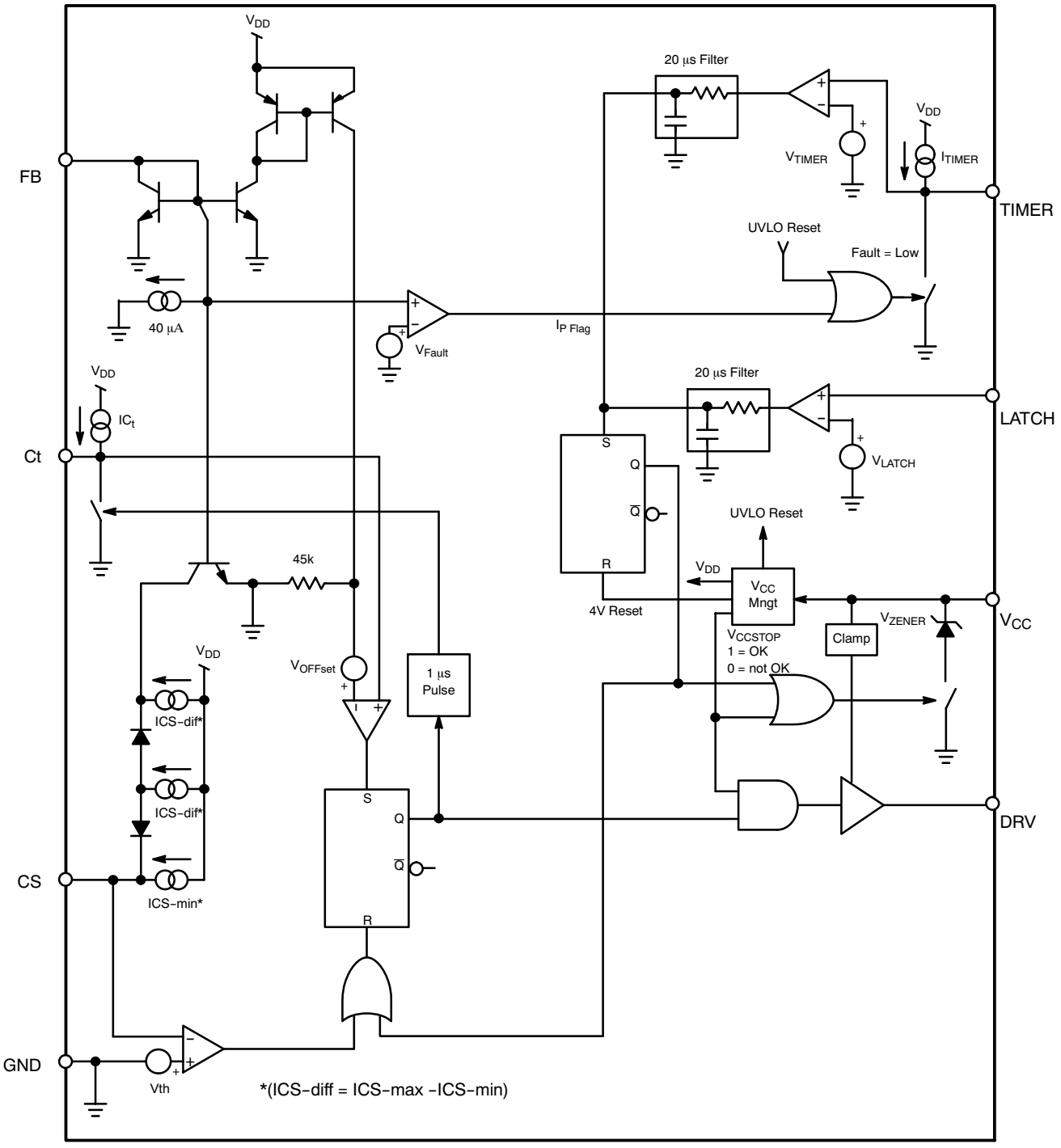


Figure 2. A Version (Latched Short−Circuit Protection)

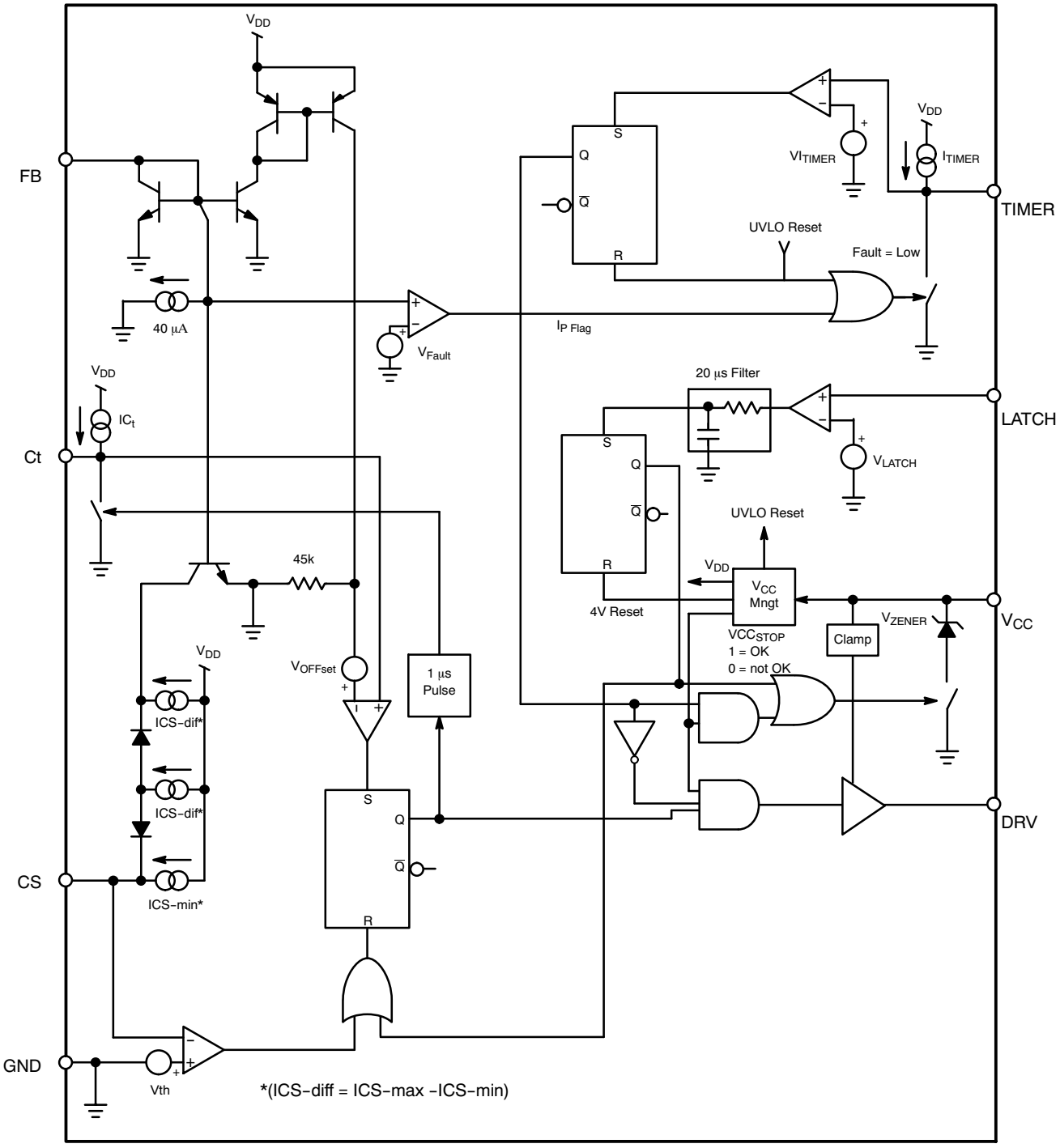


Figure 3. B Version (Auto−recovery Short−Circuit Protection)

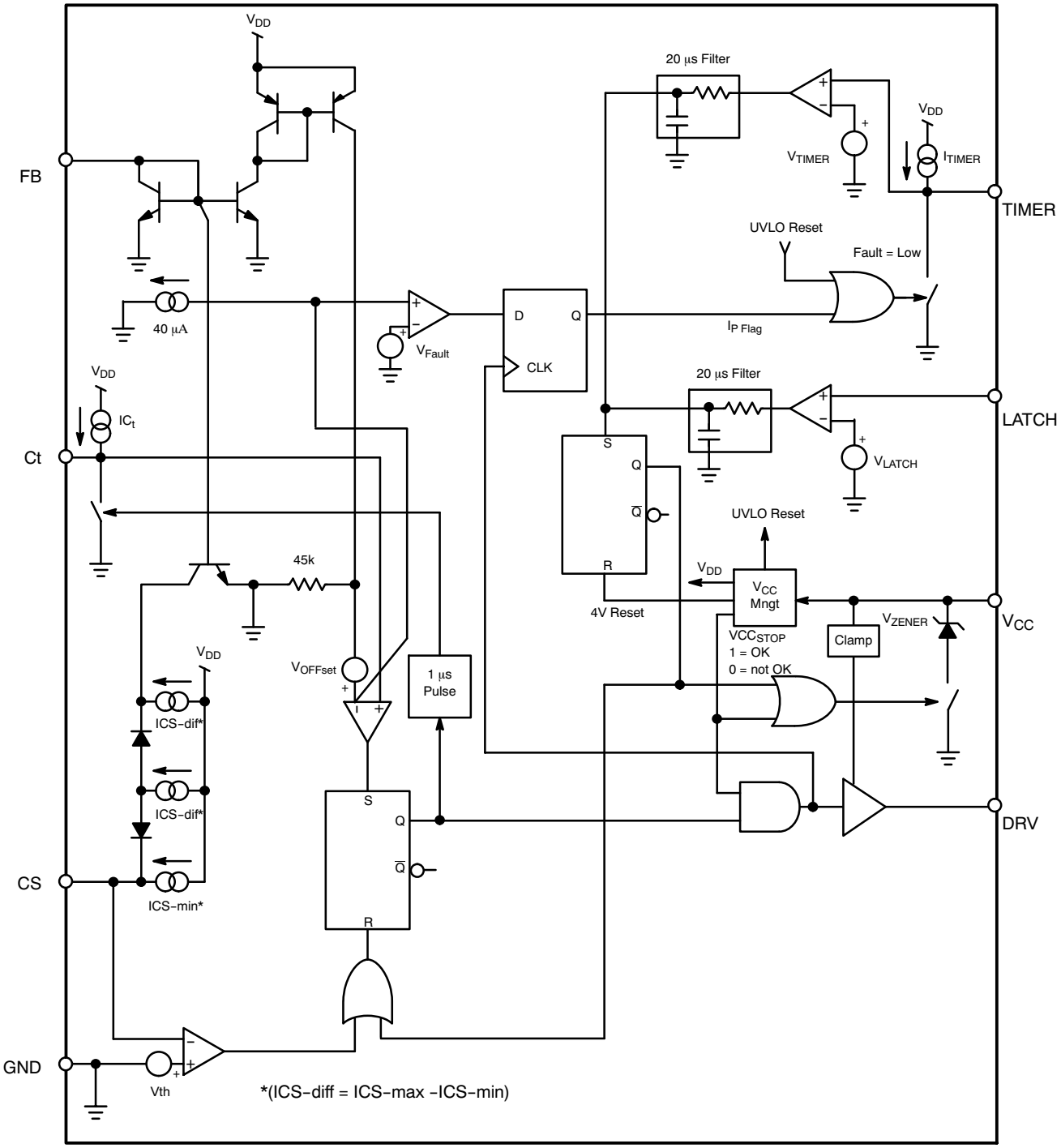


Figure 4. C Version (Latched Short−Circuit Protection)

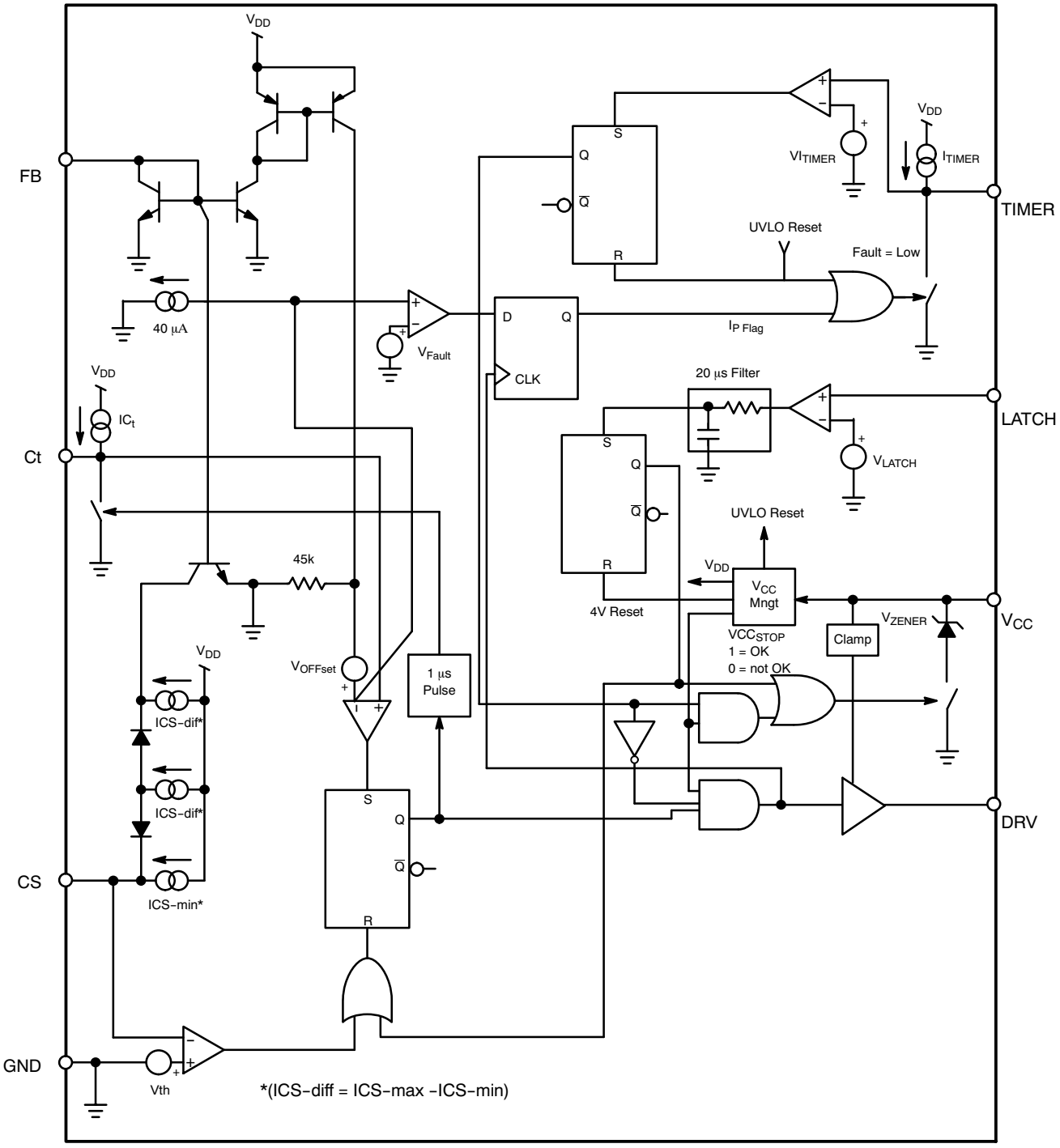


Figure 5. D Version (Auto−recovery Short−Circuit Protection)

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{SUPPLY}	Maximum Supply on V_{CC} Pin 6	−0.3 to 28	V
I_{SUPPLY}	Maximum Current in V_{CC} Pin 6	20	mA
V_{DRV}	Maximum Voltage on DRV Pin 5	−0.3 to 20	V
I_{DRV}	Maximum Current in DRV Pin 5	±400	mA
V_{MAX}	Supply Voltage on all pins, except Pin 6 (V_{CC}), Pin 5 (DRV)	−0.3 to 10	V
I_{MAX}	Maximum Current in all Pins Except Pin 6 (V_{CC}) and Pin 5 (DRV)	±10	mA
I_{FBmax}	Maximum Injected Current in Pin 1 (FB)	0.5	mA
R_{Gmin}	Minimum Resistive Load on DRV Pin	33	kΩ
$R_{\theta JA}$	Thermal Resistance Junction−to−Air PDIP−8 SOIC−8	142 176	°C/W
T_{JMAX}	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model V per Mil−STD−883, Method 3015	2	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

Electrical Characteristics (For typical values T_J = 25°C, for Min/Max Values T_J = −25°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
VCC_{ON}	V_{CC} Increasing Level at Which Driving Pulses are Authorized	6	15	18	22	V
VCC_{STOP}	V_{CC} Decreasing Level at Which Driving Pulses are Stopped	6	8.3	8.9	9.5	V
VCC_{HYST}	Hysteresis VCC_{ON} − VCC_{STOP}	6	6	–	–	V
V_{ZENER}	Clamped V_{CC} When Latched Off	6	–	6	–	V
ICC1	Startup Current	6	–	–	10	μA
ICC2	Internal IC Consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 0	6	–	1.0	1.8	mA
ICC3	Internal IC Consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 1 nF	6	–	1.6	2.5	mA
ICC4	Internal IC Consumption in Auto−Recovery Latch−off Phase	6	–	600	–	μA
ICC_{LATCH}	Current Flowing into V_{CC} pin that Keeps the Controller Latched	6	20	–	–	μA
CURRENT SENSE						
I_{CSmin}	Minimum Source Current (I_{FB} = 90 μA) T_J = 0°C to +125°C	3	61	70	75	μA
I_{CSmin}	Minimum Source Current (I_{FB} = 90 μA) T_J = −25°C to +125°C	3	58	70	75	μA
I_{CSmax}	Maximum Source Current (I_{FB} = 50 μA) T_J = 0°C to +125°C	3	251	270	289	μA
I_{CSmax}	Maximum Source Current (I_{FB} = 50 μA) T_J = −25°C to +125°C	3	242	270	289	μA
V_{TH}	Current Sense Comparator Threshold Voltage	3	10	20	35	mV
t_{delay}	Propagation Time Delay (CS Falling Edge to Gate Output)	3	–	160	300	ns
TIMING CAPACITOR						
V_{OFFSET}	Minimum Voltage on C_T Capacitor, I_{FB} = 30 μA	2	475	510	565	mV
VCT_{MAX}	Voltage on C_T Capacitor at I_{FB} = 150 μA	2	5	–	–	V
I_{CT}	Source Current (Ct Pin Grounded) T_J = 25°C T_J = −25°C to +125°C	2	9.8 9.3	10.8 10.8	11.8 11.9	μA
VCT_{MIN}	Minimum Voltage on C_T, Discharge Switch Activated	2	–	–	20	mV
T_{DISCH}	C_T Capacitor Discharge Time (Activated at DRV Turn−on)	2		1		μs
V_{FAULT}	C_T Capacitor Level at Which Fault Timer Starts A and B Versions C and D Version	2	0.4 –	0.5 0.96	0.6 –	V
K_{FAULT}	Factor Linking V_{OFFSET} and V_{FAULT} (Note 1) C and D Version	–	1.67	1.86	2.05	
FEEDBACK SECTION						
V_{FB}	FB Pin Voltage for an Injected Current of 200 μA	1	–	0.7	–	V
I_{FAULT}	FB Current Under Which a Fault is Detected A and B Versions C and D Versions	1	– –	40 51	– –	μA
I_{FBcomp}	FB Current at Which CS Compression Starts	1	–	60	–	μA
I_{FBred}	FB Current at Which CS Compression is Finished	1	–	80	–	μA
DRIVE OUTPUT						
T_r	Output Voltage Rise−time @ CL = 1 nF, 10 − 90% of Output Signal	5	–	90	–	ns
T_f	Output Voltage Fall−time @ CL = 1 nF, 10 − 90% of Output Signal	5	–	100	–	ns
R_{OH}	Source Resistance	5	–	80	–	Ω
R_{OL}	Sink Resistance	5	–	30	–	Ω
V_{DRVlow}	DRV Pin Level at V_{CC} Close to VCC_{STOP} with a 33 kΩ Resistor to GND	5	8.0	–	–	V
$V_{DRVhigh}$	DRV Pin Level at V_{CC} = 28 V with 33 kΩ Resistor to GND	5	15	17	20	V
Protection						
I_{TIMER}	Timing Capacitor Charging Current	8	10	11.5	13	μA
V_{TIMER}	Fault Voltage on Pin 8	8	4.5	5	5.5	V
T_{TIMER}	Fault Timer Duration, C_{TIMER} = 100 nF	–	–	42	–	ms
V_{LATCH}	Latching Voltage	7	4.5	5	5.5	V

1. Guaranteed by design.

The NCP1351 implements a fixed peak current mode technique whose regulation scheme implements a variable switching frequency. As shown on the typical application diagram, the controller is designed to operate with a minimum number of external components. It incorporates the following features:

- **Frequency Foldback:** Since the switching period increases when power demand decreases, the switching frequency naturally diminishes in light load conditions. This helps to minimize switching losses and offers good standby power performance.
- **Very Low Startup Current:** The patented internal supply block is specially designed to offer a very low current consumption during startup. It allows the use of a very high value external startup resistor, greatly reducing dissipation, improving efficiency and minimizing standby power consumption.
- **Natural Frequency Dithering:** The quasi−fixed t_{ON} mode of operation improves the EMI signature since the switching frequency varies with the natural bulk ripple voltage.
- **Peak Current Compression:** As the load becomes lighter, the frequency decreases and can enter the audible range. To avoid exciting transformer mechanical resonances, hence generating acoustic noise, the NCP1351 includes a patented technique, which reduces the peak current as power goes down. As such, inexpensive transformer can be used without having noise problems.
- **Negative Primary Current Sensing:** By sensing the total current, this technique does not modify the MOSFET driving voltage (V_{GS}) while switching. Furthermore, the programming resistor, together with the pin capacitance, forms a residual noise filter which blanks spurious spikes.
- **Programmable Primary Current Sense***:* It offers a second peak current adjustment variable, which improves the design flexibility.
- **Extended V_{CC} Range:** By accepting V_{CC} levels up to 28 V, the device offers added flexibility in presence of loosely coupled transformers. The gate drive is safely clamped below 20 V to avoid stressing the driven MOSFET.
- **Easy OPP:** Connecting a resistor from the CS pin to the auxiliary winding allows easy bulk voltage compensation.
- **Secondary or Primary Regulation:** The feedback loop arrangement allows simple secondary or primary side regulation without significant additional external components.
- **Latch Input:** If voltage on Pin 7 is externally brought above 5 V, the controller permanently latches off and stays latched until the user cycles V_{CC} down, below 4 V typically.
- **Fault Timer:** In presence of badly coupled transformer, it can be quite difficult to detect an overload or a short−circuit on the primary side. When the feedback current disappears, a current source charges a capacitor connected to Pin 8. When the voltage on this pin reaches a certain level, all pulses are shut off and the V_{CC} voltage is pulled down below the $VCC_{(min)}$ level. This protection is latched on the A version (the controller must be shut down and restart to resume normal operation), and auto−recovery on Version B (if the fault goes away, the controller automatically resumes operation).
- **Dual Trip Point:** in some applications, such as printer power supplies, it is necessary to let the power supply deliver more power on a transient event. If the event lasts longer than what the fault timer authorizes, then the NCP1351 either latches−off (C Version) or enters an auto−recovery mode (D Version). The level at which the timer starts is internally set to 55% of the maximum power capability.

APPLICATION INFORMATION

The Negative Sensing Technique

Standard current−mode controllers use the positive sensing technique as portrayed by Figure 6. In this technique, the controller detects a positive voltage drop across the sense resistor, representative of the flowing current. Unfortunately, this solution suffers from the following drawbacks:

1. Difficulties to precisely adjust the peak current. If 1 V is the maximum sense level, you must combine low valued resistors to reach the exact limit you need.
2. The voltage developed across the sense resistor subtracts from the gate voltage. If your $VCC_{(min)}$ is 7 V, then the actual gate voltage at the end of the on time, assuming a full load condition, is 7 V – 1 V = 6 V.
3. The current in the sense resistor also includes the C_{iss} current at turn−on. This narrow spike often disturbs the controller and requires adequate treatment through a LEB circuitry for instance.

Figure 7 represents the negative current sense technique. In this simplified example, the source directly connects to the controller ground. Hence, if V_{CC} is 8 V, the effective gate−source voltage is very close to 8 V: no sense resistor drop. How does the controller detect a negative excursion? In lack of primary current, the voltage on the CS pin reaches R_{offset} x I_{CS}. Let us assume that these elements lead to have 1 V on this pin. Now, when the power MOSFET activates, the current flows via the sense resistor and develop a negative voltage by respect to the controller ground. The voltage seen on the CS is nothing else than a positive voltage (R_{offset} x I_{CS}) plus the voltage across the sense resistor which is negative. Thus, the CS pin voltage goes low as the primary current increases. When the result reaches the threshold voltage (around 20 mV), the comparator toggles and resets the main latch. Figure 3 details how the voltage moves on the CS pin on a 1351 demoboard, whereas Figure 9 zooms on the sense resistor voltage captured by respect to the controller ground.

The choice of these two elements is simple. Suppose you want to develop 1 V across the sense resistor. You would select the offset resistor via the following formula:

$$R_{offset} = \frac{1}{I_{CS}} = \frac{1}{270\ \mu} = 3.7\ k\Omega \qquad \text{(eq. 1)}$$

If you need a peak current of 2 A, then, simply apply the ohm law to obtain the sense resistor value:

$$R_{sense} = \frac{1}{I_{peak\_max}} = \frac{1}{2} = 0.5\ \Omega \qquad \text{(eq. 2)}$$

Due to the circuit flexibility, suppose you only have access to a 0.33 Ω resistor. In that case, the peak current will exceed the 2 A limit. Why not changing the offset resistor value then? To obtain 2 A from the 0.33 Ω resistor, you should develop:

The offset resistor is thus derived by:

$$V_{sense} = R_{sense} I_{peak\_max} = 0.33 \times 2 = 660\ mV \qquad \text{(eq. 3)}$$

$$R_{offset} = \frac{0.66}{I_{CS}} = \frac{0.66}{270\ \mu} = 2.44\ k\Omega \qquad \text{(eq. 4)}$$

If reducing the sense resistor is of good practice to improve the efficiency, we recommend to adopt sense values between 0.5 V and 1 V. Reducing the voltage below these levels will degrade the noise immunity.

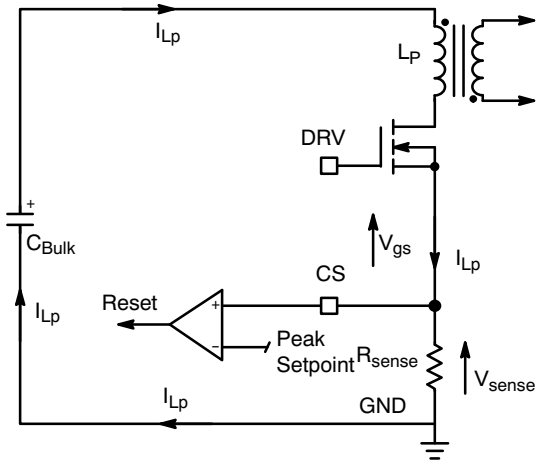


Figure 6. Positive Current−Sense Technique

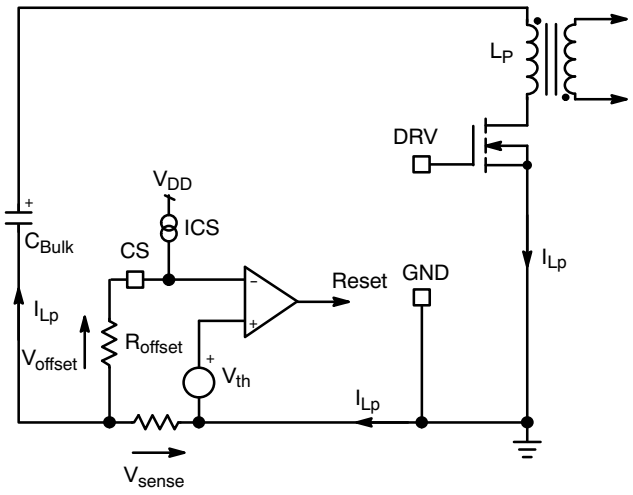


Figure 7. A Simplified Circuit of the Negative Sense Implementation

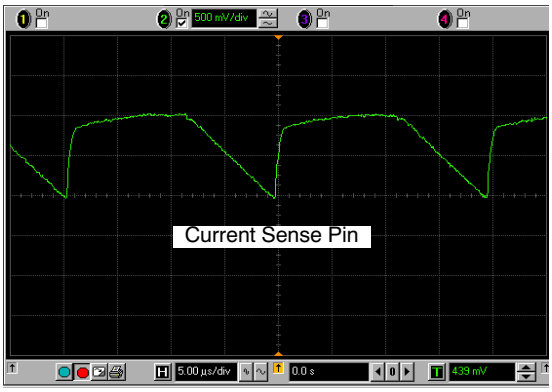


Figure 8. The Voltage on the Current Sense Pin

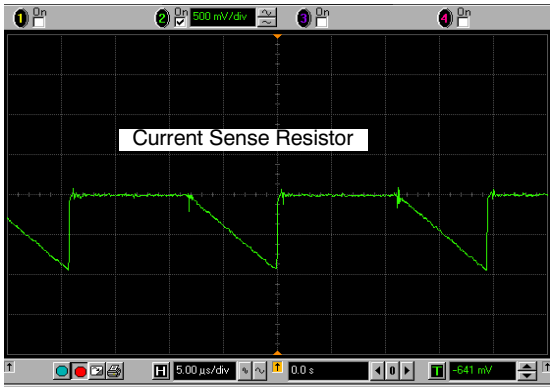


Figure 9. The Voltage Across the Sense Resistor

Below are a few recommendations concerning the wiring and the PCB layout:

- A small 22 pF capacitor can be placed between the CS pin and the controller ground. Place it as close as possible to the controller.
- Do not place the offset resistor in the vicinity of the sense element, but put it close to the controller as well.
- Regulation by frequency
- The power a flyback converter can deliver relates to the energy stored in the primary inductance L_p and obeys the following formulae:

$$P_{out\_DCM} = \frac{1}{2} L_P I_{peak}^2 F_{SW} \eta \quad \text{(eq. 5)}$$

$$P_{out\_CCM} = {}^1{}_2 L_P (I_{peak}^2 - I_{valley}^2) F_{SW} \eta \quad \text{(eq. 6)}$$

Where:

η (eta) is the converter efficiency

I_{peak} is the peak inductor current reached at the on time termination

I_{valley} represents the current at the end of the off time. It equals zero in DCM.

F_{SW} is the operating frequency.

Thus, to control the delivered power, we can either play on the peak current setpoint (classical peak current mode control) or adjust the switching frequency by keeping the peak current constant. We have chosen the second scheme in this NCP1351 for simplicity and ease of implementation. Thus, once the peak current has been selected, the feedback loop automatically reacts to satisfy Equations 5 and 6. The external capacitor that you connect between pin 2 and ground (again, place it close to the controller pins) sets the maximum frequency you authorize the converter to operate up to. Normalized values for this timing capacitor are 270 pF (65 kHz) and 180 pF (100 kHz). Of course, different combinations can be tried to design at higher or lower frequencies. Please note that changing the capacitor value does not affect the operating frequency at nominal line and load conditions. Again, the operating frequency is selected by the feedback loop to cope with Equations 5 and 6 definitions.

The feedback current controls the frequency by changing the timing capacitor end of charge voltage, as illustrated by Figure 10.

The timing capacitor ending voltage can be precisely computed using the following formula:

$$V_{C_t} = 45\ k\ (I_{FB} - 40u) + 500m \quad \text{(eq. 7)}$$

Where I_{FB} represents the injected current inside the FB pin (pin 1). The 40u term corresponds to a 40 μA offset current purposely placed to force a minimum current injection when the loop is closed. This allows the controller to detect a short−circuit condition as the feedback current drops to zero in that condition.

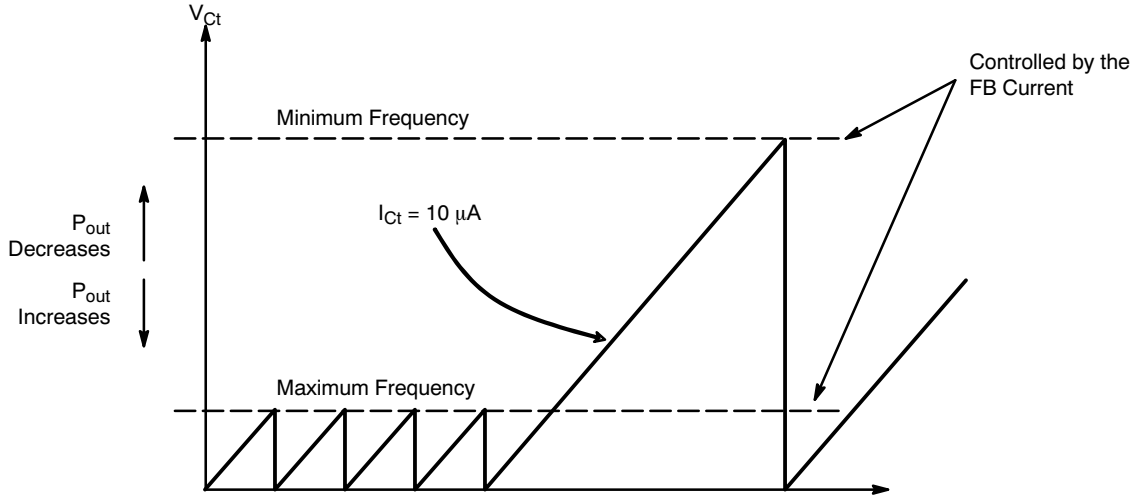


Figure 10. The Current Injected into the Feedback Loop Adjusts the Switching Frequency

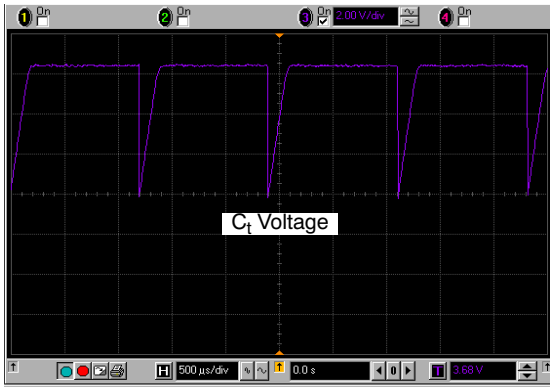


Figure 11. In Light Load Conditions, the Oscillator Further Delays the Restart Time

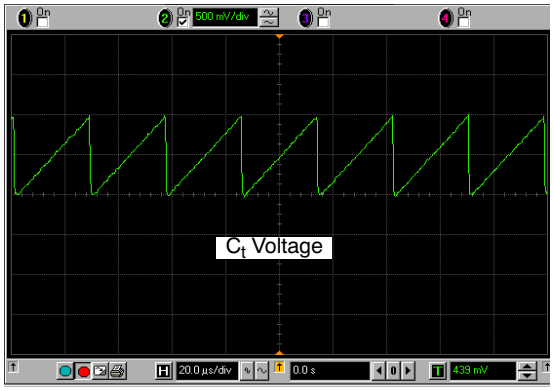


Figure 12. C_t Voltage Swing at a Moderate Loading

In light load conditions, the frequency can go down to a few hundred Hz without any problem. The internal circuitry naturally blocks the oscillator and softly shifts the restart time as shown on Figure 11 scope shot.

Delays The Restart Time

In lack of feedback current, for instance during a startup sequence or a short circuit, the oscillator frequency is pushed to the limit set by the timing capacitor. In this case, the lower threshold imposed to the timing capacitor is blocked to 500 mV (parameter V_{fault}). This is the maximum power the converter can deliver. To the opposite, as you inject current via the optocoupler in the feedback pin, the off time expands and the power delivery reduces. The maximum threshold level in standby conditions is set to 6 V.

Over Power Protection

As any universal−mains operated converters, the output power slightly increases at high line compared to what the power supply can deliver at low line. This discrepancy relates to the propagation delay from the point where the peak is detected to the MOSFET gate effective pulldown. It naturally includes the controller reaction time, but also the driver capability to pull the gate down. If the MOSFET Q_g is too large, then this parameter will greatly affect your overpower parameter. Sometimes, the small PNP can help and we recommend it if you use a large Q_g MOSFET:

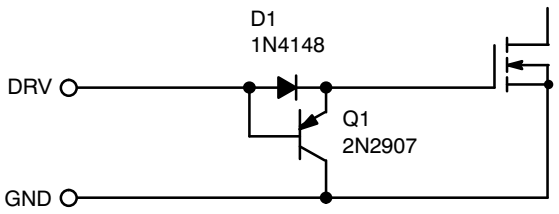


Figure 13. A Low−Cost PNP Improves the Drive Capability at Turn−off

Over power protection can be done without power dissipation penalty by arranging components around the auxiliary as suggested by Figure 14. On this schematic, the diode anode swings negative during the on time. This negative level directly depends on the input voltage and offsets the current sense pin via the R_{OPP} resistor. A small integration is necessary to reduce the O_{PP} action in light load conditions. However, depending on the compensation level, the standby power can be affected. Again, the resistor R_{OPP} should be placed as close as possible to the CS pin. The 22 pF can help to circumvent any picked−up noise and D_2 prevents the positive loading of the 270 pF capacitor during the flyback swing. We have put a typical 100 kΩ O_{PP} resistor but a tweak is required depending on your application.

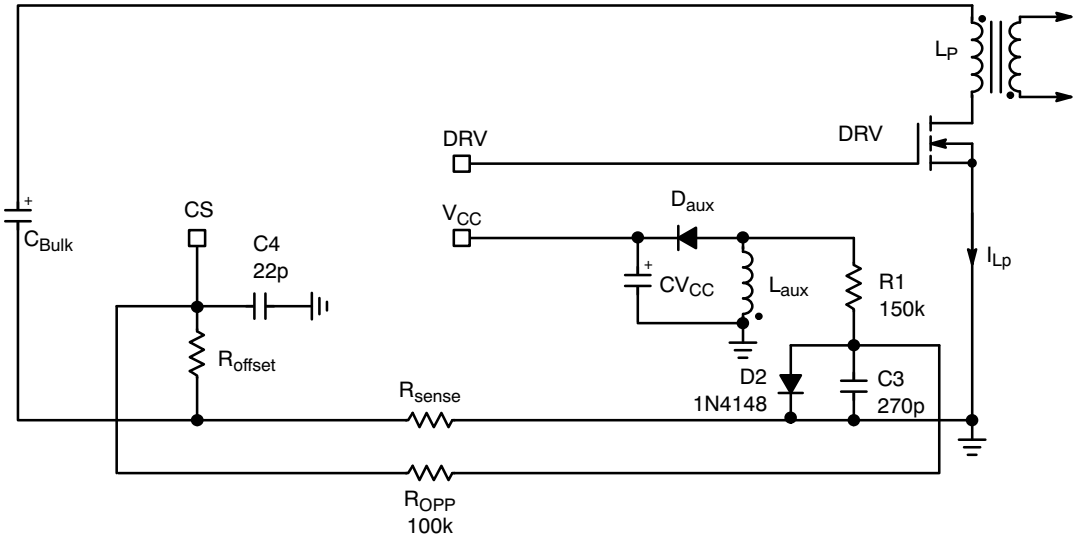


Figure 14. The OPP is Relatively Easy to Implement and It Does not Waste Power

Suppose you would need to reduce the peak current by 15% in high−line conditions. The turn−ratio between the auxiliary winding and the primary winding is N_{aux}. Assume its value is 0.15. Thus, the voltage on D_{aux} cathode swings negative during the on time to a level of:

$$V_{aux\_peak} = -V_{in\_max}N_{aux} = -375 \times 0.15 = -56\ V \quad \text{(eq. 8)}$$

If we selected a 3.7 kΩ resistor for R_{offset}, then the maximum sense voltage being developed is:

$$V_{sense} = 3.7\ k \times 270\ \mu = 1\ V \quad \text{(eq. 9)}$$

The small RC network made of R_1 and C_3, purposely limits the voltage excursion on D_2 anode. Assume the primary inductance value gives an on time of 3 μs at high−line. The voltage across C_3 thus swings down to:

$$V_{C3} = \frac{t_{on}V_{aux\_peak}}{R_1C_3} = -\frac{3\ \mu \times 56}{150\ k \times 270\ p} = -4.2\ V \quad \text{(eq. 10)}$$

Typically, we measured around −4 V on our 50 W prototype. By calculation, we want to decrease the peak current by 15%. Compared to the internal 270 μA source, we need to derive:

$$I_{offset} = -0.15 \times 270\ \mu = -40.5\ \mu A \quad \text{(eq. 11)}$$

Thus, from the −4 V excursion, the R_{OPP} resistor is derived by:

$$R_{OPP} = \frac{4}{40.5\ \mu} = 98\ k\Omega \quad \text{(eq. 12)}$$

After experimental measurements, the resistor was normalized down to 100 kΩ.

Feedback

Unlike other controllers, the feedback in the NCP1351 works in current rather than voltage. Figure 15 details the internal circuitry of this particular section. The optocoupler injects a current into the FB pin in relationship with the input/output conditions.

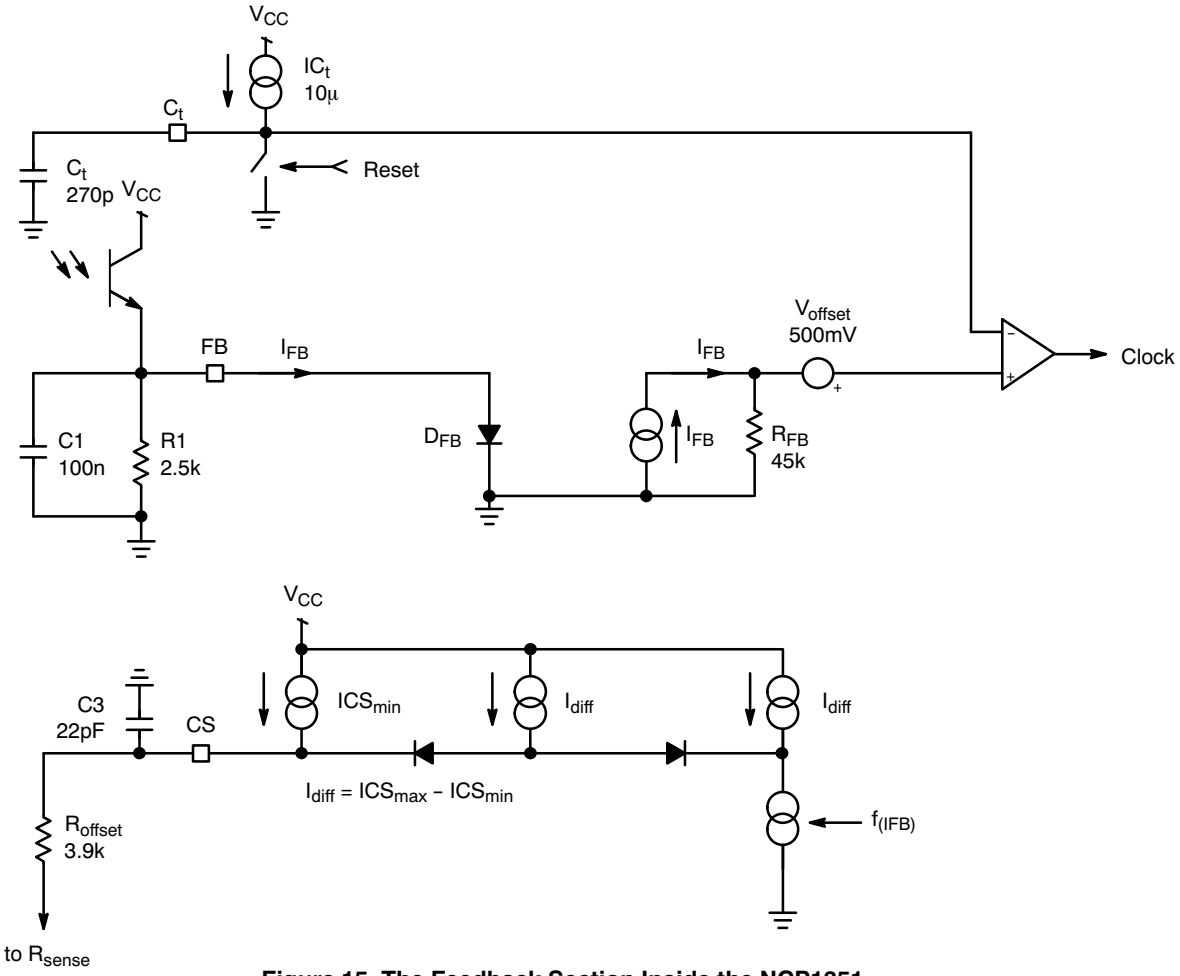


Figure 15. The Feedback Section Inside the NCP1351

The FB pin can actually be seen as a diode, forward biased by the optocoupler current. The feedback current, I_{FB} on Figure 15, enter an internal 45 kΩ resistor which develops a voltage. This voltage becomes the variable threshold point for the capacitor charge, as indicated by Figure 10. Thus, in lack of feedback current (start−up or short−circuit), there is no voltage across the 45 kΩ and the series offset of 500 mV clamps the capacitor swing. If a 270 pF capacitor is used, the maximum switching frequency is 65 kHz.

Folding the frequency back at a rather high peak current can obviously generate audible noise. For this reason, the NCP1351 uses a patented current compression technique which reduces the peak current in lighter load conditions. By design, the peak current changes from 100% of its full load value, to 30% of this value in light load conditions. This is the block placed on the lower left corner of Figure 15. In full load conditions, the feedback current is weak and all the current flowing through the external offset resistor is:

$$I_{CS} = I_{CS\_min} + I_{dif} = I_{CS\_max} - I_{CS\_min} + I_{CS\_min} = I_{CS\_max} \quad \text{(eq. 13)}$$

As the load goes lighter, the feedback current increases and starts to steal current away from the generators. Equation 12 can thus be updated by:

$$I_{CS} = I_{CS\_max} - kI_{FB} \quad \text{(eq. 14)}$$

Equation 13 testifies for the current reduction on the offset generator, k represents an internal coefficient. When the feedback current equals I_{dif}, the offset becomes:

$$I_{CS} = I_{CS\_min} \quad \text{(eq. 15)}$$

At this point, the current is fully compressed and remains frozen. To further decrease the transmitted power, the frequency does not have other choice than going down.

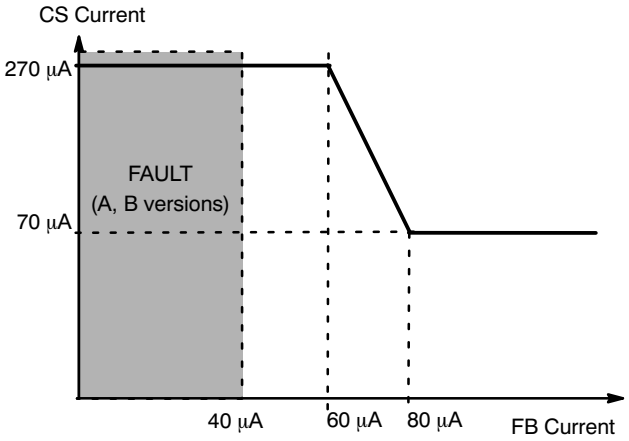


Figure 16. The NCP1351 Peak Current Compression Scheme

Looking to the data−sheet specifications, the maximum peak current is set to 270 μA whereas the compressed current goes down to 70 μA. The NCP1351 can thus be considered as a multi operating mode circuit:

- Real fixed peak current / variable frequency mode for FB current below 60 μA.
- Then maximum peak current decreases to $I_{CS,min}$ over a narrow linear range of I_{FB} (to avoid instability created by a discrete jump from $I_{CS,max}$ to $I_{CS,min}$), between 60 μA and 80 μA.
- Then if I_{FB} keeps on increasing, in a real fixed peak current/variable frequency mode with reduced peak current

For biasing purposes and noise immunity improvements, we recommend to wire a pulldown resistor and a capacitor in parallel from the FB pin to the controller ground (Figure 17). Please keep these elements as close as possible to the circuit. The pulldown resistor increases the optocoupler current but also plays a role in standby. We found that a 2.5 kΩ resistor was giving a good tradeoff between optocoupler operating current (internal pole position) and standby power.

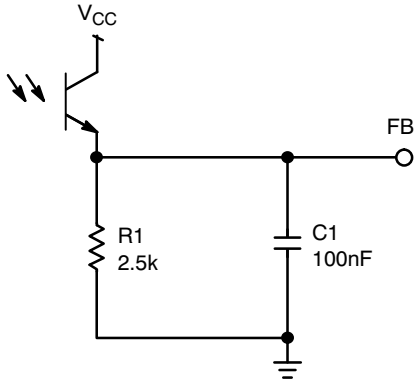


Figure 17. The Recommended Feedback Arrangement Around the FB Pin

Fault detection

The fault detection circuitry permanently observes the FB current, as shown on Figure 19. When the feedback current decreases below 40 μA, an external capacitor is charged by a 11.7 μA source. As the voltage rises, a comparator detects when it reaches 5 V typical. Upon detection, there can be two different scenarios:

1. A version: the circuit immediately latches−off and remains latched until the voltage on the current into the V_{CC} pin drops below a few μA. The latch is made via an internal SCR circuit who holds VCC to around 6 V when fired. As long as the current flowing through this latch is above a few μA, the circuit remains locked−out. When the user unplugs the converter, the V_{CC} current falls down and resets the latch.
2. B version: the circuit stops its output pulses and the auxiliary V_{CC} decreases via the controller own consumption (≈600 μA). When it touches the $V_{CC(min)}$ point, the circuit re−starts and attempts to crank the power supply. If it fails again, an hiccup mode takes place (Figure 18).
3. C version: this version includes the dual Over Current Protection (OCP) level. When the switching frequency imposed by the feedback loop reaches around 50% of the maximum value set by the Ct capacitor, the timer starts to count down. If the fault disappears, the timer is reset. When the fault is finally confirmed, the controller latches off as the A version.
4. D version: this version includes the dual Over Current Protection (OCP) level. When the switching frequency imposed by the feedback loop reaches around 50% of the maximum value set by the Ct capacitor, the timer starts to count down. If the fault disappears, the timer is reset. When the fault is finally confirmed, the controller enters auto−recovery mode, as with the B version.

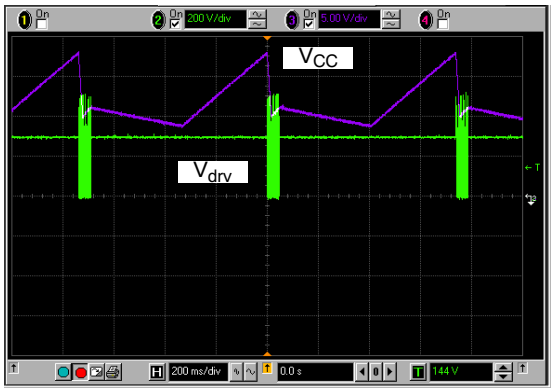


Figure 18. Hiccup Occurs with the B Version Only, the A Version Being Latched

The duty−burst in fault is around 7% in this particular case.

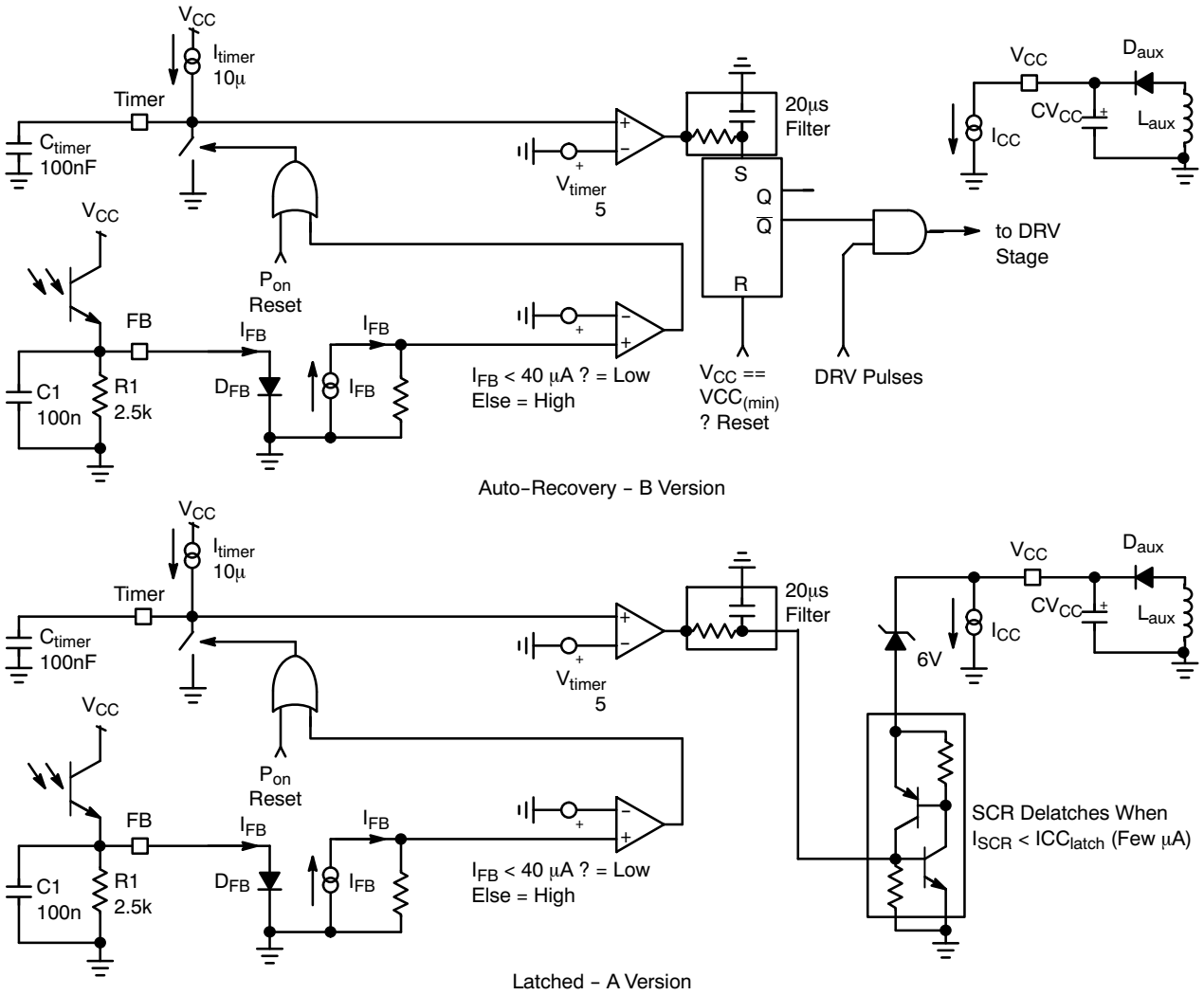


Figure 19. The Internal Fault Management Differs Depending on the Considered Version

Knowing both the ending voltage and the charge current, we can easily calculate the timer capacitor value for a given delay. Suppose we need 40 ms. In that case, the capacitor is simply:

$$C_{timer} = \frac{I_{timer} T}{V_{timer}} = \frac{11.7\ \mu \times 40\ m}{5} = 94\ nF \qquad \text{(eq. 16)}$$

Select a 100 nF value.

To let the designer understand the behavior behind the four different options (A, B, C and D), we have graphed important signals during a fault condition. In versions A and B, an internal error flag is raised as soon the controller hits the maximum operating frequency. At this moment, the external timer capacitor charge begins. If the fault persists, the timer capacitor hits the fault level and the circuit is either latched (A) or enters auto−recovery burst mode (B). If the fault disappears, the timer capacitor is simply reset to 0 V by an internal switch.

On version C and D, the error flag is asserted as soon as the current feedback imposes a switching frequency roughly equal to half of the maximum limit. For instance, should the designer select a 100 kHz maximum switching frequency, then the error flag would raise and start the timer for an operating frequency above ≈ 50 kHz. Below 50 kHz, the timer pin remains grounded. If we consider a DCM operation at full load, as the inductor peak current is kept constant, these 50 kHz correspond to 50% of the maximum delivered power. If the load stays between 50% and 100% of its nominal value, the timer continues to charge until it reaches the final level. In that case, the circuit latches off (C) or enters auto−recovery (D). This behavior is particularly well suited for applications where the converter delivers a moderate average power but is subjected to sudden peak loading conditions. For instance, a power supply is designed to permanently deliver 20 W but is sized to deliver 80 W in peak conditions. During these 80 W power excursions, the timer will react but will not shut down the power supply. On the contrary, if a short−circuit appends or if the transient overload lasts too long, the timer will immediately start to further shutdown the controller in order to protect both the application and downstream load.

Depending on the design conditions (DCM or CCM), the error flag assertion will correspond to either 50% of the maximum power (full load DCM design) or a value above this number if the converter operates in CCM at full load and remains in CCM at half the switching frequency.

The figures below details circuits operation for the various controller options.

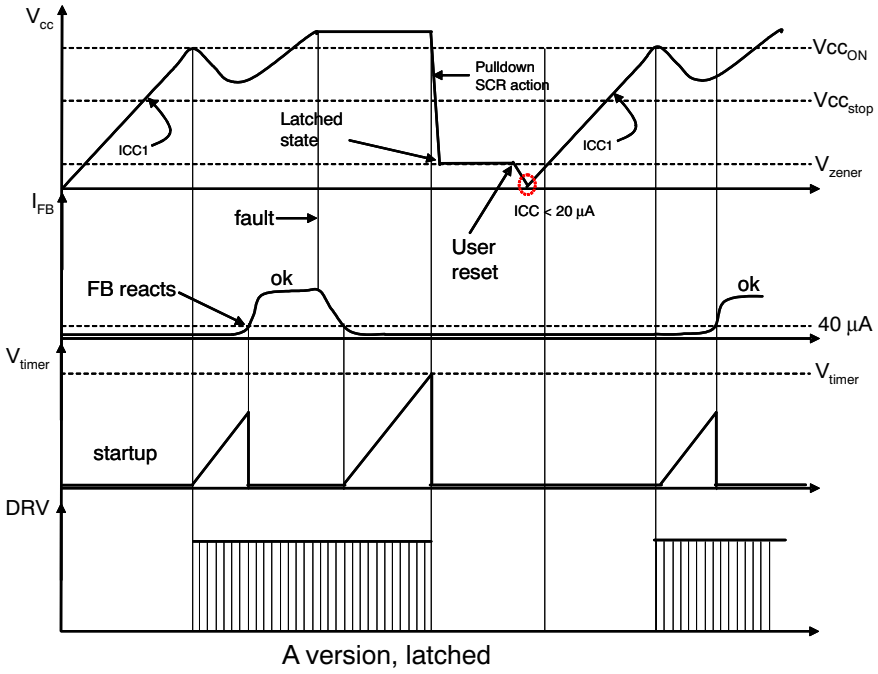


Figure 20. The A Version Latches−off in Presence of a Fault

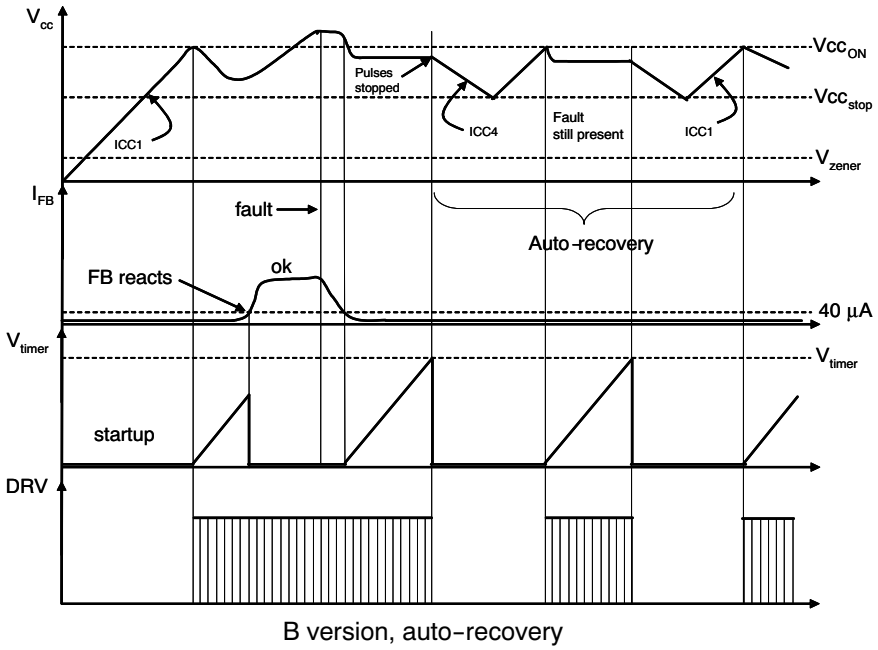
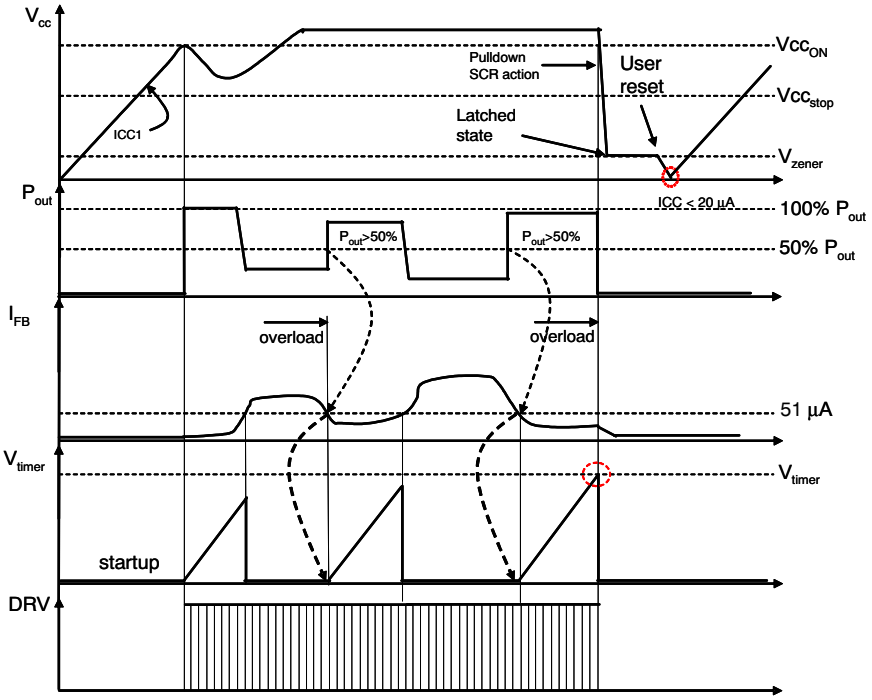
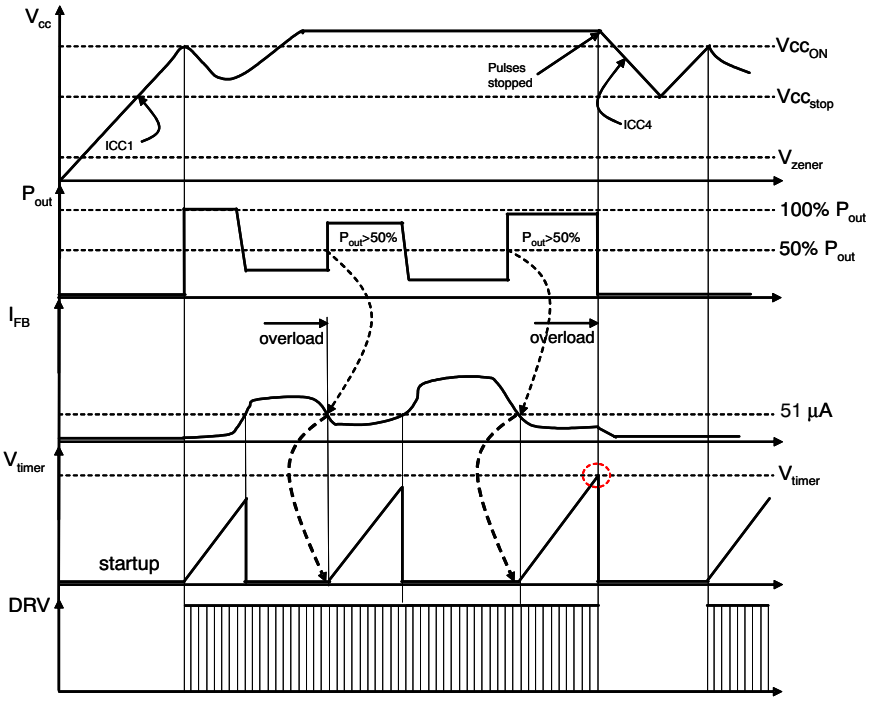


Figure 21. The B Version Enters an Auto−Recovery Burst Mode in Presence of a Fault



C version, latched dual OCP level

Figure 22. The C Version Latches if the Power Excursion Exceeds 50% of the Maximum Power Too Long (DCM Full Load Operation)



D version, auto−recovery dual OCP level

Figure 23. The D Version Enters Auto−Recovery Burst Mode if the Power Excursion Exceeds 50% of the Maximum Power (DCM Full Load Operation)

Latch Input

The NCP1351 features a patented circuitry which prevents the FB input to be of low impedance before the V_{CC} reaches the VCC_{ON} level. As such, the circuit can work in a primary regulation scheme. Capitalizing on this typical option, Figure 24 shows how to insert a zener diode in series with the optocoupler emitter pin. In that way, the current biases the zener diode and offers a nice reference voltage, appearing at the loop closure (e.g. when the output reaches the target). Yes, you can use this reference voltage to supply a NTC and form a cheap OTP protection.

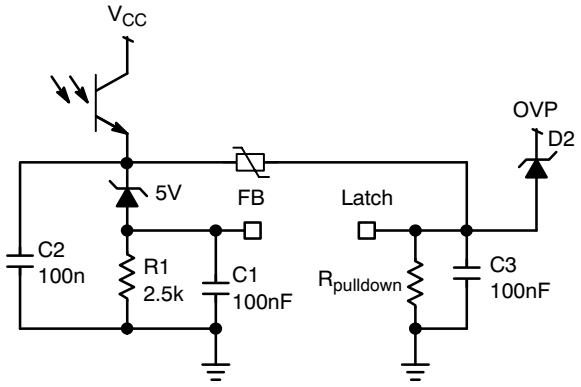


Figure 24. The Latch Input Offers Everything Needed to Implement an OTP Circuit. Another Zener Can Help combining an OVP Circuit if Necessary

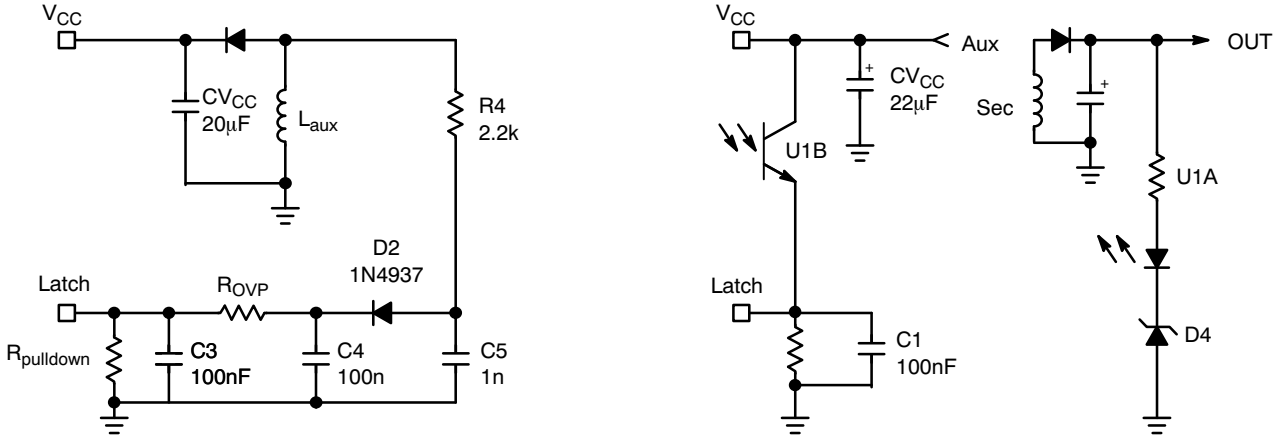


Figure 25. You can either directly observe the V_{CC} level or add a small RC filter to reduce the leakage inductance contribution. The best is to directly sense the output voltage and reacts if it runs away, as offered on the right side.

Design Example, a 19 V / 3 A

A Universal Mains Power Supply Designing a Switch−Mode Power Supply using the NCP1351 does not differ from a fixed frequency design. What changes, however, is the regulation method via frequency variations. In other words, all the calculations must be carried at the lowest line input where the frequency will hit the maximum value set by the C_t capacitor. Let us follow the steps:

V_{in} min = 100 Vdc (bulk valley in low−line conditions)
V_{in} max = 375 Vdc
V_{out} = 19 V
I_{out} = 3 A
Operating mode is CCM
η = 0.8
F_{sw} = 65 kHz

1. Turn Ratio. This is the first parameter to consider. The MOSFET BV_{dss} actually dictates the amount of reflected voltage you need. If we consider a 600 V MOSFET and a 15% derating factor, we must limit the maximum drain voltage to:

$$V_{ds\_max} = 600 \times 0.85 = 510\ V \quad \text{(eq. 17)}$$

Knowing a maximum bulk voltage of 375 V, the clamp voltage must be set to:

$$V_{clamp} = 510 - 375 = 135\ V \quad \text{(eq. 18)}$$

Based on the above level, we decide to adopt a headroom between the reflected voltage and the clamp level of 50 V. If this headroom is too small, a high dissipation will occur on the RDC clamp network and efficiency will suffer. A leakage inductance of around 1% of the magnetizing value should give good results with this choice (k_c = 1.6). The turn ratio between primary and secondary is simply:

$$\frac{(V_{out} + V_f)}{N} = \frac{V_{clamp}}{k_c} \quad \text{(eq. 19)}$$

Solving for N gives:

$$N = \frac{N_s}{N_p} = \frac{k_C(V_{out} + V_f)}{V_{clamp}} = \frac{1.6 \times (19 + 0.8)}{135} = 0.234 \quad \text{(eq. 20)}$$

Let us round it to 0.25 or 1/N = 4

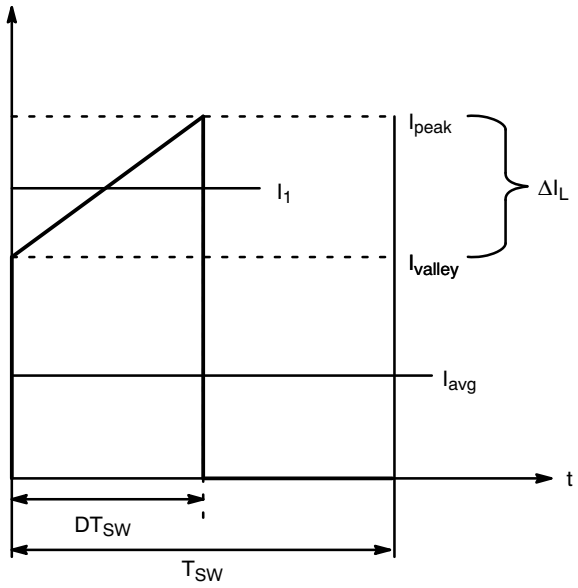


Figure 26. Primary Inductance Current Evolution in CCM

2. Calculate the maximum operating duty−cycle for this flyback converter operated in CCM:

$$d_{max} = \frac{V_{out}/N}{V_{out}/N + V_{in\_min}} = \frac{19 \times 4}{19 \times 4 + 100} = 0.43 \quad \text{(eq. 21)}$$

In this equation, the CCM duty−cycle does not exceed 50%. The design should thus be free of subharmonic oscillations in steady−state conditions. If necessary, negative ramp compensation is however feasible by the auxiliary winding.

3. To obtain the primary inductance, we can use the following equation which expresses the inductance in relationship to a coefficient k. This coefficient actually dictates the depth of the CCM operation. If it goes to 2, then we are in DCM.

$$L = \frac{(V_{in\_min} d_{max})^2}{F_{SW} K P_{in}} \quad \text{(eq. 22)}$$

where $K = \Delta I_L / I_I$ and defines the amount of ripple we want in CCM (see Figure 26).

- Small K: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- Large K: approaching BCM where the RMS losses are the worse, but smaller inductance, leading to a better leakage inductance.

From Equation 17, a K factor of 0.8 (40% ripple) ensures a good operation over universal mains. It leads to an inductance of:

$$L = \frac{(100 \times 43)^2}{65\text{ k} \times 0.8 \times 72} = 493\ \mu H \quad \text{(eq. 23)}$$

$$\Delta I_L = \frac{V_{in\_min} d_{max}}{L F_{SW}} = \frac{100 \times 0.43}{493\text{ u} \times 65\text{ k}} = 1.34\text{ A peak-to-peak} \quad \text{(eq. 24)}$$

The peak current can be evaluated to be:

$$I_{in\_avg} = \frac{P_{out}}{\eta V_{in\_min}} = \frac{19 \times 3}{0.8 \times 100} = 712\text{ mA} \quad \text{(eq. 25)}$$

$$I_{peak} = \frac{I_{avg}}{d} + \frac{\Delta I_L}{2} = \frac{0.712}{0.43} + \frac{1.34}{2} = 2.33\text{ A} \quad \text{(eq. 26)}$$

On Figure 26, I_1 can also be calculated:

$$I_I = I_{peak} - \frac{\Delta I_L}{2} = 2.33 - \frac{1.34}{2} = 1.65\text{ A} \quad \text{(eq. 27)}$$

The valley current is also found to be:

$$I_{valley} = I_{peak} - \Delta I_L = 2.33 - 1.34 = 1.0\text{ A} \quad \text{(eq. 28)}$$

4. Based on the above numbers, we can now evaluate the RMS current circulating in the MOSFET and the sense resistor:

$$I_{d\_rms} = I_I \sqrt{d} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta I_L}{2 I_1}\right)^2} = 1.65 \times 0.65 \times \sqrt{1 + \frac{1}{3}\left(\frac{1.34}{2 \times 1.65}\right)^2} = 1.1\text{ A} \quad \text{(eq. 29)}$$

5. The current peaks to 2.33 A. Selecting a 1 V drop across the sense resistor, we can compute its value:

$$R_{sense} = \frac{1}{I_{peak}} = \frac{1}{2.5} = 0.4\ \Omega \quad \text{(eq. 30)}$$

To generate 1 V, the offset resistor will be 3.7 kΩ, as already explained. Using Equation 29, the power dissipated in the sense element reaches:

$$P_{sense} = R_{sense} I_{d\_rms}^2 = 0.4 \times 1.1^2 = 484\text{ mW} \quad \text{(eq. 31)}$$

6. To switch at 65 kHz, the C_t capacitor connected to pin 2 will be selected to 180 pF.
7. As the load changes, the operating frequency will automatically adjust to satisfy either equation 5 (high power, CCM) or equation 6 in lighter load conditions (DCM).

Figure 27 portrays a possible application schematic implementing what we discussed in the above lines.

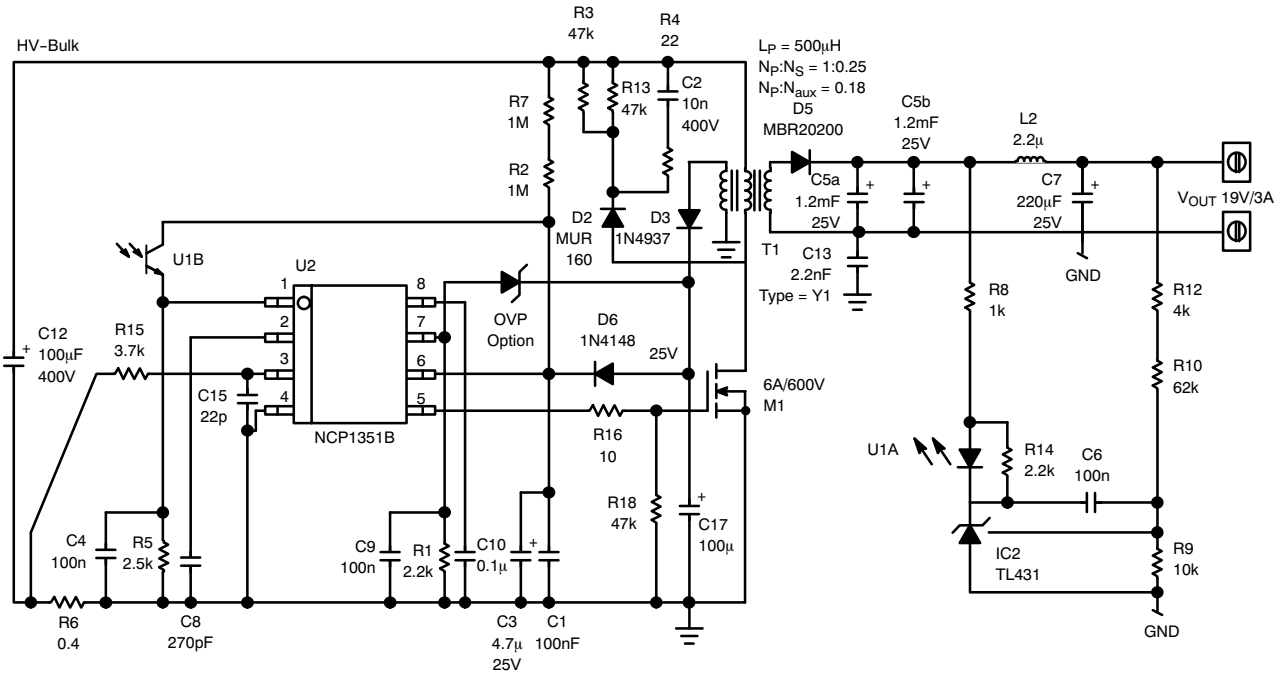


Figure 27. The 19 V Adapter Featuring the Elements Calculated Above

On this circuit, the V_{CC} capacitor is split in two parts, a low value capacitor (4.7 μF) and a bigger one (100 μF). The 4.7 μF capacitor ensures a low startup time, whereas the second capacitor keeps the V_{CC} alive in standby mode (where the switching frequency can be low). Due to D_6, it does not hamper startup time.

Application Results

We assembled a board with component values close to what is described on Figure 27. Here are the obtained results:

P_{in} @ no−load = 152 mW, V_{in} = 230 Vac
P_{in} @ no−load = 164 mW, V_{in} = 100 Vac

The efficiency stays flat to above 80%, and keeps good even at low output levels. It clearly shows the benefit of the variable frequency implemented in the NCP1351.

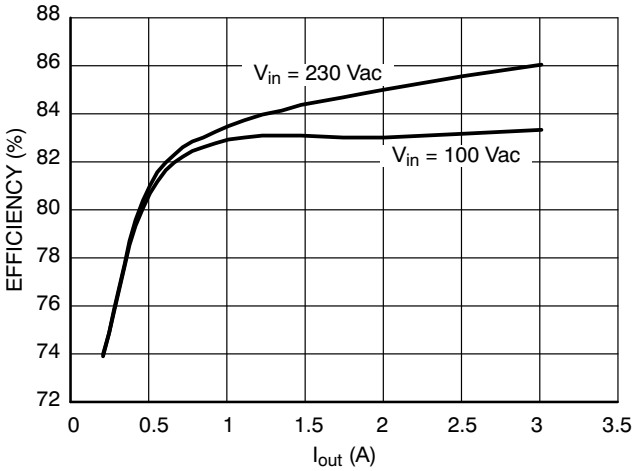


Figure 28. Efficiency Measured at Various Operating Points

Another benefit of the variable frequency lies in the low ripple operation at no−load. This is what confirms Figure 29.

Finally, the power supply was tested for its transient response, from 100 mA to 3 A, high and low line, with a slew−rate of 1 A/μs (Figure 31). Results appear in Figures 31 and 32 and confirm the stability of the board.

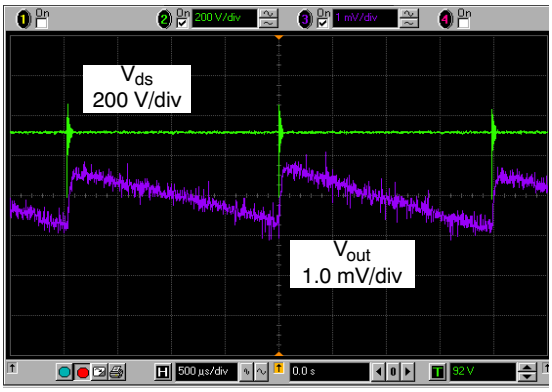


Figure 29. No−Load Output Ripple (V_{in} = 230 Vac)

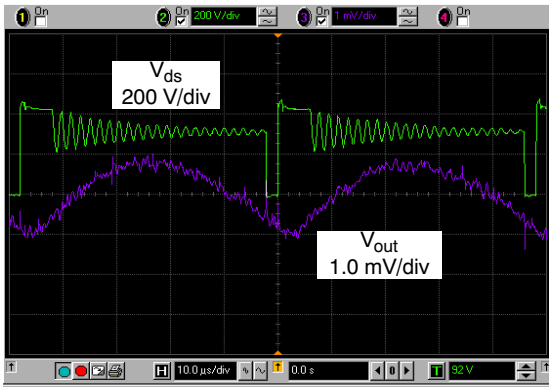


Figure 30. Same Conditions, P_{out} = 5 W

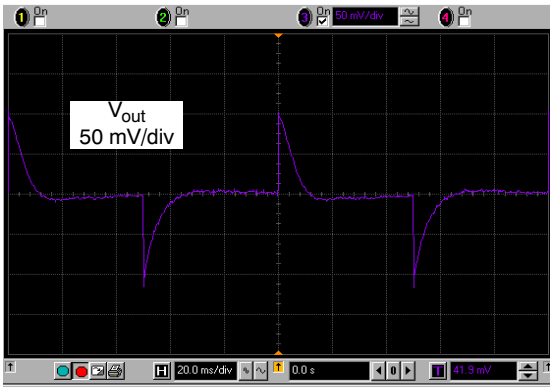


Figure 31. Transient Step, Low Line

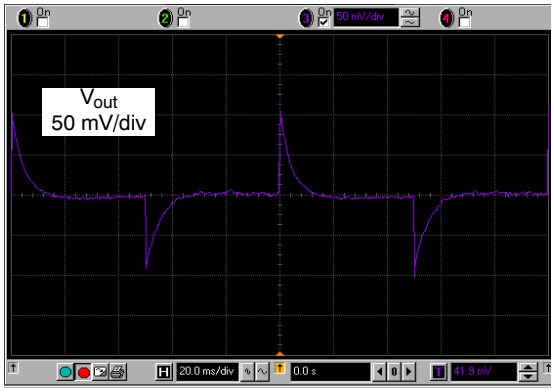


Figure 32. Transient Step, High Line

CHARACTERIZATION CURVES

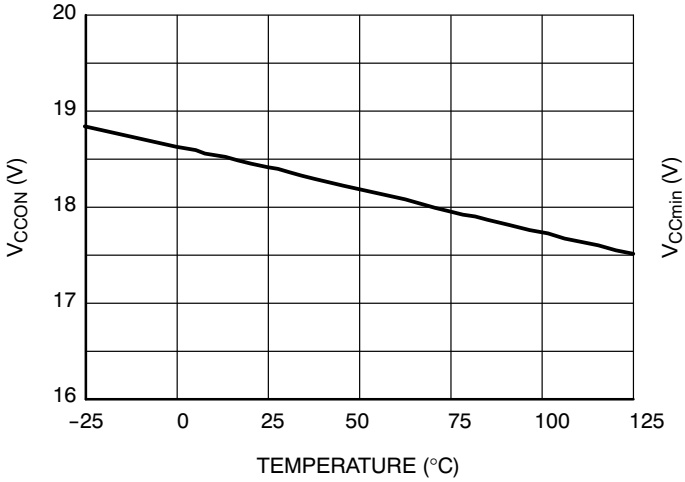


Figure 33. V_{CCON} Level versus Junction Temperature

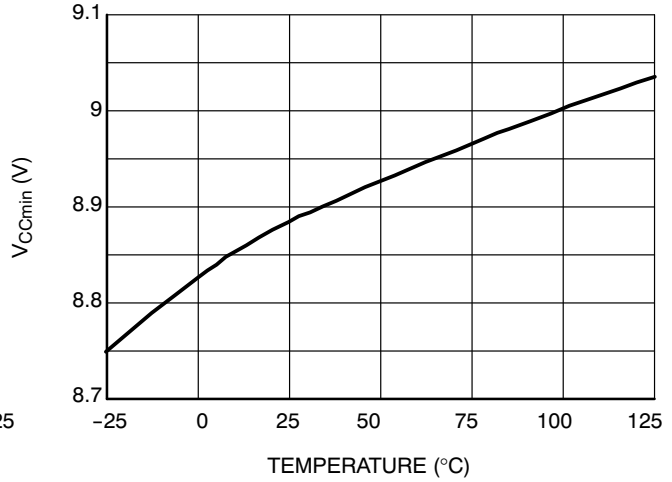


Figure 34. V_{CCmin} Level versus Junction Temperature

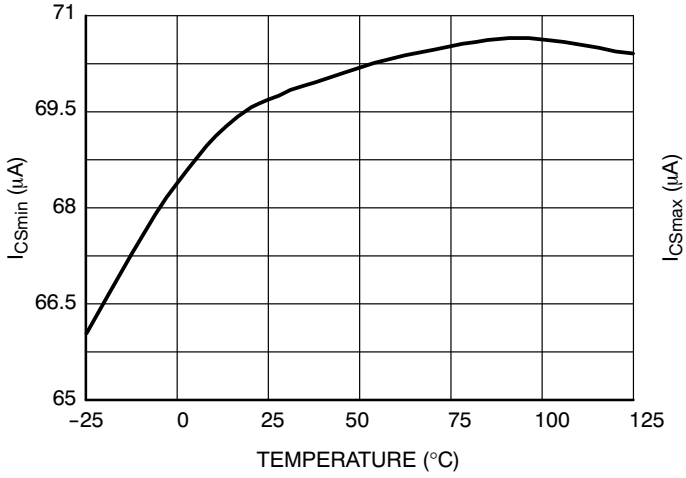


Figure 35. I_{CSmin} versus Junction Temperature

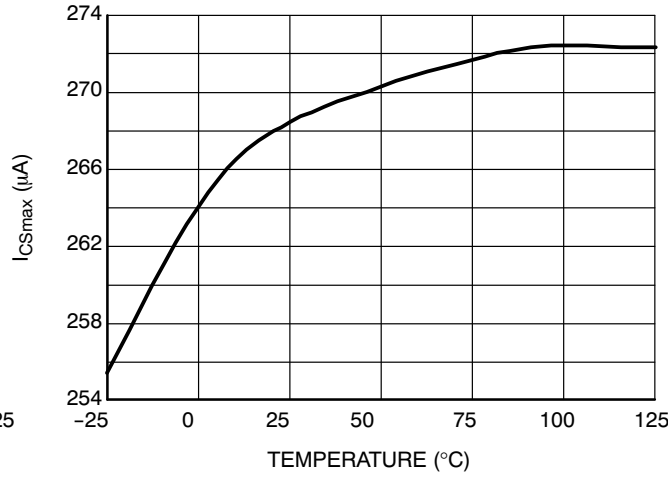


Figure 36. I_{CSmax} versus Junction Temperature

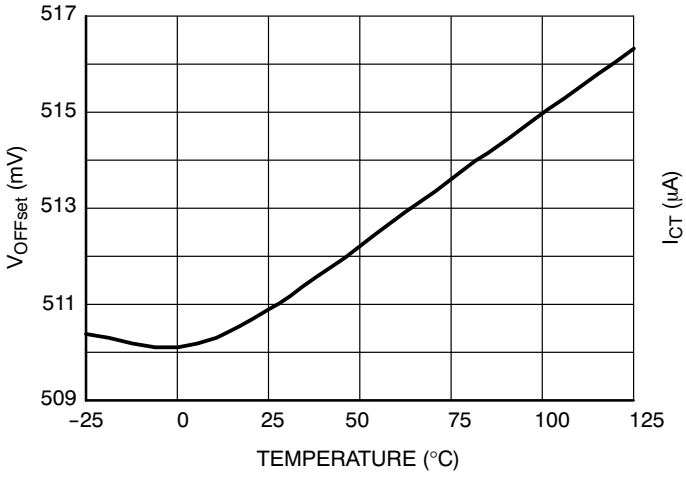


Figure 37. Oscillator Offset Voltage versus Junction Temperature

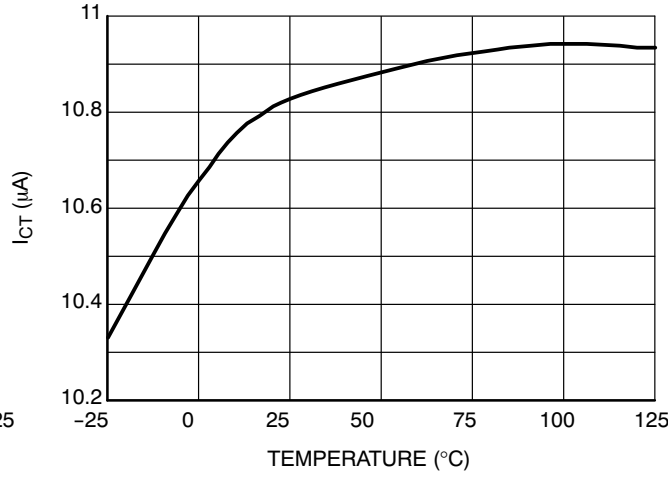


Figure 38. Timing Capacitor Charge−Current Variation versus Junction Temperature

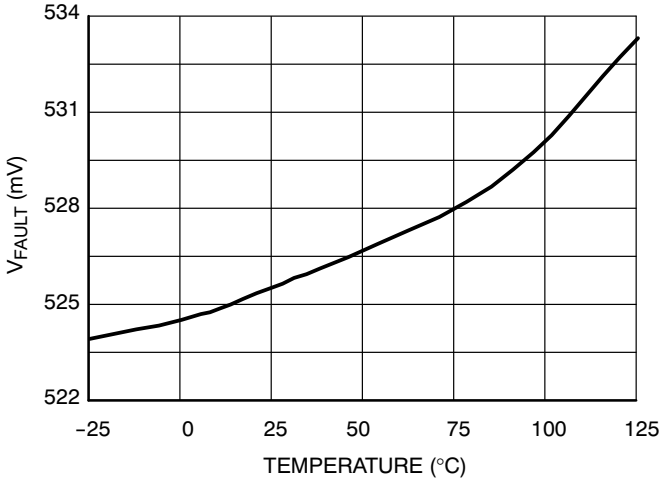


Figure 39. Fault Voltage Variations versus Junction Temperature (A and B Versions)

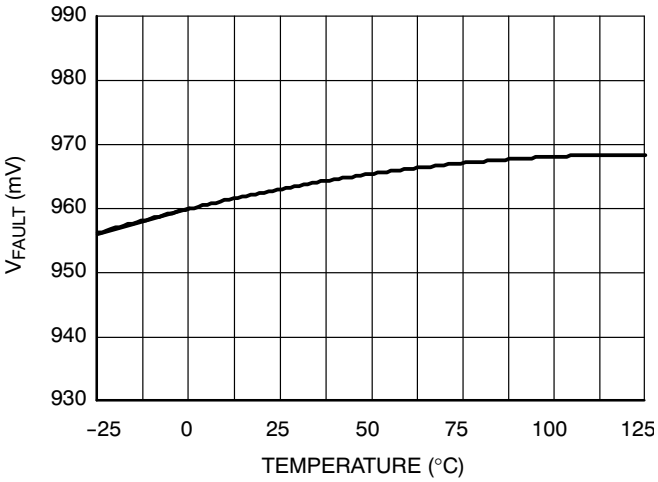


Figure 40. Fault Voltage Variations versus Junction Temperature (C and D Versions)

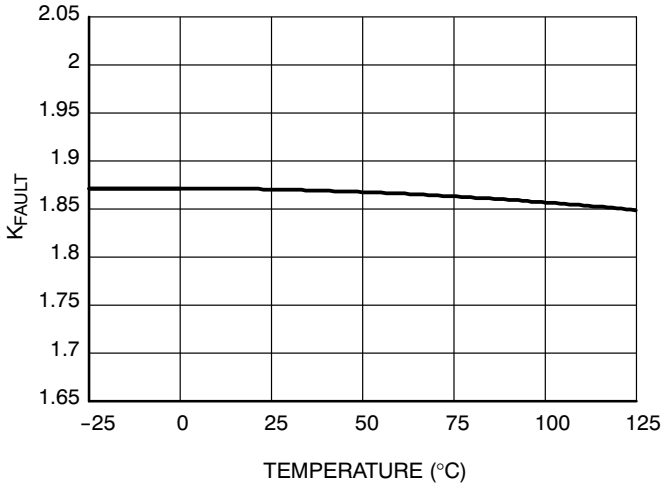


Figure 41. K_{FAULT} Variations versus Junction Temperature

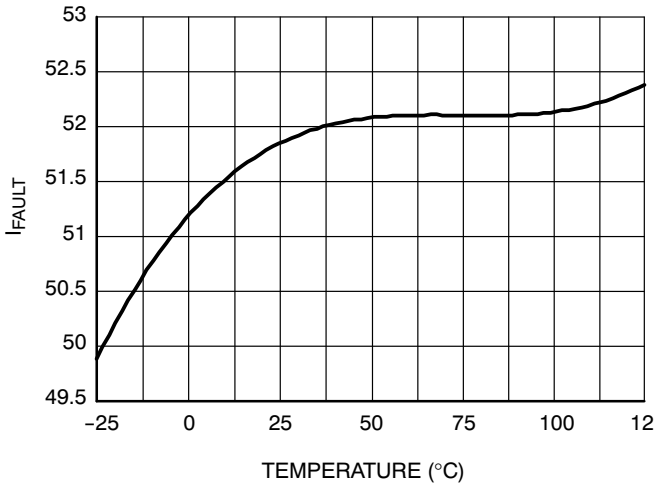


Figure 42. I_{FAULT} Current Variation versus Junction Temperature (Versions C and D)

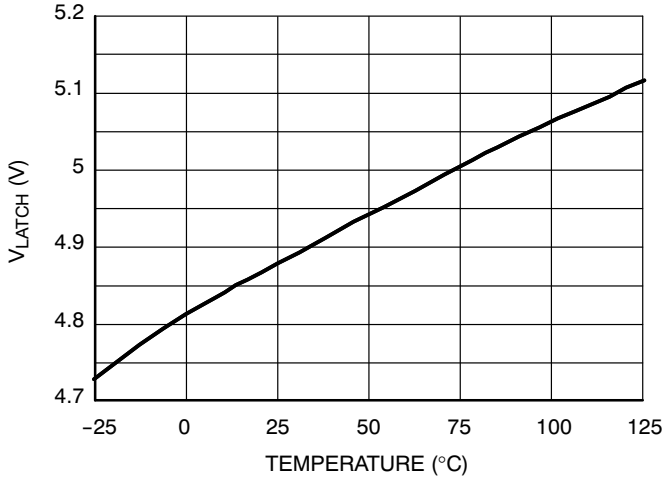


Figure 43. Latch Level Evolution versus Junction Temperature

ORDERING INFORMATION

Device	Package Type	Shipping†
NCP1351ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1351BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1351CDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1351DDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1351APG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1351BPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1351CPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1351DPG	PDIP−8 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

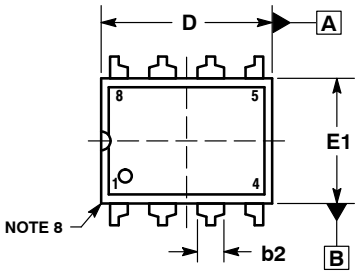
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

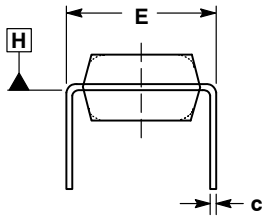
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

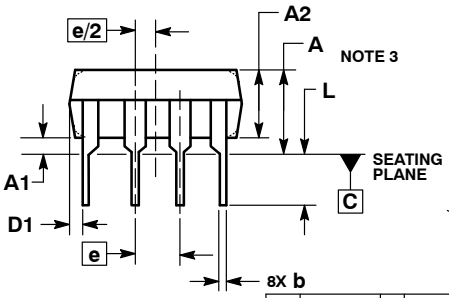
DATE 22 APR 2015



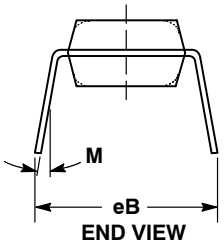
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



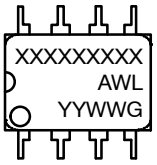
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

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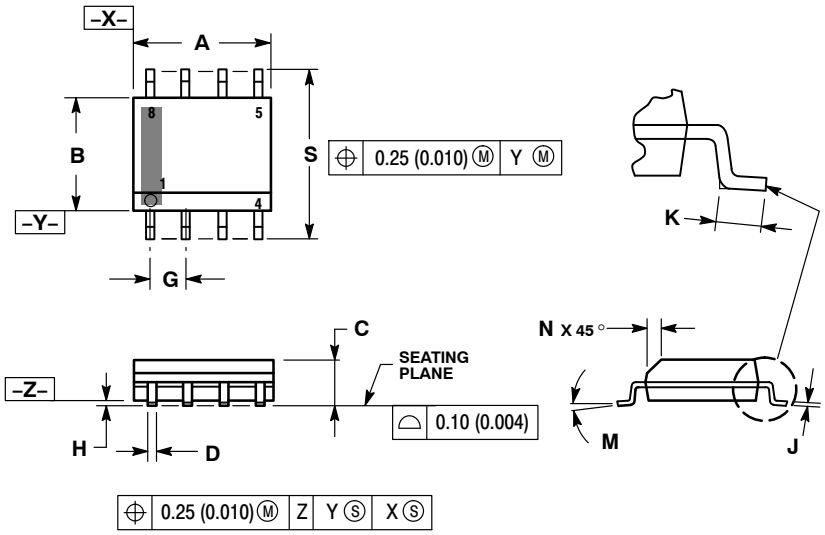
SOIC−8 NB
CASE 751−07
ISSUE AK

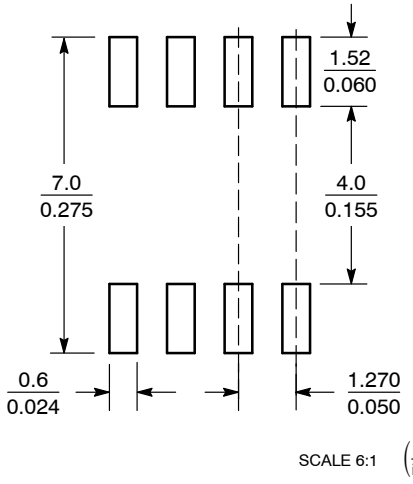
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

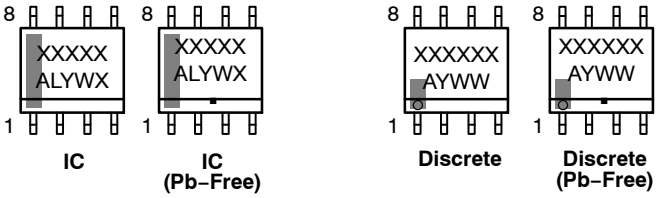
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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