LDO Regulator - Very Low Dropout, CMOS, Bias Rail
700 mA

NCP137

The NCP137 is a 700 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP137 features low I_Q consumption. The WLCSP6 1.2 mm x 0.8 mm Chip Scale package is optimized for use in space constrained applications.

Features

- Input Voltage Range: V_{OUT} to 5.5 V
- Bias Voltage Range: 2.5 V to 5.5 V
- Adjustable and Fixed Voltage Version Available
- Output Voltage Range: 0.4 V to 1.8 V (Fixed) and 0.5 V to 3.0 V (Adjustable)
- ±1% Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra−Low Dropout: Typ. 40 mV at 700 mA
- Very Low Bias Input Current of Typ. 35 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 4.7 μF Ceramic Capacitor
- Available in WLCSP6 – 1.2 mm x 0.8 mm, 0.4 mm pitch Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

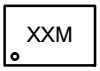
- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

ON Semiconductor™

www.onsemi.com

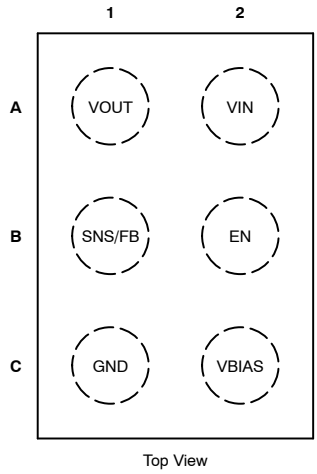
WLCSP6, 1.2x0.8
CASE 567MV

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code

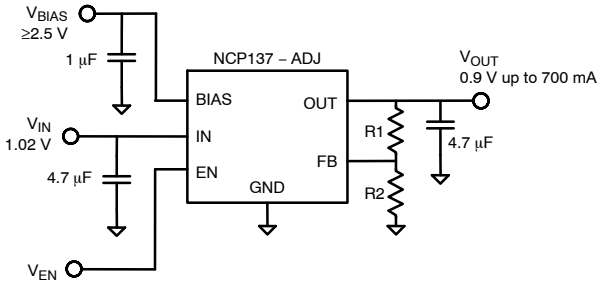
PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.



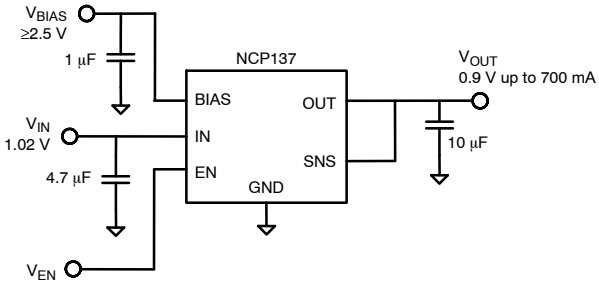
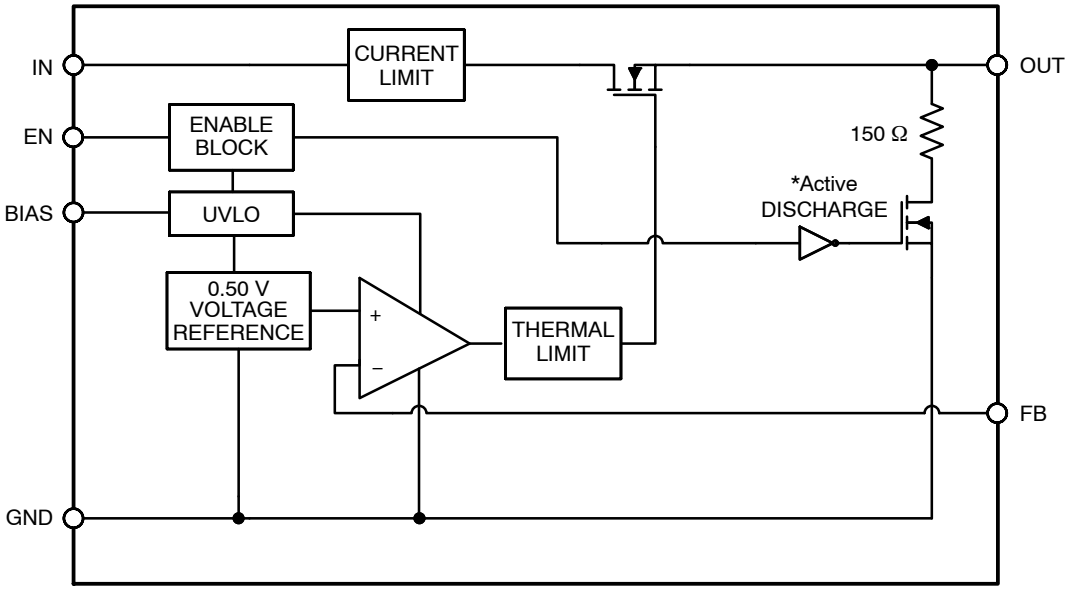
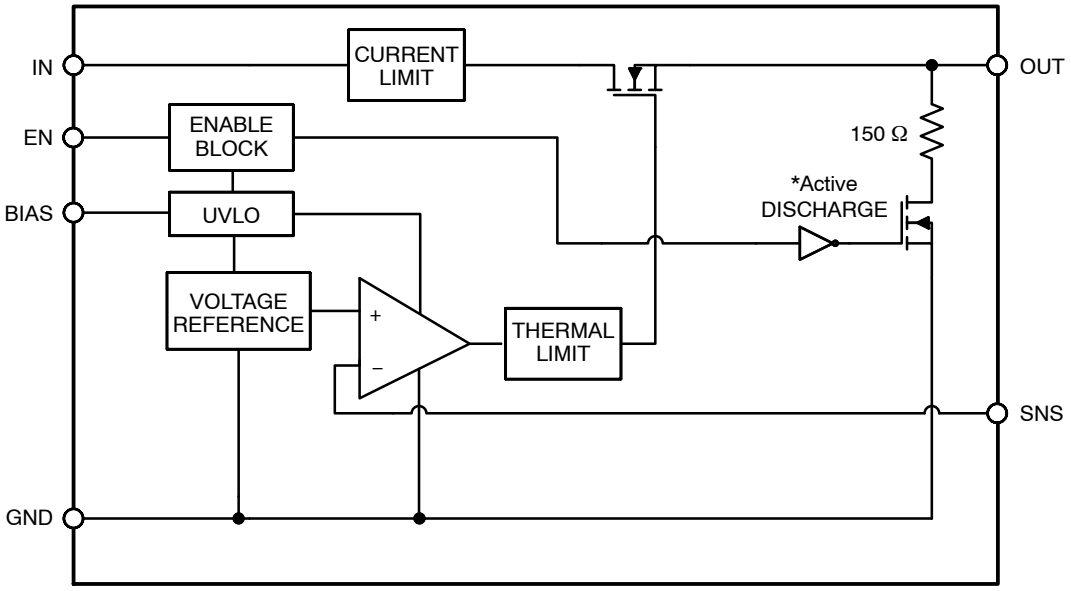


Figure 1. Typical Application Schematics



*Active output discharge function is present only in NCP137A option devices.

Figure 2. Simplified Schematic Block Diagram – Adjustable Version



*Active output discharge function is present only in NCP137A option devices.

Figure 3. Simplified Schematic Block Diagram – Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	VOUT	Regulated Output Voltage pin
A2	VIN	Input Voltage Supply pin
B1 (ADJ devices)	FB	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
B1 (Fix Volt devices)	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	VBIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 6	V
Chip Enable, Bias, FB and SNS Input	V_{EN}, V_{BIAS}, V_{FB}, V_{SNS}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.2 mm x 0.8 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	69	°C/W

3. This junction−to−ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1−ounce internal planes and 2−ounce copper on top and bottom. Top copper layer has a dedicated 1.6 sqmm copper area.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V_{IN}	V_{OUT} + V_{DO}		5.5	V
Operating Bias Voltage Range		V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		5.5	V
Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	UVLO		1.6 0.2		V
Reference Voltage (Adj devices)	T_J = +25°C	V_{REF}		0.500		V
Output Voltage Accuracy		V_{OUT}		±0.5		%
Output Voltage Accuracy	$-40°C \le T_J \le 85°C$, $V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V, 1 mA < I_{OUT} < 700 mA	V_{OUT}	−1.0		+1.0	%
V_{IN} Line Regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.0 V	$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V	$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 700 mA	$Load_{Reg}$		1.5		mV
V_{IN} Dropout Voltage	I_{OUT} = 700 mA (Notes 6, 7)	V_{DO}		40	60	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 700 mA, $V_{IN} = V_{BIAS}$ (Notes 6, 8, 9)	V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$	I_{CL}	800	1200	1500	mA
FB/SNS Pin Operating Current		I_{FB}, I_{SNS}		0.1	0.5	μA
Bias Pin Quiescent Current	V_{BIAS} = 2.7 V, I_{OUT} = 0 mA	I_{BIASQ}		35	50	μA
Bias Pin Disable Current	V_{EN} ≤ 0.4 V	$I_{BIAS(DIS)}$		0.5	1	μA
Vinput Pin Disable Current	V_{EN} ≤ 0.4 V	$I_{VIN(DIS)}$		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”	$V_{EN(H)}$	0.9			V
	EN Input Voltage “L”	$V_{EN(L)}$			0.4	
EN Pull Down Current	V_{EN} = 5.5 V	I_{EN}		0.3	1	μA
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 4.7 μF	t_{ON}		150		μs
Power Supply Rejection Ratio (Adj devices)	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 4.7 μF	PSRR(V_{IN})		75		dB
	V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.0 V, V_{BIAS} = 3.0 V, C_{OUT} = 4.7 μF	PSRR(V_{BIAS})		85		dB
Output Noise Voltage (Adj devices)	$V_{IN} = V_{OUT}$ +0.5 V, f = 10 Hz to 100 kHz, $V_{OUT(NOM)}$ = 1.0 V, C_{OUT} = 4.7 μF	V_N		35 x V_{OUT}/V_{REF}		μV_{RMS}
Thermal Shutdown Threshold	Temperature increasing			160		°C
	Temperature decreasing			140		

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Adjustable devices tested at $V_{OUT} = V_{REF}$ unless otherwise noted; external resistor tolerance is not taken into account.
6. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
7. For adjustable devices, V_{IN} dropout voltage tested at $V_{OUT(NOM)} = 2 \times V_{REF}$.
8. For adjustable devices, V_{BIAS} dropout voltage tested at $V_{OUT(NOM)} = 3 \times V_{REF}$ due to a minimum Bias operating voltage of 2.5 V.
9. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Output Discharge Pull−Down	$V_{EN} \le 0.4$ V, V_{OUT} = 0.5 V, NCP137A options only	R_{DISCH}		150		Ω
Power Supply Rejection Ratio (Fixed Voltage devices)	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.05 V, C_{OUT} = 10 μF	PSRR(V_{IN})		75		dB
	V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.05 V, V_{BIAS} = 3.0 V, C_{OUT} = 10 μF	PSRR(V_{BIAS})		85		dB
Output Noise Voltage (Fixed Voltage devices)	$V_{IN} = V_{OUT}$ +0.5 V, f = 10 Hz to 100 kHz, $V_{OUT(NOM)}$ = 1.05 V, C_{OUT} = 10 μF	V_N		40		μVRMS

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Adjustable devices tested at $V_{OUT} = V_{REF}$ unless otherwise noted; external resistor tolerance is not taken into account.
6. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
7. For adjustable devices, V_{IN} dropout voltage tested at $V_{OUT(NOM)} = 2 \times V_{REF}$.
8. For adjustable devices, V_{BIAS} dropout voltage tested at $V_{OUT(NOM)} = 3 \times V_{REF}$ due to a minimum Bias operating voltage of 2.5 V.
9. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

APPLICATIONS INFORMATION

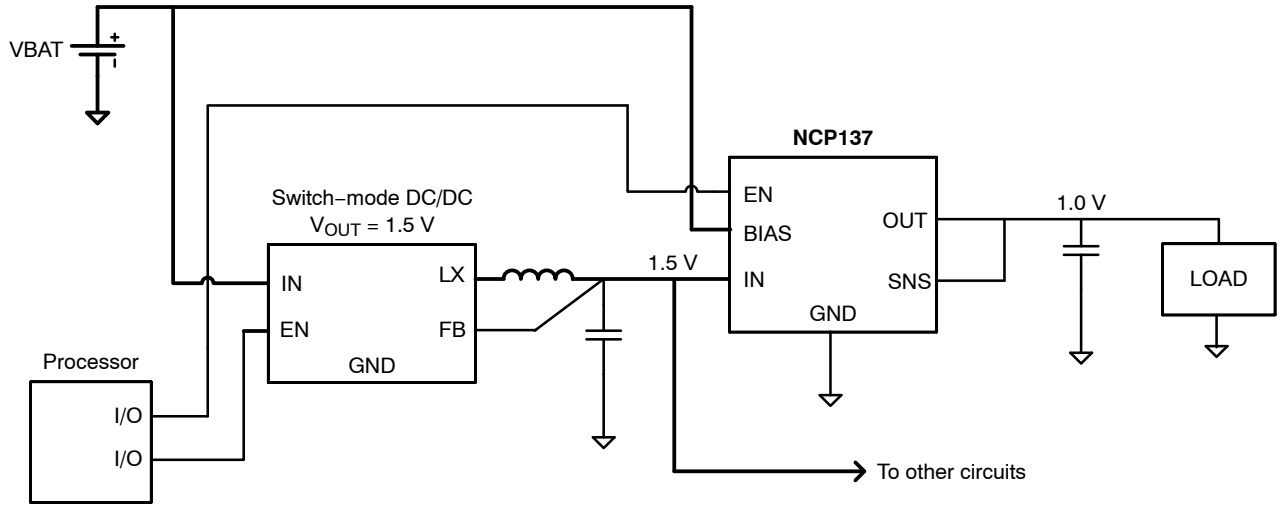


Figure 4. Typical Application: Low−Voltage DC/DC Post−Regulator with ON/OFF Functionality

The NCP137 dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. Vin to Vout operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

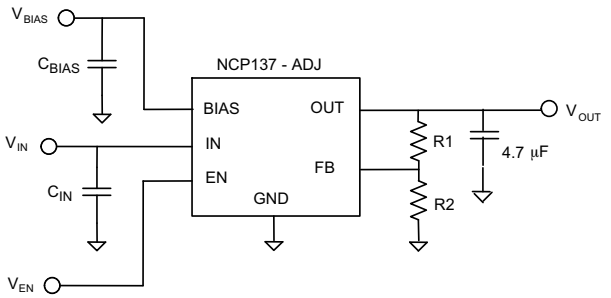
The NCP137 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP137 Voltage linear regulator Fixed and Adjustable version is available.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from 0.5 V to 3.0 V using two external resistors.

Typical application schematics is shown in Figure 5.



$$V_{OUT} = 0.5\ V \times (1 + R1/R2)$$

Figure 5. Typical Application Schematics

It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100 kΩ.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough; specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The Adjustable device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 4.7 μF to 22 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. For ADJ applications with nominal output voltage less than 0.6 V and for all the fixed voltage devices applications the output capacitor effective capacitance 10 μF to 22 μF is recommended.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} = 1 μF and C_{BIAS} = 0.1 μF or greater. Ceramic capacitors are recommended**.** For the best performance all the capacitors should be connected to the NCP137 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +105°C maximum.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
NCP137AFCTADJT2G	ADJ	A7	Output Active Discharge	WLCSP6 (Pb−Free)	5000 / Tape & Reel
NCP137AFCTCADJT2G	ADJ	A7	Output Active Discharge, Back Side Coating		
NCP137BFCTADJT2G	ADJ	D7	Non−Active Discharge		
NCP137AFCT045T2G	0.45 V	AT	Output Active Discharge		
NCP137AFCT105T2G	1.05 V	AA	Output Active Discharge		
NCP137AFCT110T2G	1.10 V	AH	Output Active Discharge		
NCP137AFCTC110T2G	1.10 V	AH	Output Active Discharge, Back Side Coating		
NCP137AFCT120T2G	1.20 V	AD	Output Active Discharge		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

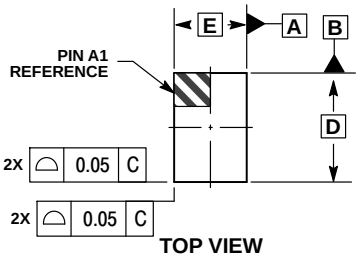
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

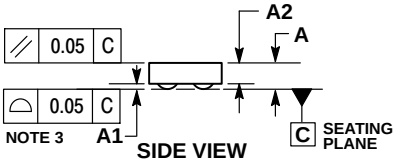
WLCSP6, 1.20x0.80
CASE 567MV
ISSUE B

SCALE 4:1

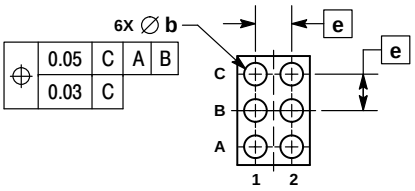
DATE 05 JUN 2018



TOP VIEW



SIDE VIEW

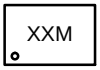


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	–––	0.33
A1	0.04	0.08
A2	0.23 REF	
b	0.24	0.30
D	1.20 BSC	
E	0.80 BSC	
e	0.40 BSC	

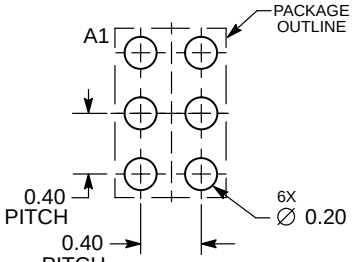
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON06670G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**WLCSP6, 1.20x0.80**		**PAGE 1 OF 1**

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