

NCP336, NCP337

Controlled Load Switch with Auto-Discharge Path, 3 A

Description

The NCP336 and NCP337 are very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail for the NCP337 part only.

Proposed in a wide input voltage range from 1.2 V to 5.5 V, in a small 1 x 1.5 mm WLCSP6, pitch 0.5 mm.

Features

- 1.2 V – 5.5 V Operating Range
- 21 mΩ P MOSFET at 4.5 V
- DC Current up to 3 A
- Output Auto-Discharge
- Active High EN Pin
- WLCSP6 1 x 1.5 mm
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices



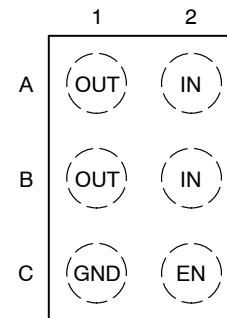
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WLCSP6
FC SUFFIX
CASE 567FH

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

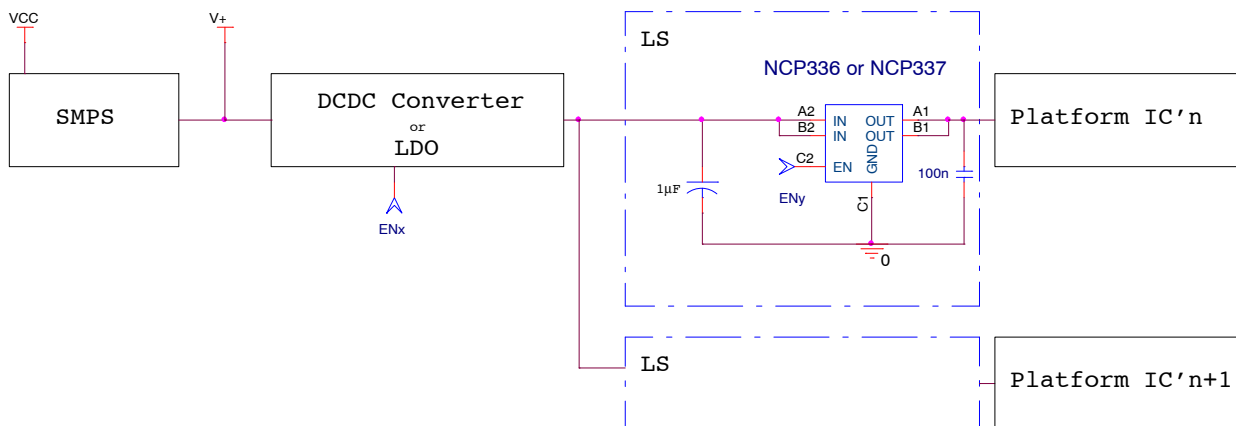


Figure 1. Typical Application Circuit

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Table 1. PIN FUNCTION DESCRIPTION

| Pin Name | Pin Number | Type | Description |
|----------|------------|--------|--|
| IN | A2, B2 | POWER | Load-switch input voltage; connect a 1 μ F or greater ceramic capacitor from IN to GND as close as possible to the IC. |
| GND | C1 | POWER | Ground connection. |
| EN | C2 | INPUT | Enable input, logic high turns on power switch. |
| OUT | A1, B1 | OUTPUT | Load-switch output; connect a 1 μ F ceramic capacitor from OUT to GND as close as possible to the IC is recommended. |

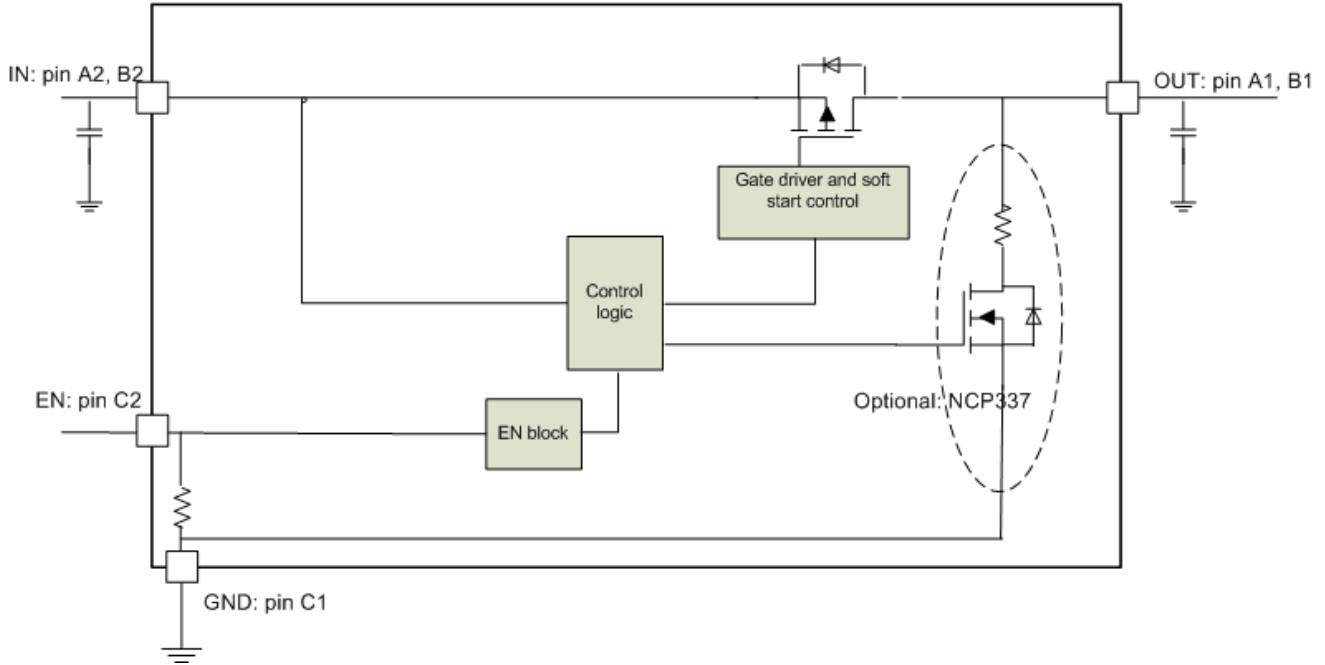


Figure 2. Block Diagram

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Table 2. MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|---------------------------|---------------|------|
| IN, OUT, EN, Pins: (Note 1) | V_{EN}, V_{IN}, V_{OUT} | -0.3 to + 7.0 | V |
| From IN to OUT Pins: Input/Output (Note 1) | V_{IN}, V_{OUT} | 0 to + 7.0 | V |
| Maximum Junction Temperature | T_J | -40 to + 125 | °C |
| Storage Temperature Range | T_{STG} | -40 to + 150 | °C |
| Moisture Sensitivity (Note 2) | MSL | Level 1 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------------|------------------------------------|-----------------------------|---------------|-----|------|------|---|
| V_{IN} | Operational Power Supply | | 1.2 | | 5.5 | V | |
| V_{EN} | Enable Voltage | | 0 | | 5.5 | | |
| T_A | Ambient Temperature Range | | -40 | 25 | +85 | °C | |
| T_J | Junction Temperature Range | | -40 | 25 | +125 | °C | |
| C_{IN} | Decoupling input capacitor | | 1 | | | μF | |
| C_{OUT} | Decoupling output capacitor | | 1 | | | μF | |
| $R_{\theta JA}$ | Thermal Resistance Junction to Air | WLCSP package (Note 3) | | 100 | | °C/W | |
| I_{OUT} | Maximum DC current | | | | 3 | A | |
| P_D | Power Dissipation Rating (Note 4) | $T_A \leq 25^\circ\text{C}$ | WLCSP package | | 0.66 | | W |
| | | $T_A = 85^\circ\text{C}$ | WLCSP package | | 0.26 | | W |

1. According to JEDEC standard JESD22-A108.
2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
3. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
4. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

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Table 4. ELECTRICAL CHARACTERISTIC Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} between 1.2 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---------------------|---|-------------------------|--|-----|-----|-----|------------------|
| POWER SWITCH | | | | | | | |
| R_{DSON} | Static drain-source on-state resistance | $V_{in} = 5.5\text{ V}$ | $I = 1\text{ A}$ (Note 5) | | 20 | 22 | $\text{m}\Omega$ |
| | | $V_{in} = 4.5\text{ V}$ | $I = 500\text{ mA}$ (Note 5) | | 21 | 25 | |
| | | $V_{in} = 3.3\text{ V}$ | $I = 500\text{ mA}$ (Note 5) | | 23 | 28 | |
| | | $V_{in} = 2.5\text{ V}$ | $I = 500\text{ mA}$ (Note 5) | | 28 | 35 | |
| | | $V_{in} = 1.8\text{ V}$ | $I = 250\text{ mA}$ (Note 5) | | 40 | 45 | |
| | | $V_{in} = 1.2\text{ V}$ | $T_A = 25^{\circ}\text{C}$, $I = 200\text{ mA}$ | | 95 | 120 | |
| R_{dis} | Output discharge path | $EN = \text{low}$ | | | 70 | 90 | Ω |
| V_{IH} | High-level input voltage | | | 0.9 | | | V |
| V_{IL} | Low-level input voltage | | | | | 0.5 | |
| R_{pd} | EN pull down resistor | | | | 5 | | $\text{M}\Omega$ |

QUIESCENT CURRENT

| | | | | | | | |
|-----------|-------------------|-------------------------|------------------------------|--|--|---|---------------|
| I_{std} | Standby current | $V_{in} = 4.2\text{ V}$ | $EN = \text{low}$, No load | | | 1 | μA |
| I_q | Quiescent current | $V_{in} = 4.2\text{ V}$ | $EN = \text{high}$, No load | | | 1 | μA |

TIMINGS

| | | | | | | | |
|----------|----------------------------|-------------------------------------|---|--|------|--|---------------|
| T_{EN} | Enable time | $V_{in} = 3.6\text{ V}$ (Note 6) | $R_L = 25\ \Omega$, $C_{out} = 1\ \mu\text{F}$ | | 323 | | μs |
| T_R | Output rise time | | $R_L = 25\ \Omega$, $C_{out} = 1\ \mu\text{F}$ | | 810 | | |
| T_{ON} | ON time ($T_{EN} + T_R$) | | $R_L = 25\ \Omega$, $C_{out} = 1\ \mu\text{F}$ | | 1130 | | |
| T_F | Output fall time | | NCP337. $R_L = 25\ \Omega$, $C_{out} = 1\ \mu\text{F}$ | | 42 | | |

5. Guaranteed by design and characterization

6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

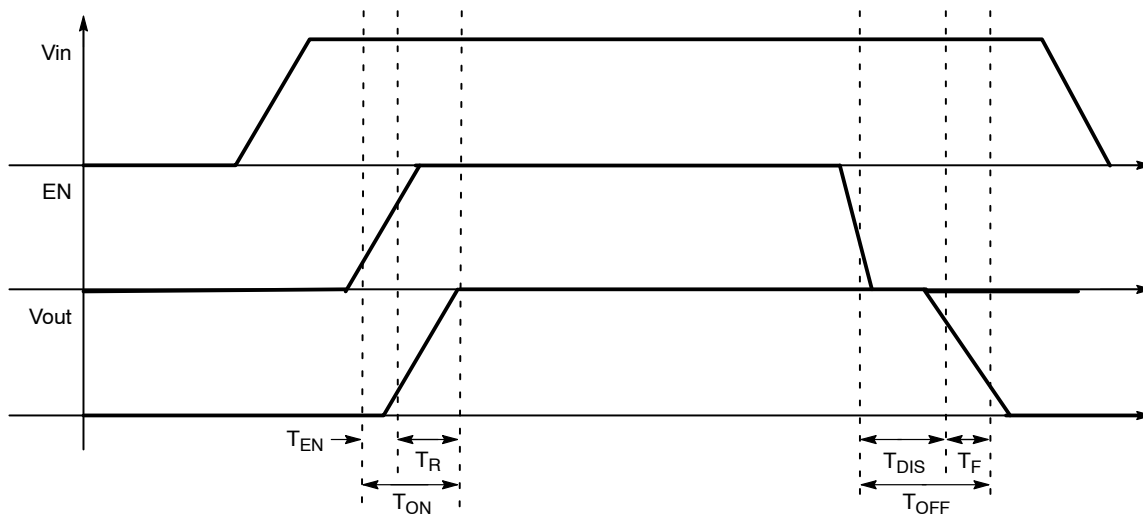


Figure 3. Enable, Rise and Fall Time

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TYPICAL CHARACTERISTICS

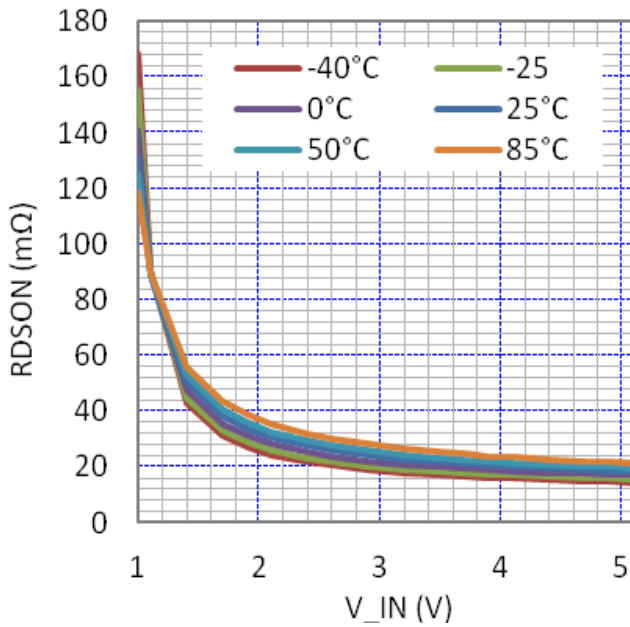


Figure 4. Rdson (mΩ) vs. Vin (V)

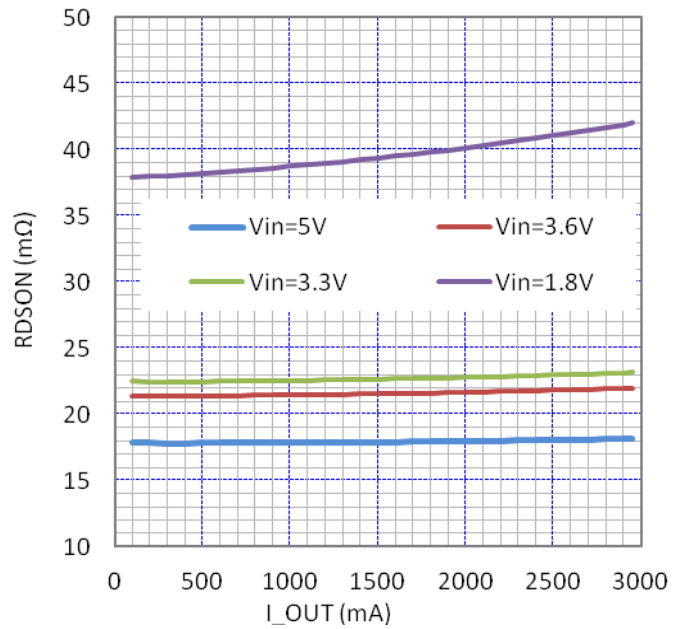


Figure 5. Rdson (mΩ) vs. Iload (A)

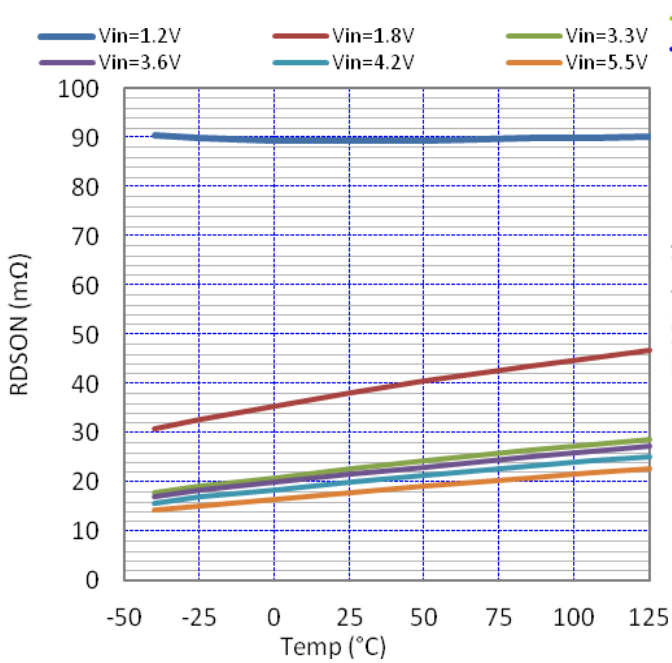


Figure 6. Rdson (mΩ) vs. Temperature (°C) at 100 mA

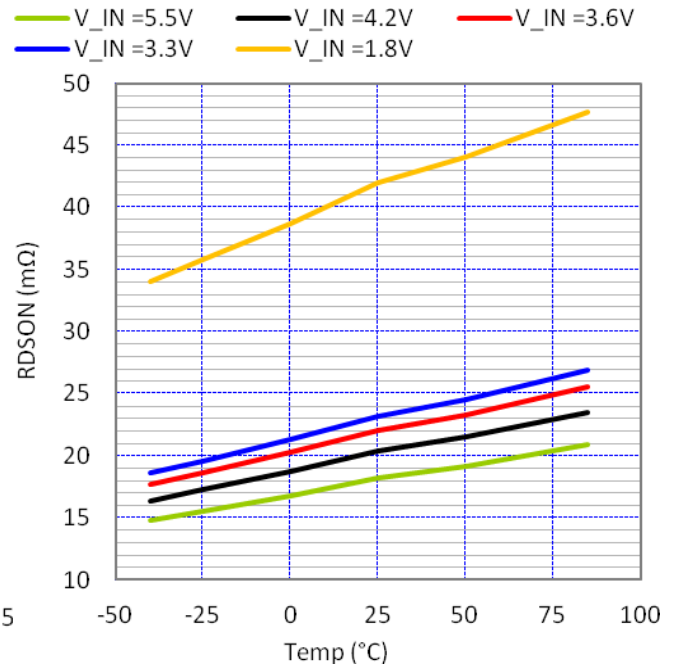


Figure 7. Rdson (mΩ) vs. Temperature (°C) at 3 A

TYPICAL CHARACTERISTICS

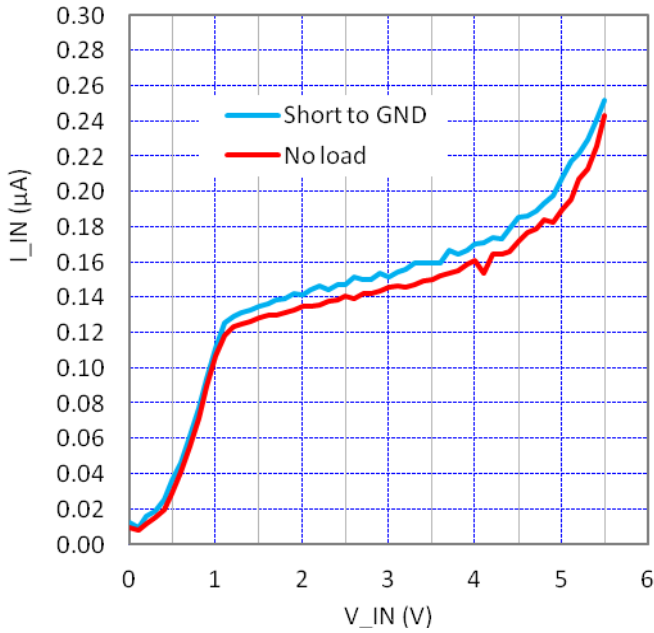


Figure 8. Standby (μA) and Leakage Current (μA) vs. V_{in} (V)

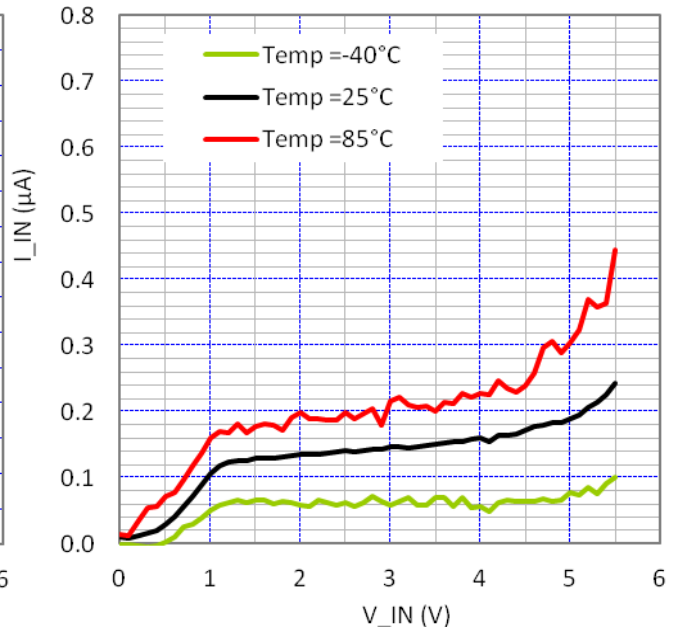


Figure 9. Standby Current (μA) vs. Temperature ($^{\circ}\text{C}$)

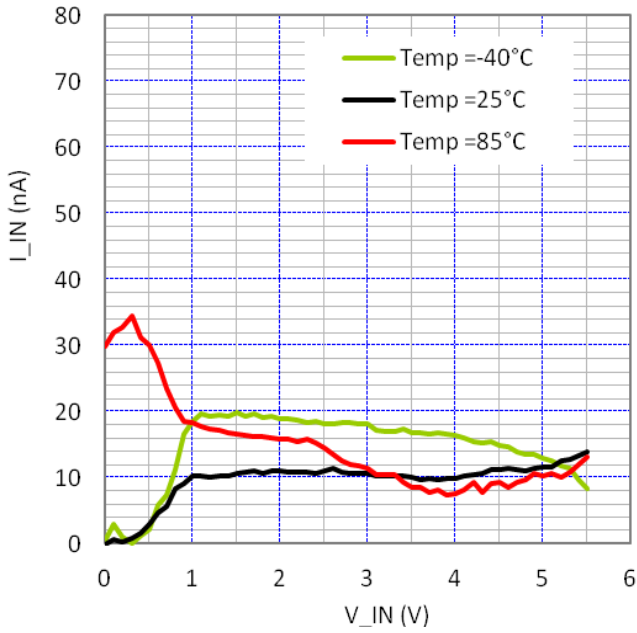


Figure 10. Leakage Current (μA) vs. Temperature ($^{\circ}\text{C}$)

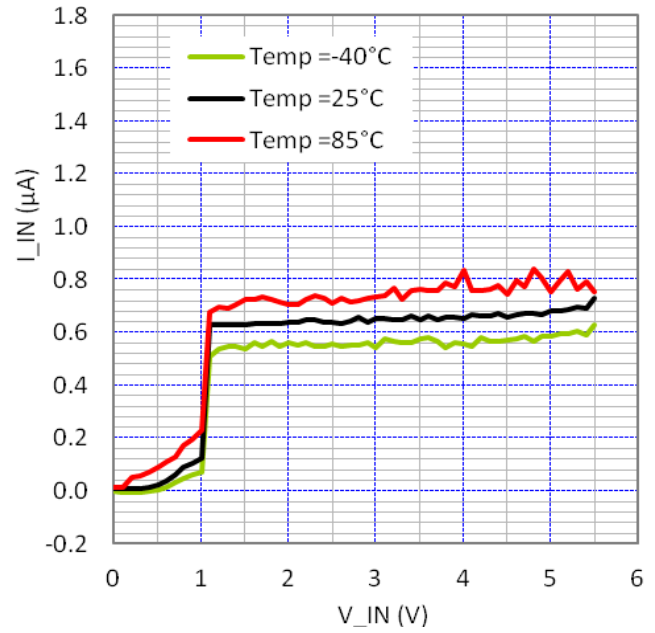


Figure 11. Quiescent Current (μA) vs. Temperature ($^{\circ}\text{C}$)

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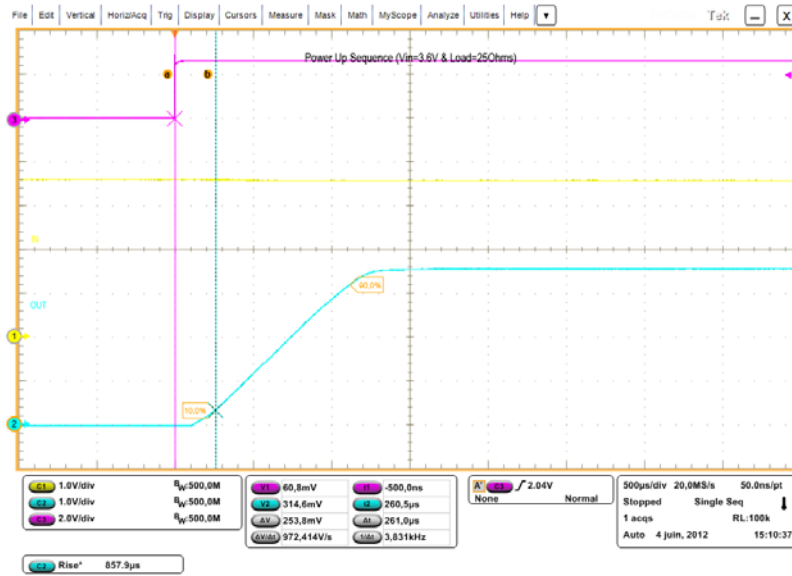


Figure 12. Enable Time and Rise Time

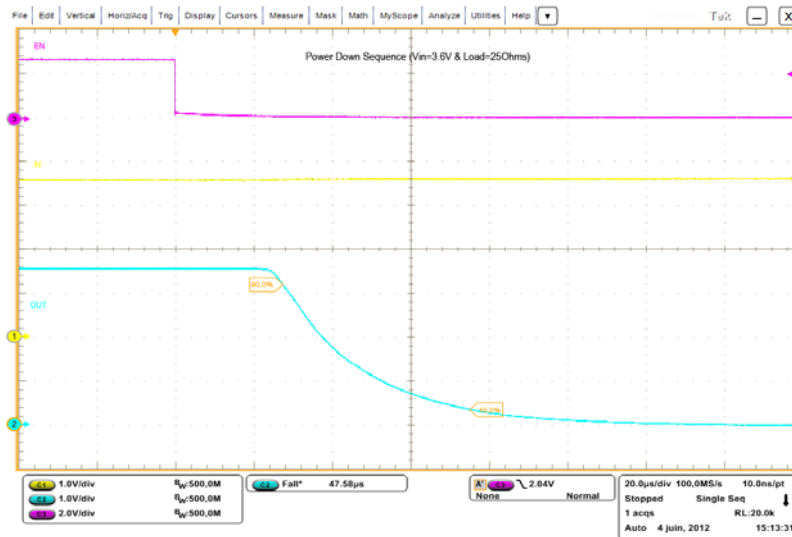


Figure 13. Disable Time and Fall Time

FUNCTIONAL DESCRIPTION

Overview

The NCP337 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.2 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of V_{in} of 1.2 V and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and $V_{in} > 1.2$ V.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at 70 Ω .

Cin and Cout Capacitors

IN and OUT, 1 μ F, at least, capacitors must be placed as close as possible the part to for stability improvement.

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APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

- $P_D = R_{DS(on)} \times (I_{OUT})^2$
 P_D = Power dissipation (W)
 $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
 I_{OUT} = Output current (A)

- $T_J = P_D \times R_{\theta JA} + T_A$
 T_J = Junction temperature ($^{\circ}\text{C}$)
 $R_{\theta JA}$ = Package thermal resistance ($^{\circ}\text{C}/\text{W}$)
 T_A = Ambient temperature ($^{\circ}\text{C}$)

PCB Recommendations

The NCP337 integrates an up to 3 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

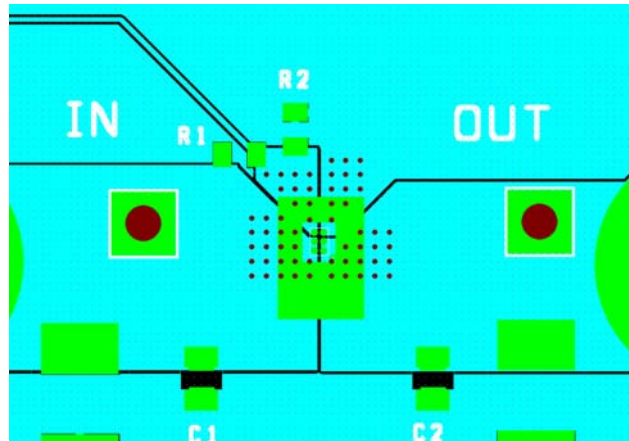


Figure 14. Routing Example: 2 oz, 4 layers with vias across 2 internal inners.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J : junction temperature.

T_A : ambient temperature.

R_{θ} = Thermal resistance between IC and air, through PCB.

$R_{DS(on)}$: intrinsic resistance of the IC Mosfet.

I: load DC current.

Taking into account of R_{θ} obtain with:

- 1 oz, 2 layers: 100 $^{\circ}\text{C}/\text{W}$.

At 3 A, 25 $^{\circ}\text{C}$ ambient temperature, $R_{DS(on)}$ 20 m Ω @ V_{in} 5 V, the junction temperature will be:

$$T_J = T_A + R_{\theta} \times P_D = 25 + (0.024 \times 3^2) \times 100 = 43^{\circ}\text{C}$$

Taking into account of R_{θ} obtain with:

- 2 oz, 4 layers: 60 $^{\circ}\text{C}/\text{W}$.

At 3 A, 65 $^{\circ}\text{C}$ ambient temperature, $R_{DS(on)}$ 24 m Ω @ V_{in} 5 V, the junction temperature will be:

$$T_J = T_A + R_{\theta} \times P_D = 65 + (0.024 \times 3^2) \times 60 = 78^{\circ}\text{C}$$

ORDERING INFORMATION

| Device | Marking | Option | Package | Shipping [†] |
|-------------|---------|-----------------------|------------------|-----------------------|
| NCP337FCT2G | AC | Auto discharge | WLCSP 1 x 1.5 mm | 3000 Tape / Reel |
| NCP336FCT2G | AF | Without Autodischarge | WLCSP 1 x 1.5 mm | 3000 Tape / Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

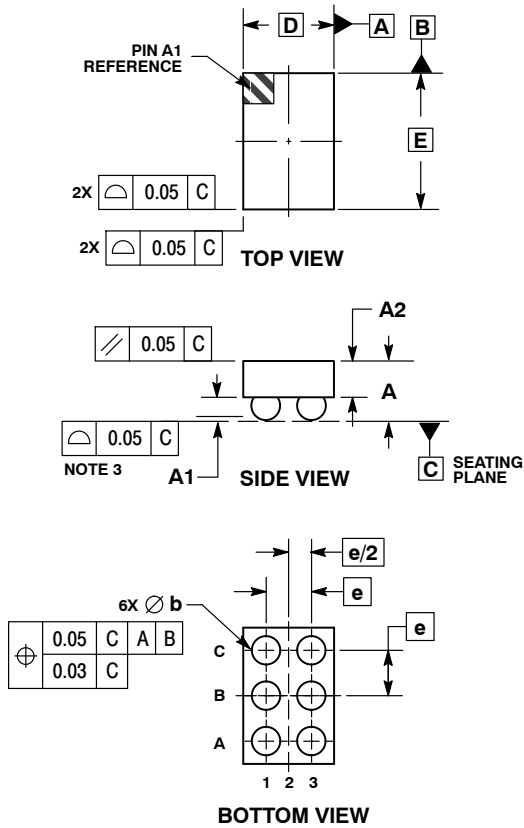
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SCALE 4:1

WLCSP6, 1.00x1.50
CASE 567FH
ISSUE O

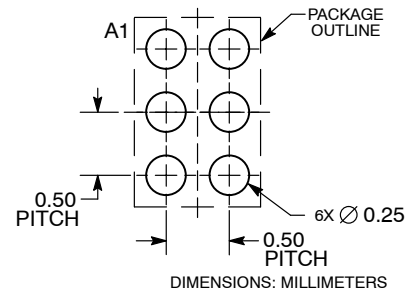
DATE 17 APR 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.54 | 0.63 |
| A1 | 0.22 | 0.28 |
| A2 | 0.33 | REF |
| b | 0.29 | 0.34 |
| D | 1.00 | BSC |
| E | 1.50 | BSC |
| e | 0.50 | BSC |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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