NCP372

Positive and Negative Overvoltage Protection Controller with Internal Low R_{on} NMOS FETs and Status FLAG

The NCP372 is able to disconnect systems from its output pin when wrong operating conditions are detected at it's input. The system is both positive and negative overvoltage protected up to ±28 V.

This device uses internal NMOS, and therefore, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP372 is able to instantaneously disconnect the output from the input, due to integrated Low R_{on} Power NMOS, if the input voltage exceeds the overvoltage threshold (OVLO) or undervoltage threshold (UVLO).

At powerup ($\overline{EN}$ pin = low level), the V_{out} turns on 30 ms after the V_{in} exceeds the undervoltage threshold.

The NCP372 provides a negative going flag ($\overline{FLAG}$) output, which alerts the system that a fault has occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1.0 μF or larger capacitor.

Features

- Overvoltage Protection up to 28 V
- Negative Voltage Protection down to −28 V
- Reverse Current Blocking
- On−Chip Low $R_{DS(on)}$ NMOS Transistor: Typical 130 mΩ
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Soft−Start
- Alert $\overline{FLAG}$ Output
- Shutdown $\overline{EN}$ Input
- Compliance to IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- 12 Lead LLGA 3x3 mm Package
- This is a Pb−Free and Halogen−Free Device

Applications

- Cell Phones
- Camera Phones
- Digital Still Cameras
- Personal Digital Assistant
- MP3 Players
- GPS

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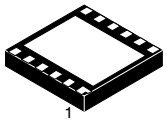
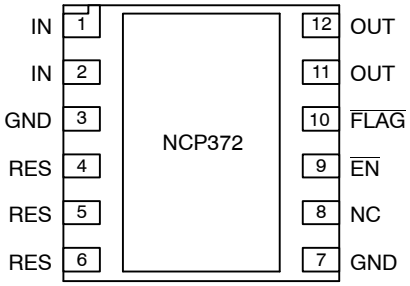


12 PIN LLGA
MU SUFFIX
CASE 513AK

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

TYPICAL APPLICATION CIRCUIT AND FUNCTIONAL BLOCK DIAGRAM

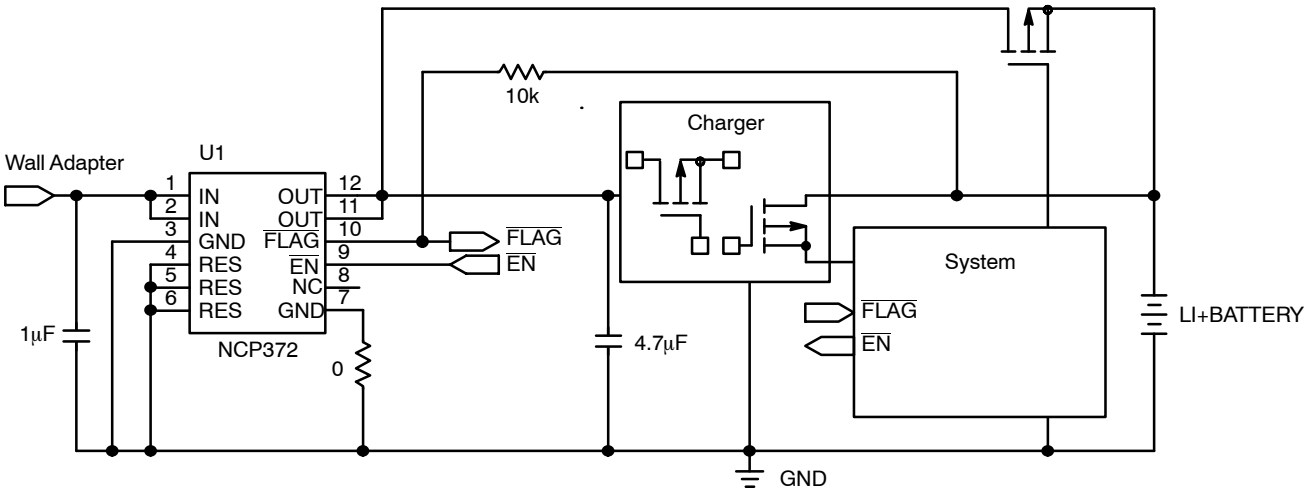


Figure 1. Typical Application Circuit

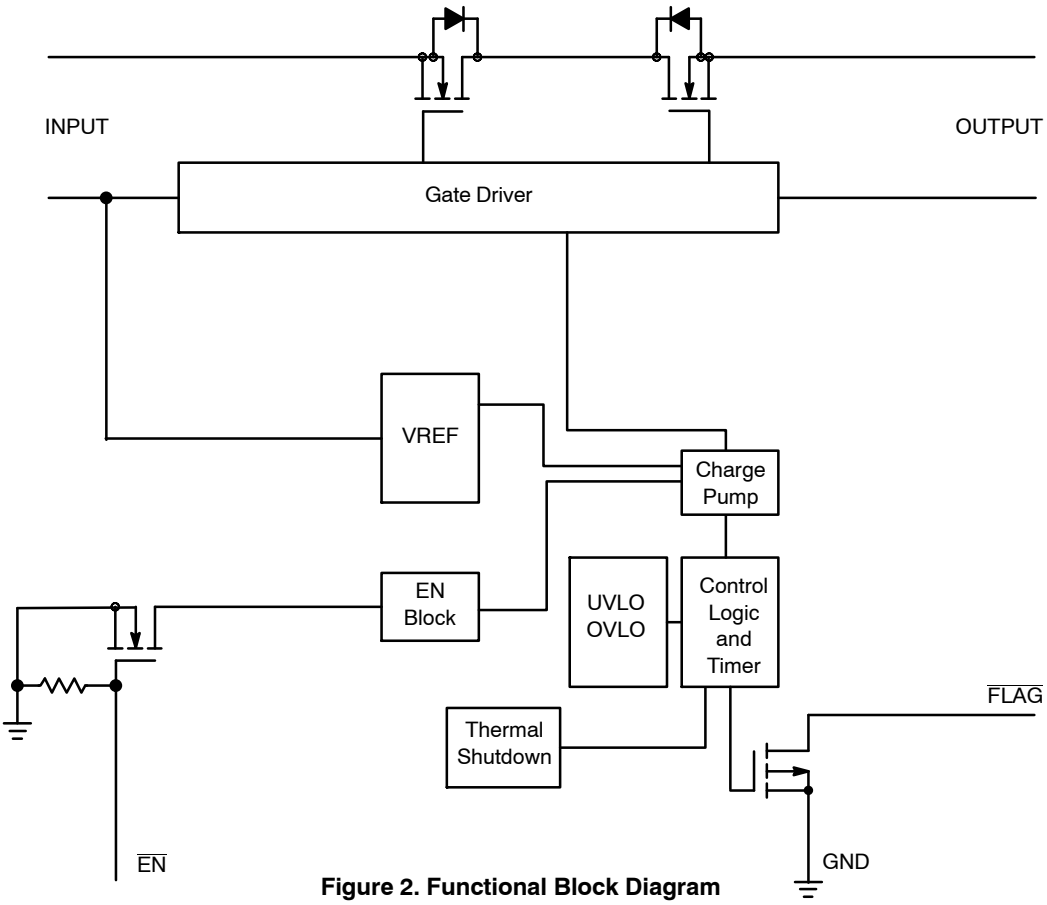


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
1, 2	IN	POWER	Input voltage pins. These pins are connected to the power supply. A 1 μF low ESR ceramic capacitor, or larger, must be connected between these pins and GND. The two IN pins must be hardwired to common supply.
3	GND	POWER	Main Ground
4	RES	INPUT	Reserved pin. This pin must be connected to GND.
5	RES	INPUT	Reserved pin. This pin must be connected to GND.
6	RES	INPUT	Reserved pin. This pin must be connected to GND.
7	GND	POWER	This pin must be directly hardwired to GND or through a pull down resistor with a 1 MΩ maximum value.
8	NC	NC	Not Connected
9	$\overline{EN}$	INPUT	Enable Pin. The device enters into shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND to a pull−down or to an I/O pin. This pin does not have an impact on the fault detection.
10	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect fault condition. The pin goes low when input voltage exceeds OVLO threshold, drops below UVLO threshold, or internal temperature exceeds thermal shutdown limit. Since the pin is open drain functionality, an external pull up resistor to VBat must be added (10 kΩ minimum value).
11,12	OUT	OUTPUT	Output Voltage Pin. This pin follows IN pins when “no input fault” is detected. The output is disconnected from the V_{IN} power supply when the input voltage is under the UVLO threshold or above OVLO threshold or thermal shutdown limit is exceeded.
13	PAD1	POWER	The PAD1 is used to dissipate the internal MOSFET thermal energy and must be soldered to an isolated PCB area. The area must not be connected to any potential other than a completely isolated one. See PCB Recommendations on page 10.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN to GND)	$Vmin_{in}$	−30	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{in}$	30	V
Maximum Voltage (OUT to GND)	$Vmax_{out}$	10	V
Maximum Voltage (All others to GND)	Vmax	7	V
Maximum DC Current	Imax	2.5	A
Thermal Resistance, Junction−to−Air, (Note 1)	$R_{\theta JA}$	200	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Junction Operating Temperature	T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2, (Note 2) Machine Model (MM) Model = B, (Note 3)	Vesd	15kV air, 8kV contact 2000V 200V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to PAD1). See PCB recommendation paragraph.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS (V_{in} = 5 V, Minimum/Maximum limits at −40°C < T_A < +85°C unless otherwise noted. Typical values are at T_A = +25°C)

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}	$\overline{EN}$ = low or high, V_{out} = 0 V	−28		28	V
Input Voltage	Vin_{min}	$\overline{EN}$ = low or high, V_{out} = 4.25V	−24			V
Undervoltage Lockout Threshold	UVLO	Vin falls below UVLO Threshold	2.6	2.7	2.8	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$	V_{in} rises above UVLO Threshold + $UVLO_{hyst}$	45	60	75	mV
Over voltage Lockout Threshold NCP372MUAITXG	OVLO	V_{in} rises above OVLO threshold	6.0	6.3	6.6	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$	V_{in} falls below to OVLO − $OVLO_{hyst}$	60	80	100	mV
V_{in} to V_{out} Resistance	$R_{DS(on)}$	V_{in} = 5 V, $\overline{EN}$ = low, Load Connected to V_{out} V_{in} = 5 V, $\overline{EN}$ = low, Load Connected to V_{out} @ 25°C		130 130	220 200	mΩ
Input Standby Current	Idd_{STD}	No Load. $\overline{EN}$ = high, V_{in} connected		90	170	μA
Input Supply Quiescent Current	Idd_{IN}	25°C Overtemperature Range		200	260 310	μA
$\overline{FLAG}$ Output Low Voltage	Vol_{flag}	1.2 V < V_{in} < UVLO Sink 50 μA on $\overline{FLAG}$ Pin		30	400	mV
		V_{in} > OVLO, Sink 1 mA on FLAG Pin			400	
$\overline{FLAG}$ Leakage Current	$\overline{FLAG}_{leak}$	$\overline{FLAG}$ Level = 5.5 V		1.0		nA
$\overline{EN}$ Voltage High	V_{ihEN}		1.2			V
$\overline{EN}$ Voltage Low	V_{ilEN}				0.55	V
$\overline{EN}$ Leakage Current	$\overline{EN}_{leak}$	V_{in} connected V_{in} disconnected		200 1.0		nA
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SDHYST}			30		°C
TIMINGS						
Start Up Delay	t_{on}	From V_{in} > UVLO to V_{out} ≥ 0.3 V	20	30	40	ms
$\overline{FLAG}$ Going Up Delay	t_{start}	From V_{out} > 0.3 V to $\overline{FLAG}$ = 1.2 V	20	30	40	ms
Turn Off Delay	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V V_{in} Increasing from 5 V to 8 V at 3 V/μs		1.5	5.0	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG}$ ≤ 0.4 V See Figure 3 and 9 V_{in} Increasing from 5 V to 8 V at 3 V/μs		1.5		μs
Disable Time	t_{dis}	$\overline{EN}$ = 0.4 V to 1.2 V to V_{out} ≤ 0.3 V		2.5		μs

NOTE: Electrical parameters are guaranteed by correlation across the full range of temperature.

TIMING DIAGRAMS

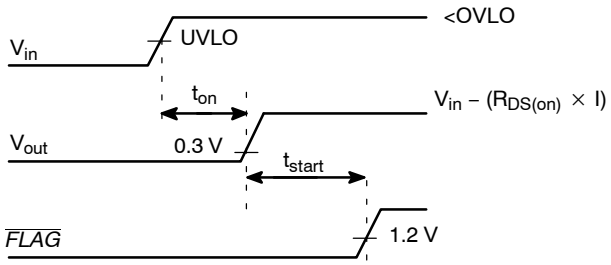


Figure 3. Startup

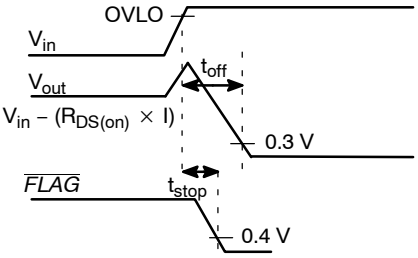


Figure 4. Shutdown on Overvoltage Detection

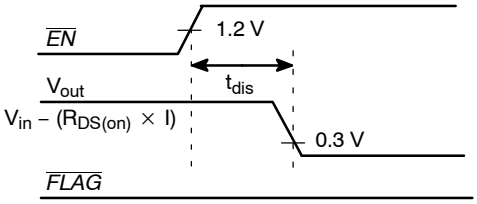


Figure 5. Disable on $\overline{EN}$ = 1

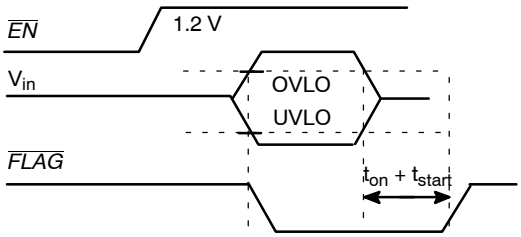


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

TYPICAL OPERATING CHARACTERISTICS

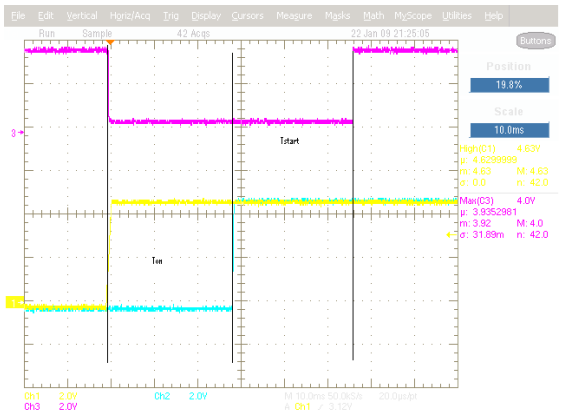


Figure 7. t_{on}, t_{start}, $\overline{EN}$ = low (10 ms/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$)

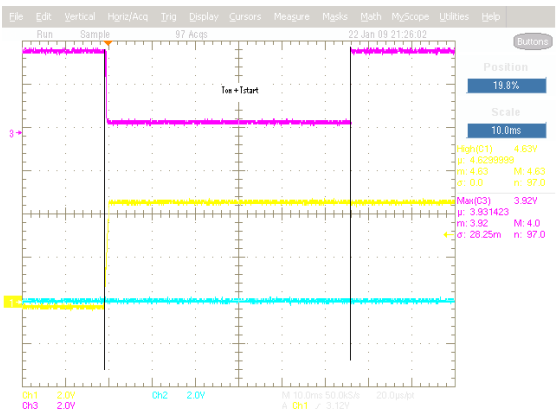


Figure 8. t_{start}, $\overline{EN}$ = low (10 ms/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$)

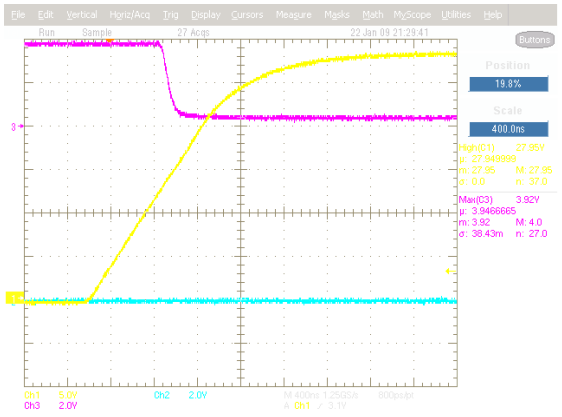


Figure 9. V_{in} rise to fault (400 ns/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$)

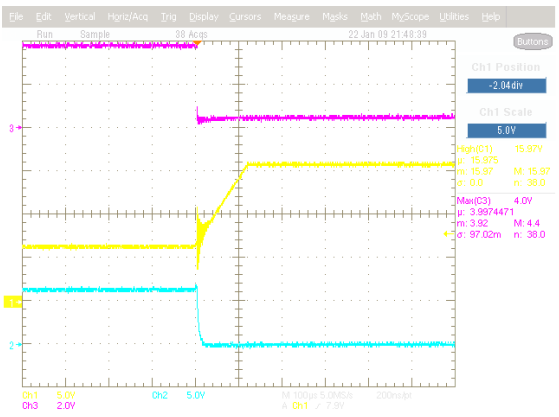


Figure 10. V_{in} rise to fault (100 µs/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$)

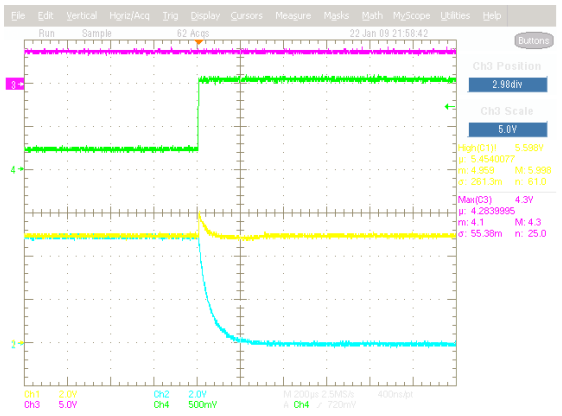


Figure 11. Disable time (200 µs/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$, Ch4: $\overline{EN}$)

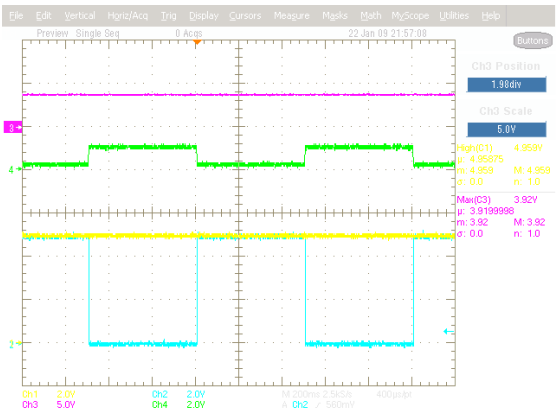


Figure 12. $\overline{EN}$ on & off (200 ms/div, Ch1: V_{in}, Ch2: V_{out}, Ch3: $\overline{FLAG}$, Ch4: $\overline{EN}$)

TYPICAL OPERATING CHARACTERISTICS

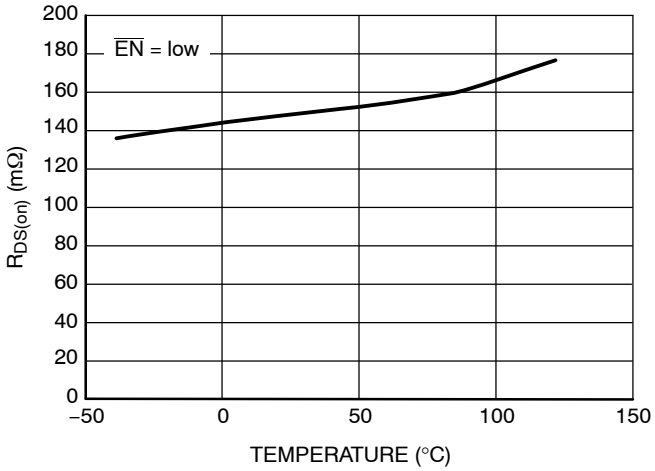


Figure 13. $R_{DS(on)}$ vs. Temperature

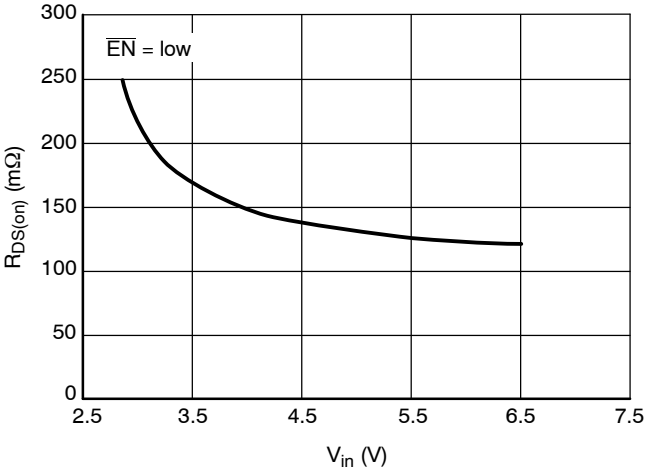


Figure 14. $R_{DS(on)}$ vs. V_{in}

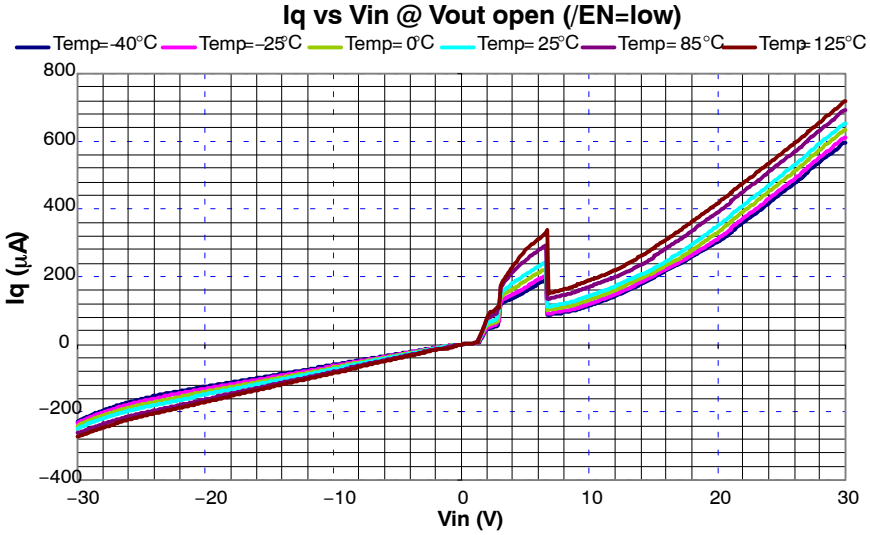


Figure 15. Quiescent Current vs. V_{in} from −30 V to +30 V, Enable Mode

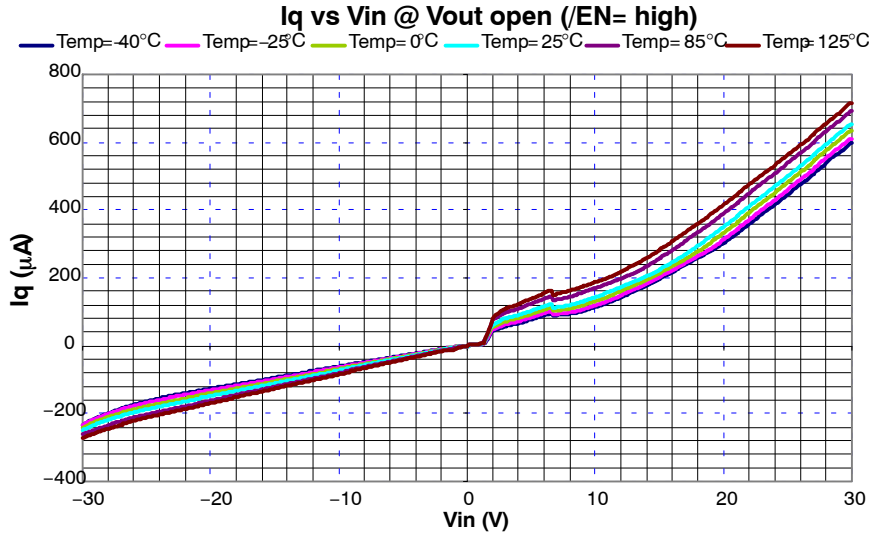


Figure 16. Quiescent Current vs. V_{in} from −30 V to +30 V, Disable Mode

Operation

The NCP372 provides overvoltage protection for positive and negative voltages, up to 28 V or down to −28 V. The negative protection is ensured by an internal Low $R_{DS(on)}$ NMOS FET. A second internal Low $R_{DS(on)}$ NMOS FET protects the systems (i.e.: charger) connected on the V_{out} pin, against positive overvoltage. At powerup, with $\overline{EN}$ pin = low, the output rises t_{on} seconds after the input overtakes the undervoltage UVLO (Figure 3). The NCP372 provides a $\overline{FLAG}$ output, which alerts the system that a fault has occurred. The $\overline{FLAG}$ signal rises t_{start} seconds after the output signal rises. $\overline{FLAG}$ pin is an open drain output.

Undervoltage Lockout (UVLO)

To ensure proper operation under any condition, the device has a built−in undervoltage lockout (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is 2.7 V nominal. The $\overline{FLAG}$ output remains low as long as V_{in} does not reach UVLO threshold. This circuit has a built in hysteresis to provide noise immunity to transient conditions.

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lockout (OVLO) circuit. During overvoltage condition, the output remains disabled until the input voltage exceeds 6.3 V.

$\overline{FLAG}$ output remains low until V_{in} is higher than OVLO. This circuit has a built in hysteresis to provide noise immunity to transient conditions.

$\overline{FLAG}$ Output

The NCP372 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin goes low as soon the OVLO threshold is exceeded or when the V_{in} level is below the UVLO threshold. When V_{in} level recovers normal condition, $\overline{FLAG}$ goes high, after t_{start} delay following the output response. The pin is an open drain output, thus a pullup resistor (typically 1.0 MΩ, minimum 10 kΩ) must be provided to V_{CC}. The $\overline{FLAG}$ level always reflects V_{in} status, even if the device is turned off ($\overline{EN}$ = 1).

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced low or connected to ground. A high level on the pin, disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Negative Voltage and Reverse Current

The built−in NMOS protects the downstream system from negative voltages occurring on IN pin down to −28 V. The same NMOS avoids reverse currents that could discharge the battery.

When a fault occurs, the output is disconnected from IN pin and $\overline{FLAG}$ goes low.

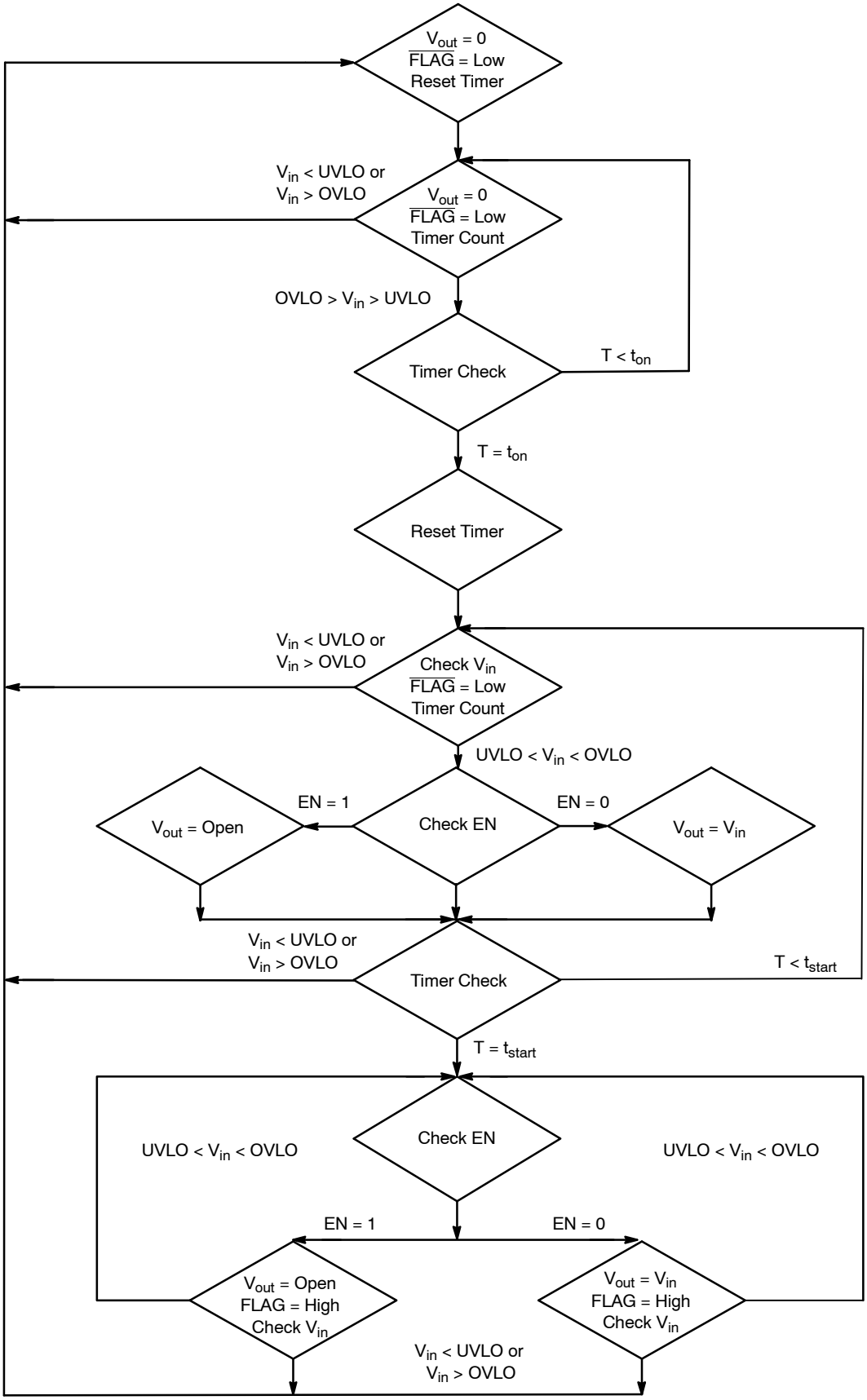


Figure 17. State Machine

Thermal Shutdown protection

In case of internal overheating, the integrated thermal shutdown protection turns off the internal MOSFETs in order to instantaneously decrease the device temperature. The thermal threshold has been set at 150°C $\overline{\text{FLAG}}$ then goes low to inform the MCU.

As the thermal hysteresis is 30°C, the MOSFETs will turn on as soon the device temperature falls below 120°C.

If the fault event is still present, the temperature increase engages the thermal shutdown again until the fault event disappears.

PCB Recommendations

Since the NCP372 integrates 2.5 A N−MOSFETs, PCB rules must be respected to properly evacuate the heat out of the silicon.

From an applications standpoint, PAD1 of the NCP372 package should be connected to an isolated PCB area to increase the heat transfer if necessary.

In any case, PAD1 should be not connected to any other potential or GND other than the isolated extra copper surface.

To assist in the design of the transfer plane connected to PAD1, Figure 18 shows the copper area required with respect to $R_{\theta JA}$.

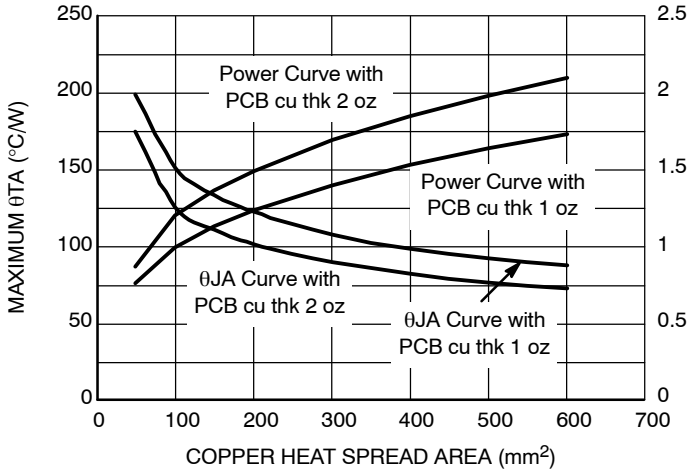


Figure 18. Copper heat Spread Area

ESD Tests

The NCP372 conforms to the IEC61000−4−2, level 4 on the Input pin. A 1 μF (I.E Murata GRM188R61E105KA12D) must be placed close to the IN pins. If the IEC61000−4−2 is not a requirement, a 100 nF/25 V must be placed between IN and GND.

The above configuration supports 15 kV (Air) and 8 kV (Contact) at the input per IEC61000−4−2 (level 4).

Please refer to Figure 19 for the IEC61000−4−2 electrostatic discharge waveform.

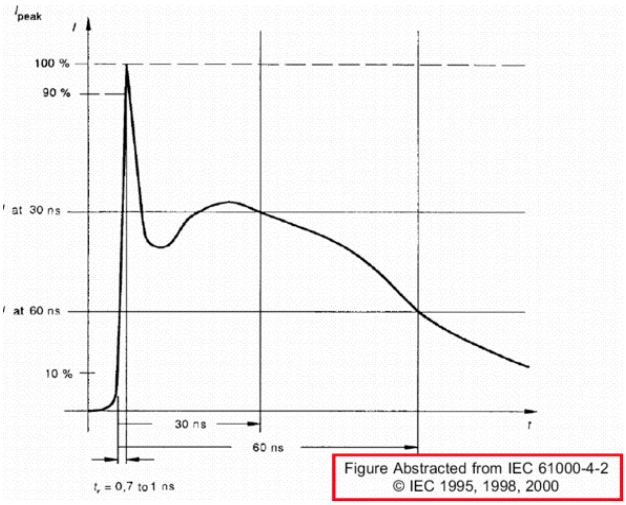


Figure 19. I_{peak} = f(t)/IEC61000−4−2

$R_{DS(on)}$ and Dropout

The NCP372 includes two internal low $R_{DS(on)}$ N−MOSFETs to protect the system, connected on OUT pin, from overvoltage, negative voltage and reverse current protection. During normal operation, the $R_{DS(on)}$ characteristics of the N−MOSFETs give rise to low losses on V_{out} pin.

As example: R_{load} = 8 Ω, Vin= 5 V. $R_{DS(on)}$ = 155 mΩ. I_{out} = 800 mA.

V_{out} = 4.905 V

NMOS Losses = $R_{DS(on)}$ x I_{out}^2 = 0.155 x 0.8^2 = 0.0992 W

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP372MUAITXG	NCAI 372	LLGA12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SELECTION GUIDE

The NCP372 can be available in several undervoltage and overvoltage options. Part number is designated as follows:

NCP372MUxxTxG

a b c d

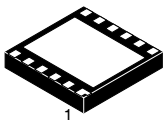
Code	Contents
a	UVLO Typical Threshold a: A = 2.7 V
b	OVLO Typical Threshold b: I = 6.3 V
c	Tape & Reel Type c: X = 3000
d	d: G = Pb−Free

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

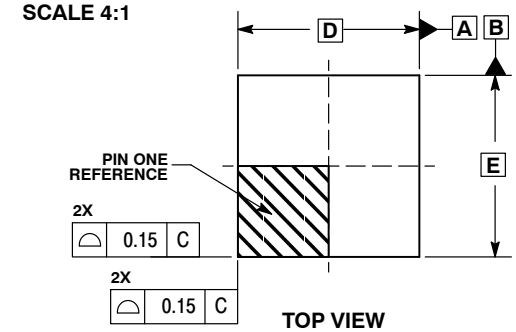
ON Semiconductor®

LLGA12 3x3, 0.5P
CASE 513AK−01
ISSUE O

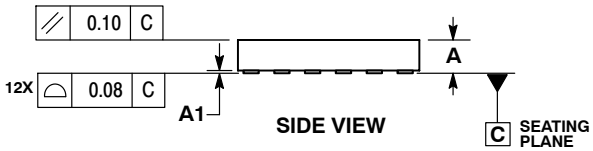
DATE 28 JUN 2007



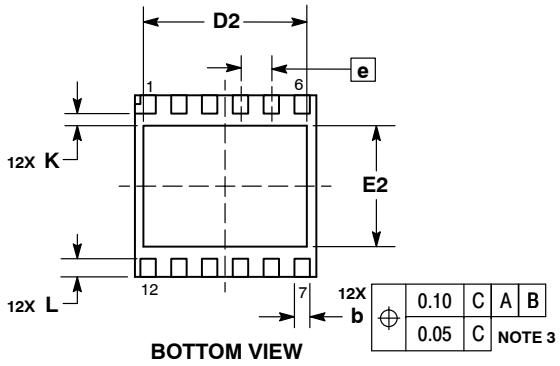
SCALE 4:1



TOP VIEW



SIDE VIEW

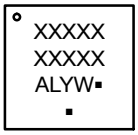


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.60	2.80
E	3.00 BSC	
E2	1.90	2.10
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

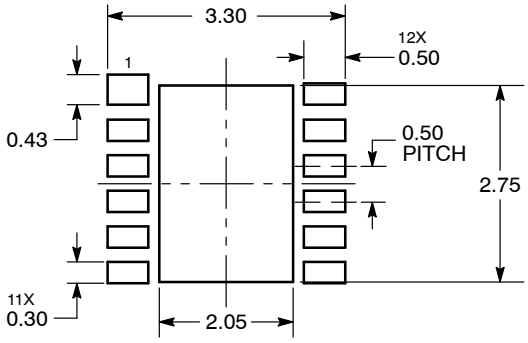
GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**12 PIN LLGA, 3 X 3 X 0.55T, 0.5P**	**PAGE 1 OF 1**

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