NCP392B

Adjustable Front End Overvoltage Protection Controller with Protected Vbus Output

The NCP392B is an overvoltage front end protection and be able to disconnect the systems from its output pin in case wrong input operating conditions are detected, up to +28 V. Due to this device using internal NMOS, no external device is necessary, reducing the system cost and the PCB area of the application board.

Internal OVLO threshold is available, or can be adjusted if external resistor bridge is used (A version).

At power up ($\overline{EN}$ pin = low level), the Vout turns on tstart time after internal timer elapsed.

Additional timer option is available in the B version for OTG supporting.

A LDO, internally connected on IN pin, provided a protected output voltage even if an over voltage is present on IN pin.

Features

- Over−voltage Protection Up to + 28 V
- On−chip Low $R_{DS(on)}$ NMOS Transistors: Typical 34 mΩ
- Over−voltage Lockout (OVLO)
- Externally Adjustable OVLO (A Version)
- Protected VBUS Indicator Output VBUS_DET
- Internal 15 ms Startup Delay
- 100 ms Start Up Delay Option (B Version)
- Shutdown $\overline{EN}$ Input
- + 100 V Surge Capability, in Compliance with IEC61000−4−5 Standard
- Compliance to IEC61000−4−2 (Level 4)
  - 8 kV (Contact)
  - 15 kV (Air)
- ESD Ratings:
  - Machine Model = B (200 V)
  - Human Body Model = 2 (2 kV)
- CSP−12 package 1.3 x 2.0 mm, 0.4 mm Pitch
- This is a Pb−Free Device

Typical Applications

- Cell Phones
- Tablets
- Camera Phones
- Digital Still Cameras
- Personal Digital Applications

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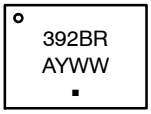
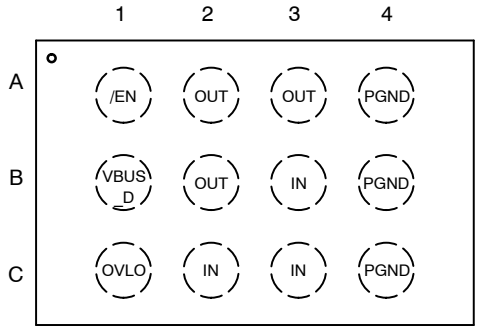
WLCSP 12
FCC SUFFIX
CASE 567JM

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

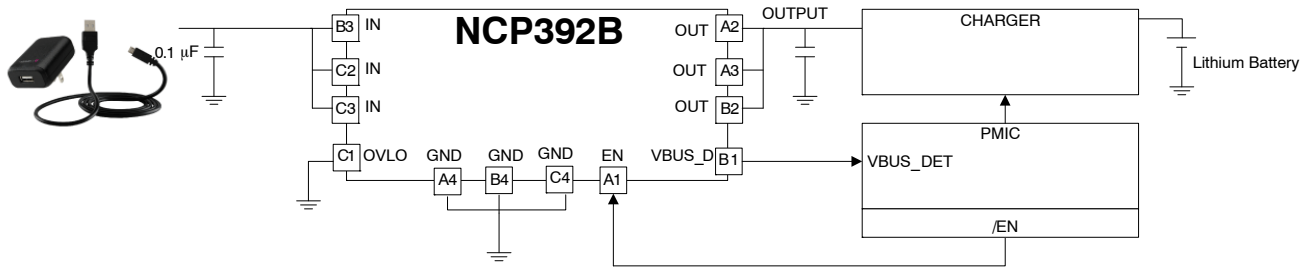


Figure 1. Typical Application Circuit: NCP392B with Adjustable OVLO

FUNCTIONAL BLOCK DIAGRAM

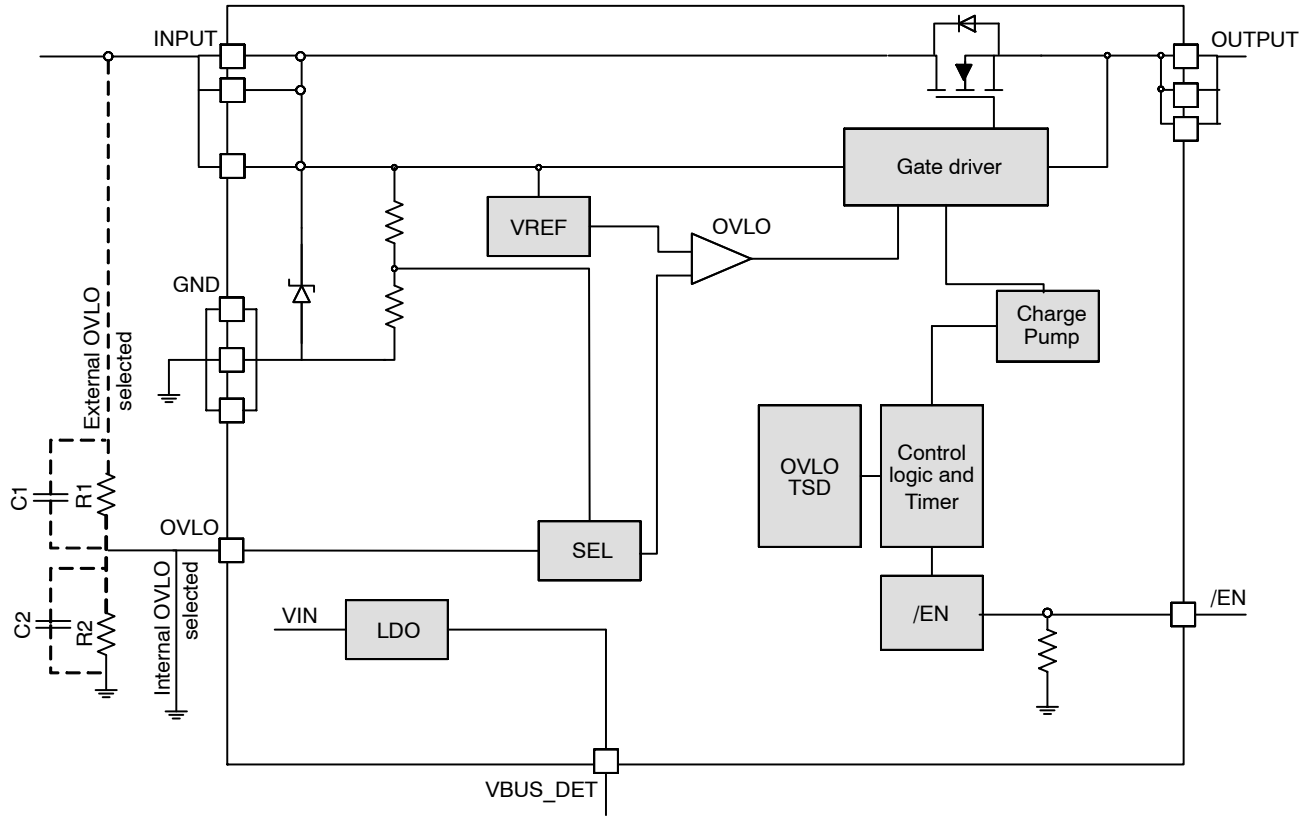
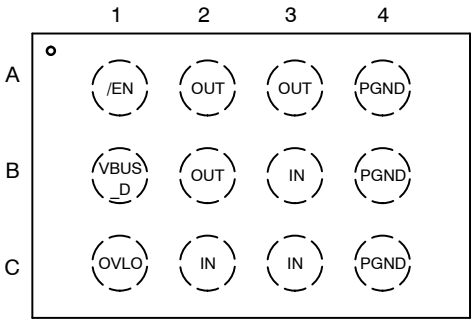


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION



(Top View)

Figure 3. Pinout

Table 1. NCP392 PIN DESCRIPTION

Pin	Pin Name	Type	Description
A1	$\overline{EN}$	I/O	Enable pin bar. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin is tied low with internal pull down. This pin does not have an impact on the VBUS_DET.
A2, A3, B2	OUT	OUTPUT	Output voltage pins. These pins follow IN pins, with debounce time, when “no fault” are detected. The outputs are disconnected from the Vin power supply when the input voltage is below UVLO, above OVLO threshold or internal thermal protection is exceeded. The three OUT pins must be hardwired together and used for power dissipation.
A4, B4, C4	PGND	POWER	Ground. The three GND pins must be hardwired together and connect to the system GND.
B1	VBUS_DET	OUTPUT	Vbus detect pin. This pin reflects Vin pin, and be in pass through mode up to regulation level. Upper this trip, this output regulates IN voltage whatever OVLO event or /EN setting.
B3, C2, C3	IN	POWER	Input voltage pins. These pins are connected to the power supply. The three IN pins must be hardwired together.
C1	OVLO	INPUT	External OVLO Adjustment. Connect external resistor bridge to OVLO pin to select a different OVLO threshold. Connect OVLO pin to GND if not used. In this case internal OVLO will be selected.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage (IN, OVLO to GND)	$Vmin_{IN}$	−0.3	V
Minimum Voltage (All others to GND)	Vmin	−0.3	V
Maximum Voltage (IN to GND)	$Vmax_{IN}$	29	V
Maximum Voltage (OVLO to GND)	$Vmax_{OVLO}$	14	V
Maximum Voltage (OUT to GND)	$Vmax_{OUT}$	22	V
Maximum Voltage (VBUS_DET to GND)	$Vmax_{VBUS}$	10	V
Maximum Voltage (All others to GND)	Vmax	7	V
Maximum DC current	Imax	4.5	A
Peak input current	Ipeak	8	A
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	70	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Operating temperature	T_J	+ 125	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), model = 2 (Note 1) Machine Model (MM) model = B (Note 2)	V_{esd}	15 kV air, 8 kV contact 2000 V 200 V	kV V V
Moisture Sensitivity	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
2. Machine Model, 200 pF discharged through all pins following specification JESD22/A115

Table 3. ELECTRICAL CHARACTERISTICS

Min / Max limits values (−40°C < T_A < +85°C and T_J = 125°C) and V_{in} = +5 V (Unless otherwise noted). Typical values are T_A = +25°C.

Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}, V_{OVLO}		2.8		28	V
Under voltage Lockout	UVLO	V_{in} rising			2.8	V
Under voltage Lockout hysteresis	$UVLO_{hyst}$	V_{in} falling	40	60	80	mV
Internal Over voltage Lockout threshold NCP392BR	OVLO	V_{in} rising (Note 3) OVLO pin tied to GND 25°C	5.9	5.95	6	V
Internal Over voltage Lockout hysteresis	$OVLO_{hyst}$	V_{in} falling	1.5		2.5	%
External OVLO Reference	$OVLO_{EXT}$		1.18	1.221	1.26	V
External Adjustable OVLO			4		20	V
Over−Voltage Lockout Hysteresis	$OVLO_{EXThyst}$	V_{in} falling		2		%
External OVLO select	$OVLO_{SEL}$		0.2		0.3	V
Vin versus Vout Resistance	R_{DSon}	V_{in} = 5 V, /EN = GND, −40°C < T_J < 125°C		34	50	mΩ
Supply Quiescent Current	Idd	No load. /EN = 0.4 V		90	200	μA
Standby Current	Istb	No load. /EN = 1.2 V, No load on VBUS_DET			150	μA
OVLO select leakage	I_{OVLO}				100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Please contact your ON Semiconductor representative for additional OVLO threshold.
   Electrical parameters are guaranteed by correlation across the full range of temperature.

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Characteristics	Symbols	Conditions	Min	Typ	Max	Unit
VBUS_DET (A Version)						
VBUS_DET Regulation	$VBUS_{THRES}$	V_{in} > $VBUS_{THRES}$	6.5		9	V
VBUS_DET Pass Through		V_{in} < $VBUS_{THRES}$, I load 1 mA	V_{in} − 0.2		V_{in}	V
VBUS_DET ron	LDO_{RON}			60		Ω
VBUS_DET Current				1.5		mA
LOGIC						
$\overline{EN}$ Voltage High	Vih		1.2			V
$\overline{EN}$ Voltage Low	Vil				0.4	V
$\overline{EN}$ Pull−down	EN_{pd}			100		kΩ
TIMINGS						
Start up Time	t_{START}	From V_{in} > 2.8 V to 10% V_{out}, /EN low		15		ms
Enable time	t_{EN}	V_{in} present, From /EN high to low, 10% V_{out}		15		ms
Soft start	t_{RISE}	From 10% to 90% of V_{out}, C load 100 μF, Rload, 100 Ω, /EN low		1		ms
VBUS_DET rise time	t_{VBUS}	/EN low, From Vin applied to 90% VBUS_DET, 4.7 μF load		3.5	5.5	ms
Turn off time	t_{OFF}	Surge off time		100		ns
Disable time	t_{DIS}	From EN >1.2 V to 90% V_{out}. No load		20		μs
OVLO turn off time	t_{OVLO}	V_{in} rising 2 V/μs		1.5		μs
TSD						
Thermal shutdown	TSD			140		°C
Thermal shutdown rearming	TSD rearm			115		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Please contact your ON Semiconductor representative for additional OVLO threshold.
   Electrical parameters are guaranteed by correlation across the full range of temperature.

Operation

The NCP392B provides over−voltage protection for positive voltage surge, up to +28 V. An additional clamp, between IN and GND, protects the part against surge test, following IEC 61000−4−5 standard. A protected VBUS_DET output pin provides a secondary supply for the platform biasing.

Under−voltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in under−voltage lock out (UVLO) circuit. This circuit has a built−in hysteresis to provide noise immunity to transient conditions.

Over−voltage Lockout (OVLO)

To protect connected systems on Vout pin from over−voltage, the device has a built−in over−voltage lock out (OVLO) circuit. During over−voltage condition, the output remains disabled until the input voltage is above OVLO − hysteresis.

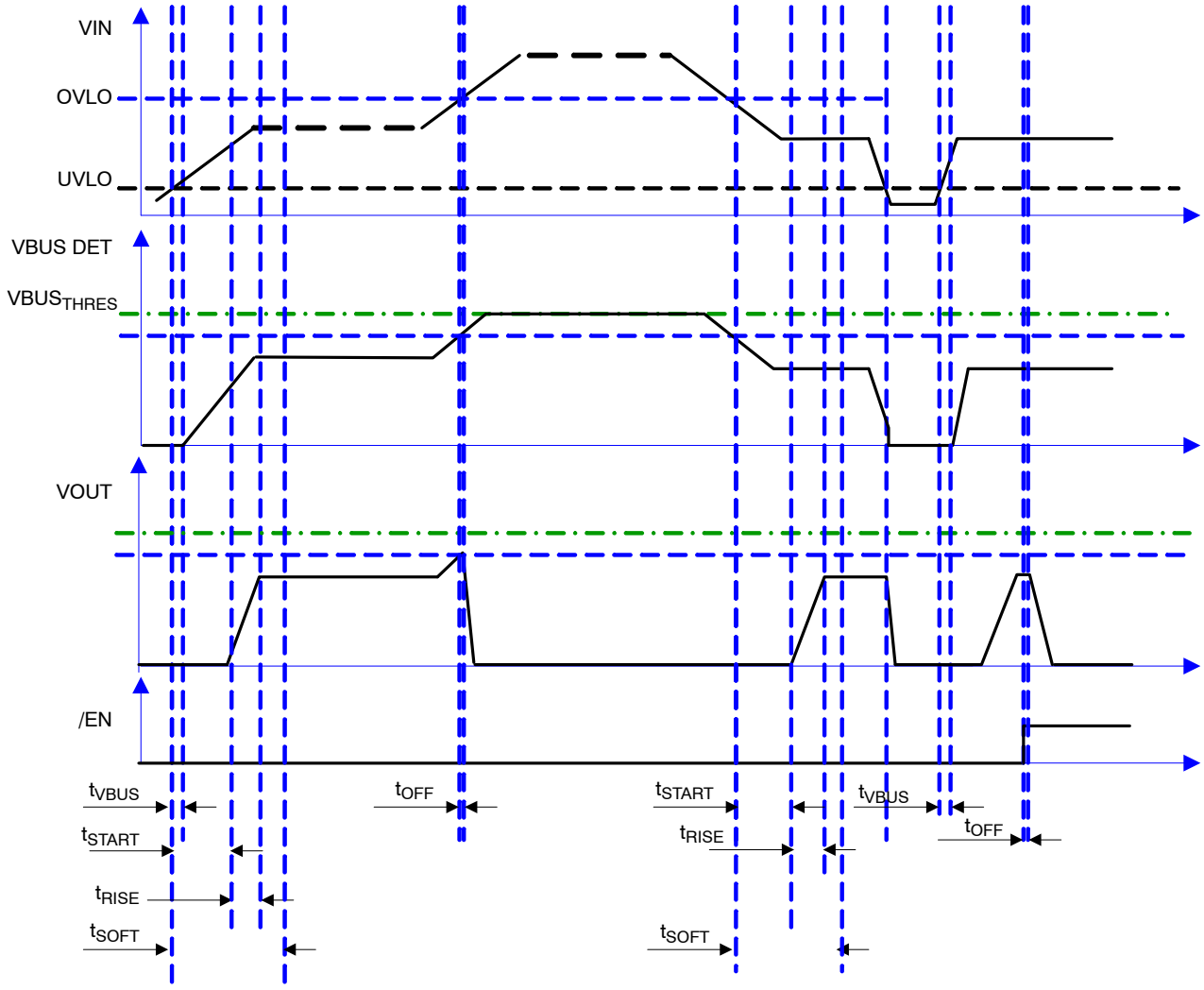


Figure 4. UVLO, OVLO and /EN Functionality

To select the internal OVLO threshold, the OVLO pin must be externally tied to GND.

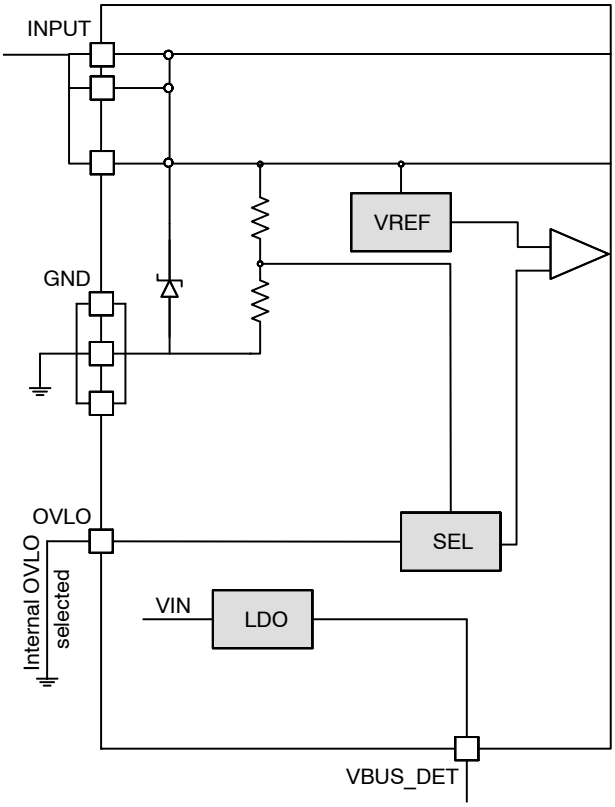


Figure 5. External Connection to GND of OVLO

If OVLO pin is not grounded, and by adding external bridge resistor on OVLO pin, between IN and GND, overvoltage protection can be adjusted as following:

$$NEW\_OVLO_{TH} = \frac{OVLO_{EXT} \times (R_1 + R_2)}{R_2} \quad \text{(eq. 1)}$$

With: $OVLO_{EXT}$ = 1.221 V Typical (OVLO External Reference)

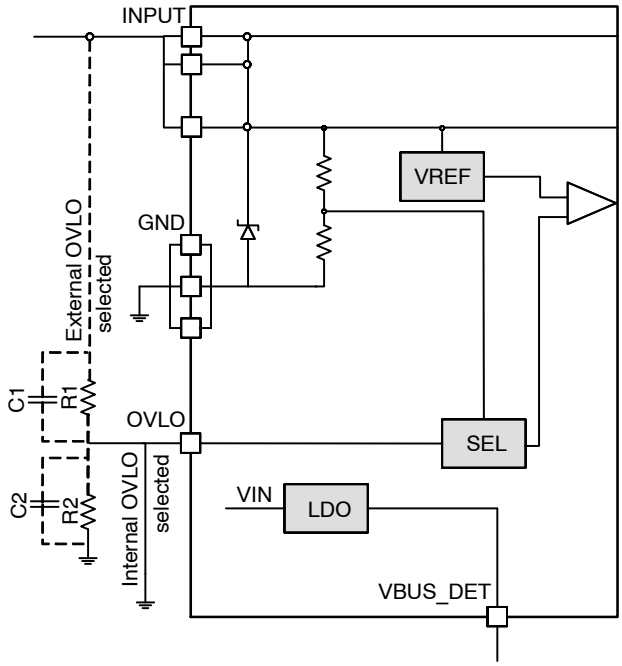


Figure 6. External Connection to Resistor Bridge of OVLO

Example:
NEW_OVLO_{TH} target 12 V.

(eq. 2)

$$R1 = R2 \times \left(\frac{OVLO}{1.221} - 1\right) = R2 \times \left(\frac{12}{1.221} - 1\right) = 8.828 \times R2$$

Taking into account external input bridge doesn't have excessive current consumption, and 1% is recommended:

R2 arbitrarily fixed at 1.05 MΩ.
R1 = 9.269 MΩ (9.31 MΩ standard value)
Obtained typical OVLO = 12.04 V

C_1 and C_2 should be selected in such a way that the time constant $R_1C_1 = R_2C_2$.

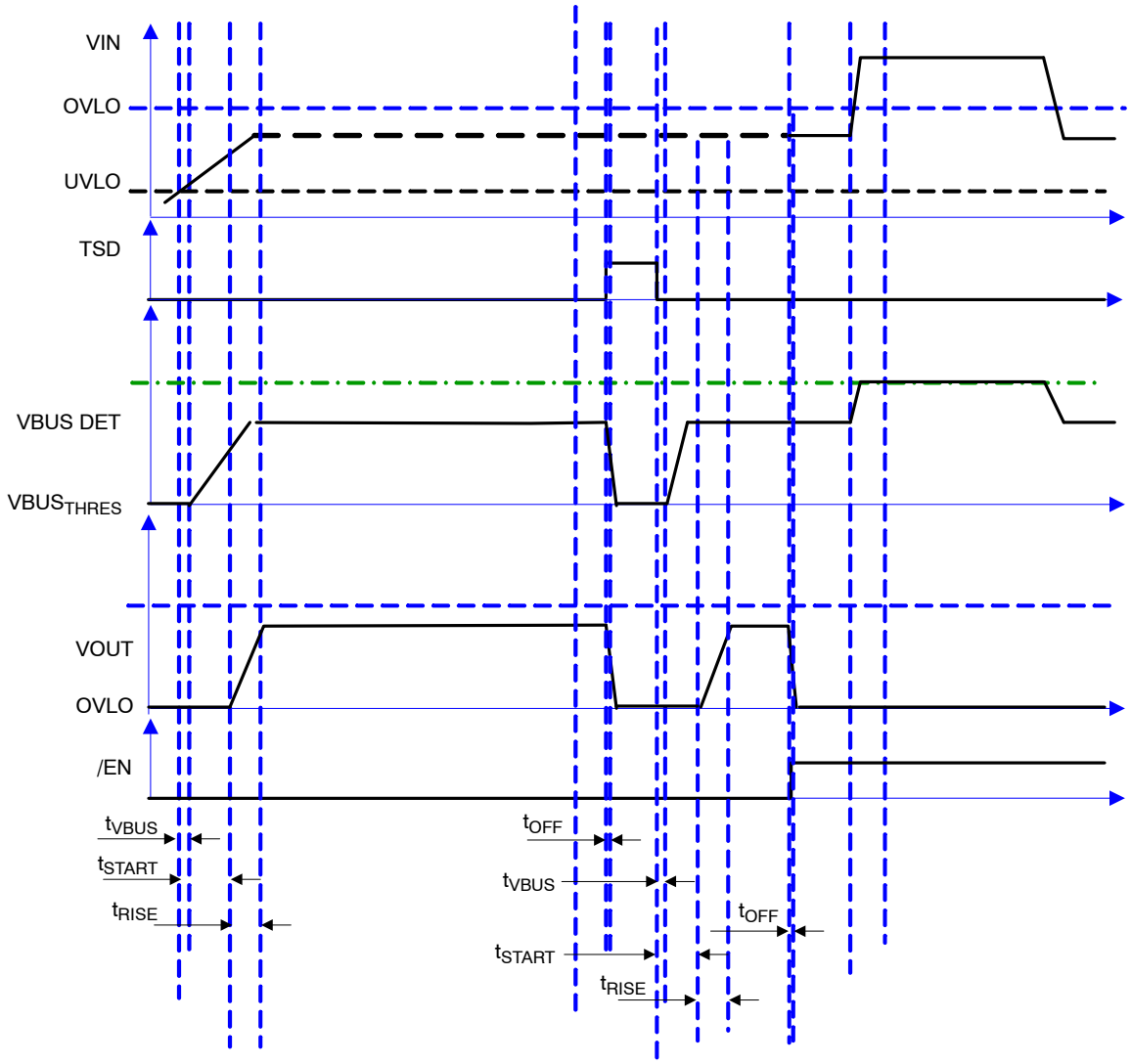


Figure 7. $OVLO_{EXT}$, TSD Modes

$\overline{EN}$ Inputs and Production Mode

To enable normal operation, the $\overline{EN}$ pin has to be at low level. Internal pull down is embedded in the part.

A high level on the $\overline{EN}$ pin, disconnects OUT pin from IN pin.

Table 4. CONTROL LOGIC MODES

OVP State NCP392Bx		OVLO EXT	
		Low	High
/EN	Low	ON T_{start} 15 ms	OFF
	High	OFF	OFF

Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown (TSD) protection allows to open the internal MOSFET in order to instantaneously decrease the device temperature.

Embedded hysteresis allows to reengage the MOSFET when the junction temperature decreases.

If the fault event is still present, the temperature increases again and engages the thermal shutdown one more time until fault event disappeared.

PCB Recommendations

To limit internal power dissipation, PCB routing must be carefully done to improve current capability.

The NCP392B is declined in a CSP package. So power dissipation can be decreased on each pin connection but main thermal area must be as large as possible around IN and OUT pins. Taking into account and respectively, four IN and OUT pins must be hardwired together on the PCB**.**

Maximum power dissipation can be calculated with following formula:

$$T_J - T_A = R_{\theta JA} \times P_d \qquad \text{(eq. 3)}$$

T_J: junction temperature
T_A: ambient temperature
$R_{\theta JA}$: thermal resistance of the junction to air through the case and board.
P_d: power dissipation = $R_{DS(on)}$ x I^2

ESD Tests

The NCP392B fully supports the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board).

That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8 kV ESD protected input.

Please refer to the Figure 8 to see the IEC 61000−4−2 electrostatic discharge waveform.

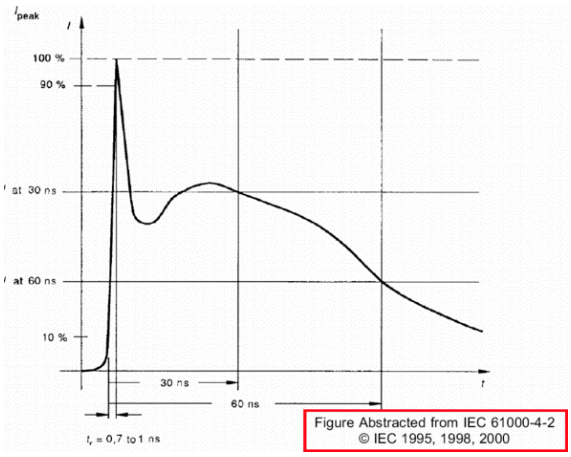


Figure 8. I_{peak} = f(t) / IEC61000−4−2

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCP392BRFCCT1G	392BR	OVLO 5.95 V	WLCSP (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

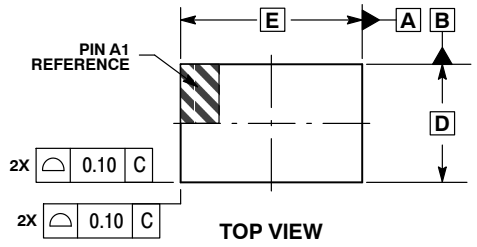
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

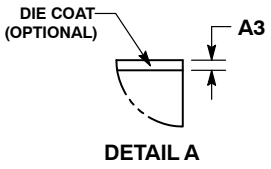
WLCSP12, 1.3x2.0
CASE 567JM
ISSUE A

SCALE 4:1

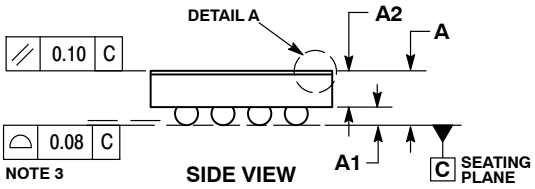
DATE 02 JUL 2014



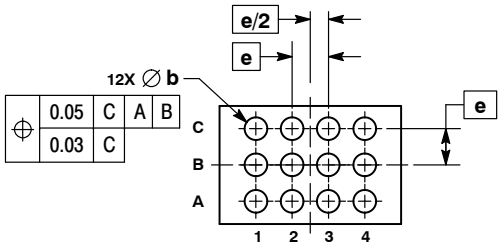
TOP VIEW



DETAIL A



SIDE VIEW

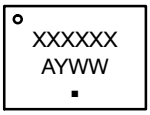


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.04 REF	
b	0.24	0.30
D	1.26	1.31
E	2.01	2.04
e	0.40 BSC	

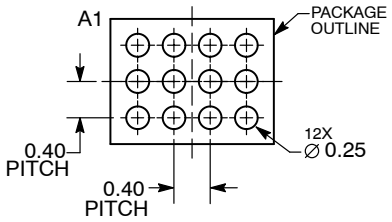
GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP12, 1.3X2.0**	**PAGE 1 OF 1**

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