NCP4305

Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

The NCP4305 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and half bridge resonant LLC.

The combination of externally adjustable minimum off-time and on-time blanking periods helps to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP4305 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency. The high accuracy driver and 5 V gate clamp enables the use of GaN FETs.

Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback, Forward or LLC Applications
- Precise True Secondary Zero Current Detection
- Typically 12 ns Turn off Delay from Current Sense Input to Driver
- Rugged Current Sense Pin (up to 200 V)
- Ultrafast Turn−off Trigger Interface/Disable Input (7.5 ns)
- Adjustable Minimum ON−Time
- Adjustable Minimum OFF-Time with Ringing Detection
- Adjustable Maximum ON−Time for CCM Controlling of Primary QR Controller
- Improved Robust Self Synchronization Capability
- 8 A / 4 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−load & Disable Mode
- Adaptive Gate Drive Clamp
- GaN Transistor Driving Capability (options A and C)
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- SOIC-8 and DFN−8 (4x4) and WDFN8 (2x2) Packages
- These are Pb−Free Devices

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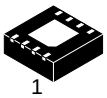
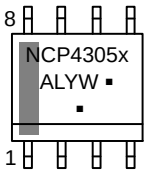
SOIC−8
D SUFFIX
CASE 751

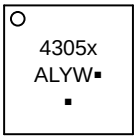


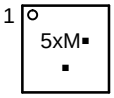
DFN8
MN SUFFIX
CASE 488AF

WDFN8
MT SUFFIX
CASE 511AT

MARKING DIAGRAMS







4305x	= Specific Device Code x = A, B, C, D or Q
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 49 of this data sheet.

Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

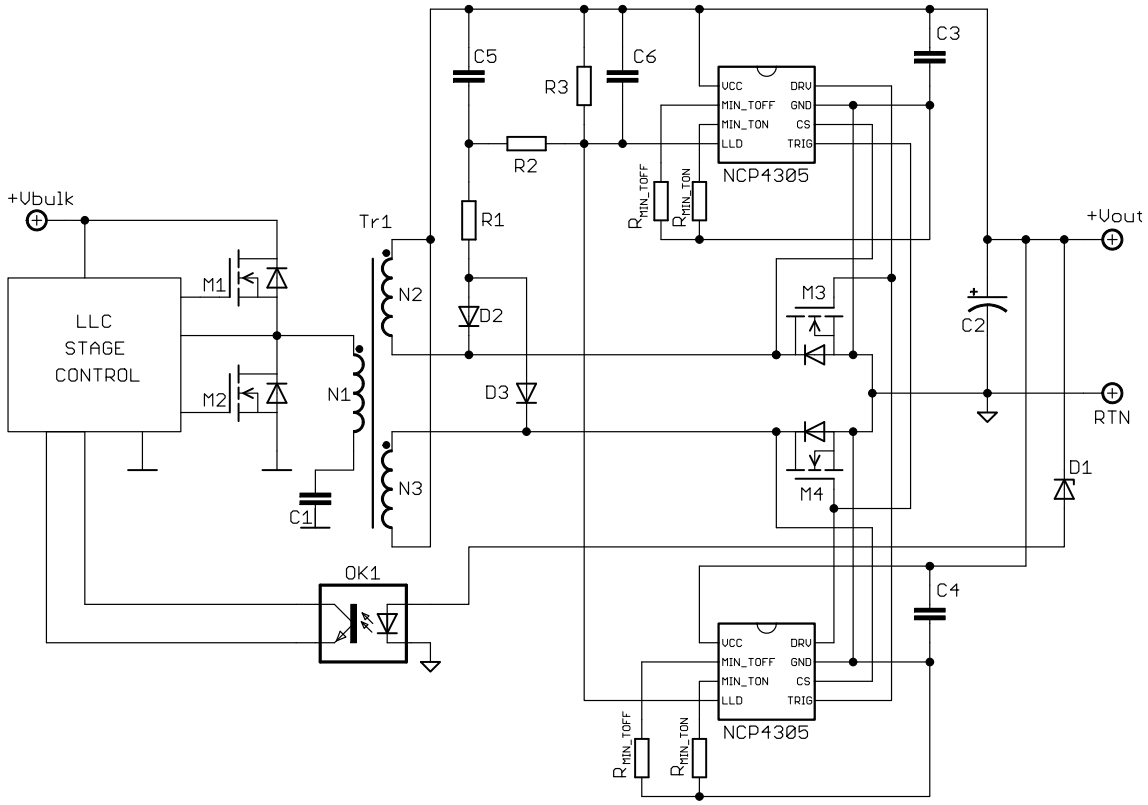


Figure 1. Typical Application Example − LLC Converter with Optional LLD and Trigger Utilization

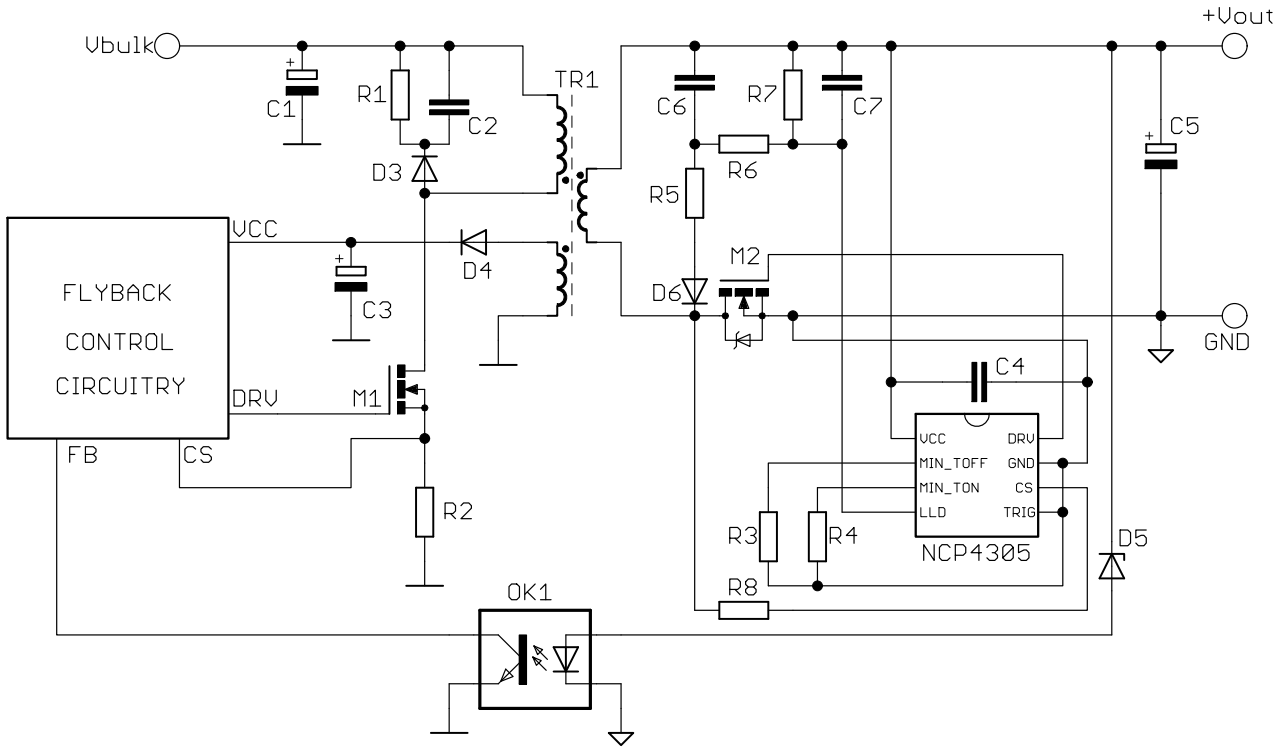


Figure 2. Typical Application Example − DCM, CCM or QR Flyback Converter with optional LLD and Disabled TRIG

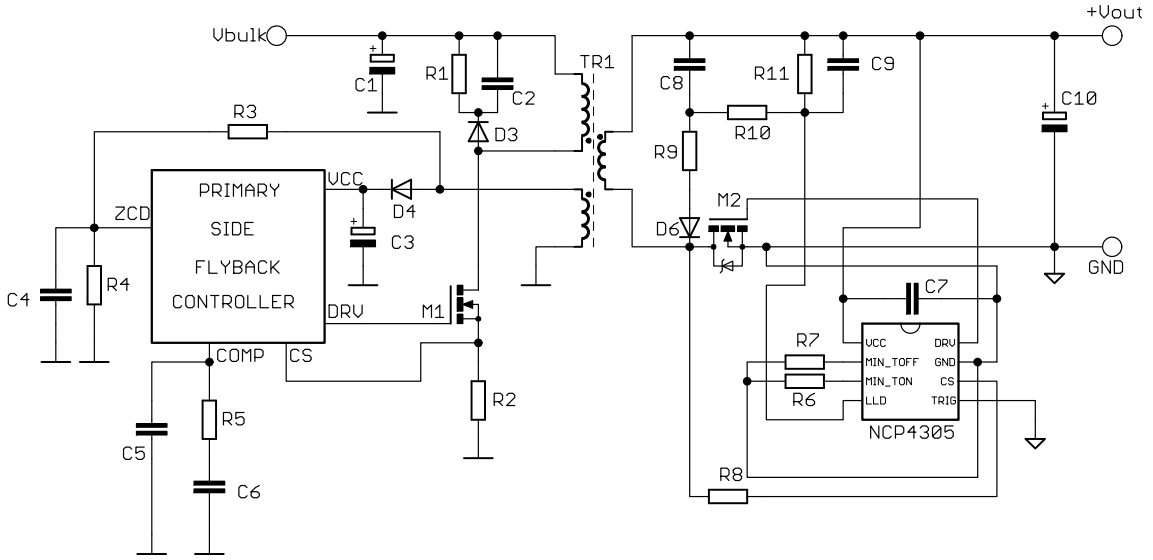


Figure 3. Typical Application Example − Primary Side Flyback Converter with optional LLD and Disabled TRIG

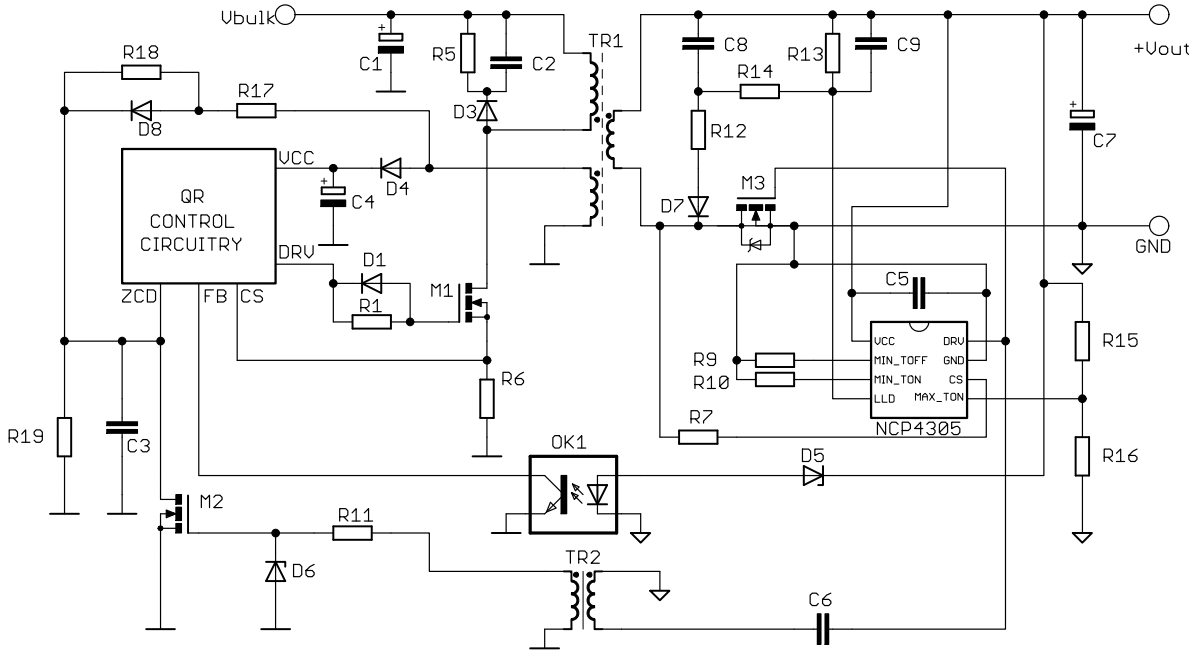


Figure 4. Typical Application Example − QR Converter − Capability to Force Primary into CCM Under Heavy Loads utilizing MAX−TON

PIN FUNCTION DESCRIPTION

ver. A, B, C, D	ver. Q	Pin Name	Description
1	1	VCC	Supply voltage pin
2	2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground.
3	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground.
4	4	LLD	This input modulates the driver clamp level and/or turns the driver off during light load conditions.
5	−	TRIG/DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs.
6	6	CS	Current sense pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn−off detection threshold is 0 mV. A resistor in series with this pin can decrease the turn off threshold if needed.
7	7	GND	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum on and off time adjust resistors, LLD and trigger inputs. GND pin should be wired directly to the SR MOSFET source terminal/soldering point using Kelvin connection. DFN8 exposed flag should be connected to GND
8	8	DRV	Driver output for the SR MOSFET
−	5	MAX_TON	Adjust the maximum on time period by connecting resistor to ground.

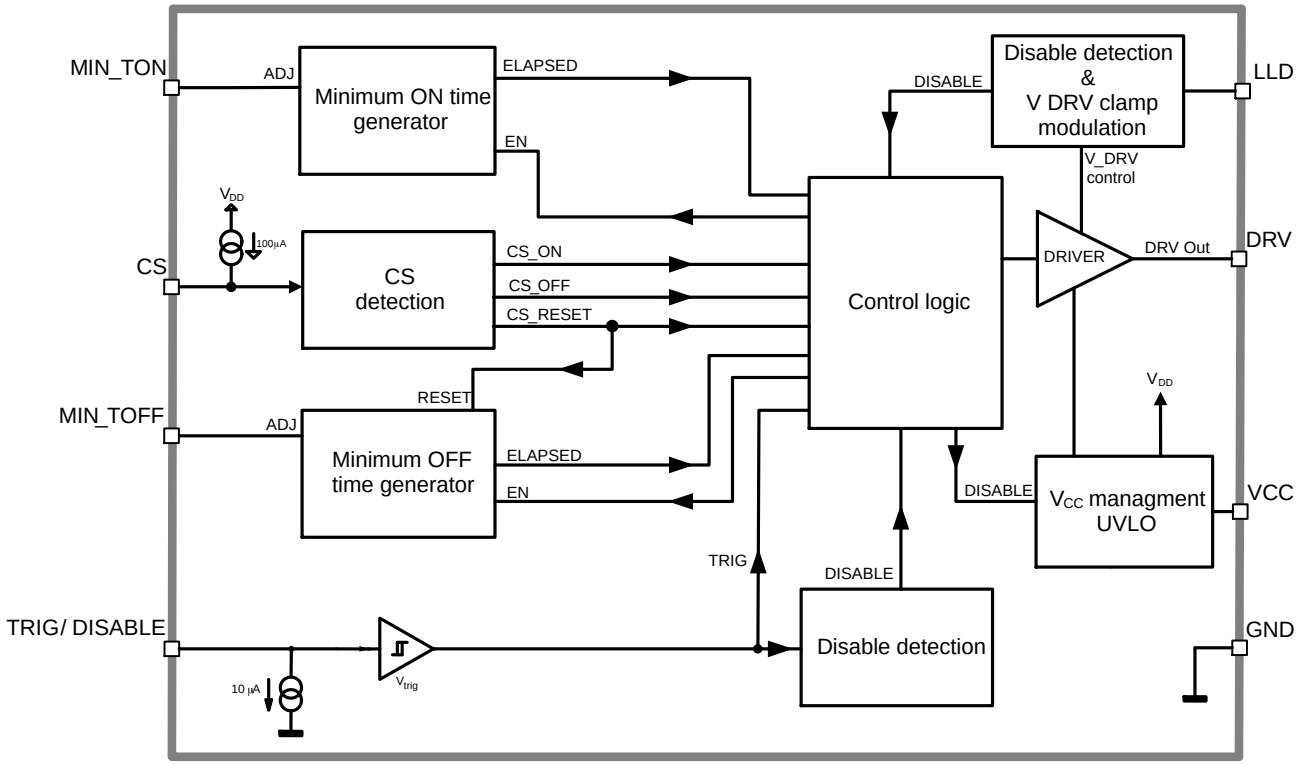


Figure 5. Internal Circuit Architecture − NCP4305A, B, C, D

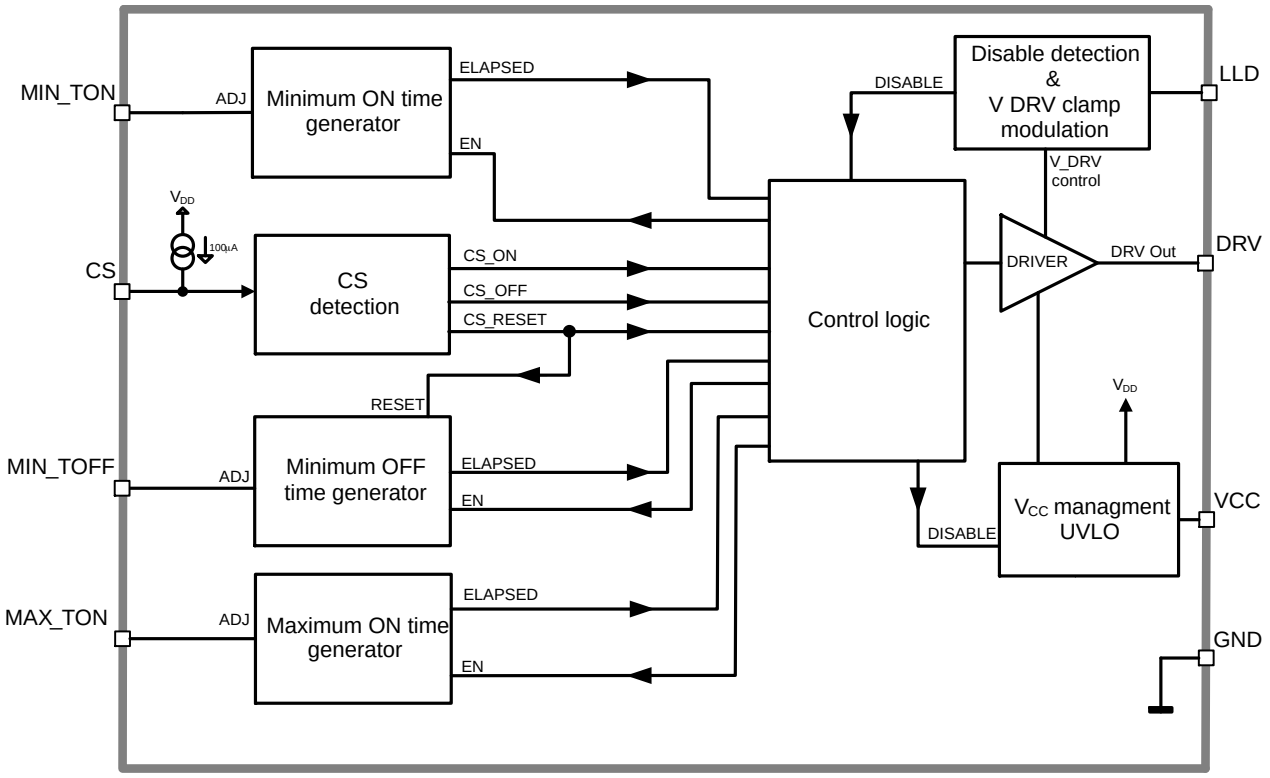


Figure 6. Internal Circuit Architecture − NCP4305Q (CCM QR) with MAX_TON

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 37.0	V
TRIG/DIS, MIN_TON, MIN_TOFF, MAX_TON, LLD Input Voltage	$V_{TRIG/DIS}$, V_{MIN_TON}, V_{MIN_TOFF}, V_{MAX_TON}, V_{LLD}	−0.3 to V_{CC}	V
Driver Output Voltage	V_{DRV}	−0.3 to 17.0	V
Current Sense Input Voltage	V_{CS}	−4 to 200	V
Current Sense Dynamic Input Voltage (t_{PW} = 200 ns)	V_{CS_DYN}	−10 to 200	V
MIN_TON, MIN_TOFF, MAX_TON, LLD, TRIG Input Current	I_{MIN_TON}, I_{MIN_TOFF}, I_{MAX_TON}, I_{LLD}, I_{TRIG}	−10 to 10	mA
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, SOIC8	$R_{\theta J-A\_SOIC8}$	160	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, DFN8	$R_{\theta J-A\_DFN8}$	80	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in^2 Copper Area, WDFN8	$R_{\theta J-A\_WDFN8}$	160	°C/W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model, Except Pin 6, per JESD22−A114E	ESD_{HBM}	2000	V
ESD Capability, Human Body Model, Pin 6, per JESD22−A114E	ESD_{HBM}	1000	V
ESD Capability, Machine Model, per JESD22−A115−A	ESD_{MM}	200	V
ESD Capability, Charged Device Model, Except Pin 6, per JESD22−C101F	ESD_{CDM}	750	V
ESD Capability, Charged Device Model, Pin 6, per JESD22−C101F	ESD_{CDM}	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device meets latch−up tests defined by JEDEC Standard JESD78D Class I.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Maximum Operating Input Voltage	V_{CC}		35	V
Operating Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_J ≤ 125°C; V_{CC} = 12 V; C_{DRV} = 0 nF; R_{MIN_TON} = R_{MIN_TOFF} = 10 kΩ; $V_{TRIG/DIS}$ = 0 V; V_{LLD} = 0 V; V_{CS} = −1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
SUPPLY SECTION							
VCC UVLO (ver. B & C)	V_{CC} rising		V_{CCON}	8.3	8.8	9.4	V
	V_{CC} falling		V_{CCOFF}	7.3	7.8	8.3	
VCC UVLO Hysteresis (ver. B & C)			V_{CCHYS}		1.0		V
VCC UVLO (ver. A, D & Q)	V_{CC} rising		V_{CCON}	4.20	4.45	4.80	V
	V_{CC} falling		V_{CCOFF}	3.70	3.95	4.20	
VCC UVLO Hysteresis (ver. A, D & Q)			V_{CCHYS}		0.5		V
Start−up Delay	V_{CC} rising from 0 to V_{CCON} + 1 V @ tr = 10 μs		t_{START_DEL}		75	125	μs
Current Consumption, R_{MIN_TON} = R_{MIN_TOFF} = 0 kΩ	C_{LOAD} = 0 nF, f_{SW} = 500 kHz	A, C	I_{CC}	3.3	4.0	5.6	mA
		B, D, Q		3.8	4.5	6.0	
	C_{LOAD} = 0 nF, f_{SW} = 500 kHz, WDFN	A, C		3.0	4.0	5.6	
		B, D, Q		3.5	4.5	6.0	
	C_{LOAD} = 1 nF, f_{SW} = 500 kHz	A, C		4.5	6.0	7.5	
		B, D, Q		7.7	9.0	10.7	
	C_{LOAD} = 10 nF, f_{SW} = 500 kHz	A, C		20	25	30	
		B, D, Q		40	50	60	
Current Consumption	No switching, V_{CS} = 0 V, R_{MIN_TON} = R_{MIN_TOFF} = 0 k		I_{CC}	1.5	2.0	2.5	mA
Current Consumption below UVLO	No switching, V_{CC} = V_{CCOFF} − 0.1 V, V_{CS} = 0 V		I_{CC_UVLO}		75	125	μA
Current Consumption in Disable Mode	V_{LLD} = V_{CC} − 0.1 V, V_{CS} = 0 V		I_{CC_DIS}	40	55	70	μA
	V_{TRIG} = 5 V, V_{LLD} = V_{CC} − 3 V, V_{CS} = 0 V			45	65	80	
DRIVER OUTPUT							
Output Voltage Rise−Time	C_{LOAD} = 10 nF, 10% to 90% V_{DRVMAX}		t_r		40	55	ns
Output Voltage Fall−Time	C_{LOAD} = 10 nF, 90% to 10% V_{DRVMAX}		t_f		20	35	ns
Driver Source Resistance			R_{DRV_SOURCE}		1.2		Ω
Driver Sink Resistance			R_{DRV_SINK}		0.5		Ω
Output Peak Source Current			I_{DRV_SOURCE}		4		A
Output Peak Sink Current			I_{DRV_SINK}		8		A
Maximum Driver Output Voltage	V_{CC} = 35 V, C_{LOAD} > 1 nF, V_{LLD} = 0 V, (ver. B, D and Q)		V_{DRVMAX}	9.0	9.5	10.5	V
	V_{CC} = 35 V, C_{LOAD} > 1 nF, V_{LLD} = 0 V, (ver. A, C)			4.3	4.7	5.5	
Minimum Driver Output Voltage	V_{CC} = V_{CCOFF} + 200 mV, V_{LLD} = 0 V, (ver. B)		V_{DRVMIN}	7.2	7.8	8.5	V
	V_{CC} = V_{CCOFF} + 200 mV, V_{LLD} = 0 V, (ver. C)			4.2	4.7	5.3	
	V_{CC} = V_{CCOFF} + 200 mV, V_{LLD} = 0 V, (ver. A, D, Q)			3.6	4.0	4.4	
Minimum Driver Output Voltage	V_{LLD} = V_{CC} − V_{LLDREC} V		$V_{DRVLLDMIN}$	0.0	0.4	1.2	V

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 10 kΩ; $V_{TRIG/DIS}$ = 0 V; V_{LLD} = 0 V; V_{CS} = −1 to +4 V; f_{CS} = 100 kHz, DC_{CS} = 50%, unless otherwise noted. Typical values are at T_J = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CS INPUT						
Total Propagation Delay From CS to DRV Output On	V_{CS} goes down from 4 to −1 V, t_{f_CS} = 5 ns	t_{PD_ON}		35	60	ns
Total Propagation Delay From CS to DRV Output Off	V_{CS} goes up from −1 to 4 V, t_{r_CS} = 5 ns	t_{PD_OFF}		12	23	ns
CS Bias Current	V_{CS} = −20 mV	I_{CS}	−105	−100	−95	μA
Turn On CS Threshold Voltage		$V_{TH\_CS\_ON}$	−120	−75	−40	mV
Turn Off CS Threshold Voltage	Guaranteed by Design	$V_{TH\_CS\_OFF}$	−1		0	mV
Turn Off Timer Reset Threshold Voltage		$V_{TH\_CS\_RESET}$	0.42	0.48	0.54	V
CS Leakage Current	V_{CS} = 200 V	$I_{CS\_LEAKAGE}$			0.4	μA
TRIGGER DISABLE INPUT						
Minimum Trigger Pulse Duration	V_{TRIG} = 5 V; Shorter pulses may not be proceeded	$t_{TRIG\_PW\_MIN}$			10	ns
Trigger Threshold Voltage		V_{TRIG_TH}	1.87	2.02	2.18	V
Trigger to DRV Propagation Delay	V_{TRIG} goes from 0 to 5 V, t_{r_TRIG} = 5 ns	t_{PD_TRIG}		7.5	12.5	ns
Trigger Blank Time After DRV Turn−on Event	V_{CS} drops below $V_{TH\_CS\_ON}$	t_{TRIG_BLANK}	35	50	65	ns
Delay to Disable Mode	V_{TRIG} = 5 V	t_{DIS_TIM}	75	100	125	μs
Disable Recovery Timer	V_{TRIG} goes down from 5 to 0 V	t_{DIS_REC}	5	8	13	μs
Minimum Pulse Duration to Disable Mode End	V_{TRIG} = 0 V; Shorter pulses may not be proceeded	$t_{DIS\_END\_MIN}$			200	ns
Pull Down Current	V_{TRIG} = 5 V	I_{TRIG}	9	13	16	μA
MINIMUM t_{ON} and t_{OFF} ADJUST						
Minimum t_{ON} time	R_{MIN_TON} = 0 Ω	t_{ON_MIN}	35	55	75	ns
Minimum t_{OFF} time	R_{MIN_TOFF} = 0 Ω	t_{OFF_MIN}	190	245	290	ns
Minimum t_{ON} time	R_{MIN_TON} = 10 kΩ	t_{ON_MIN}	0.92	1.00	1.08	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 10 kΩ	t_{OFF_MIN}	0.92	1.00	1.08	μs
Minimum t_{ON} time	R_{MIN_TON} = 50 kΩ	t_{ON_MIN}	4.62	5.00	5.38	μs
Minimum t_{OFF} time	R_{MIN_TOFF} = 50 kΩ	t_{OFF_MIN}	4.62	5.00	5.38	μs
MAXIMUM t_{ON} ADJUST						
Maximum t_{ON} Time	V_{MAX_TON} = 3 V	t_{ON_MAX}	4.3	4.8	5.3	μs
Maximum t_{ON} Time	V_{MAX_TON} = 0.3 V	t_{ON_MAX}	41	48	55	μs
Maximum t_{ON} Output Current	V_{MAX_TON} = 0.3 V	I_{MAX_TON}	−105	−100	−95	μA
LLD INPUT						
Disable Threshold	$V_{LLD\_DIS} = V_{CC} - V_{LLD}$	V_{LLD_DIS}	0.8	0.9	1.0	V
Recovery Threshold	$V_{LLD\_REC} = V_{CC} - V_{LLD}$	V_{LLD_REC}	0.9	1.0	1.1	V
Disable Hysteresis		V_{LLD_DISH}		0.1		V
Disable Time Hysteresis	Disable to Normal, Normal to Disable	t_{LLD_DISH}		45		μs
Disable Recovery Time		$t_{LLD\_DIS\_REC}$	7.0	12.5	16.0	μs
Low Pass Filter Frequency		f_{LPLLD}	6	10	13	kHz
Driver Voltage Clamp Threshold	$V_{DRV} = V_{DRVMAX}$, $V_{LLDMAX} = V_{CC} - V_{LLD}$	V_{LLDMAX}		2.0		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

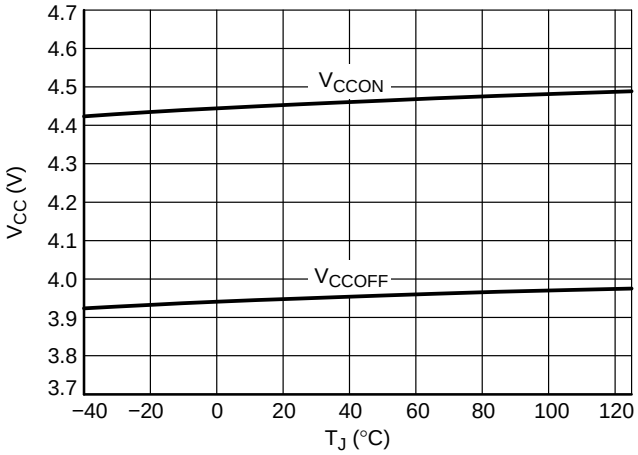


Figure 7. V_{CCON} and V_{CCOFF} Levels, ver. A, D, Q

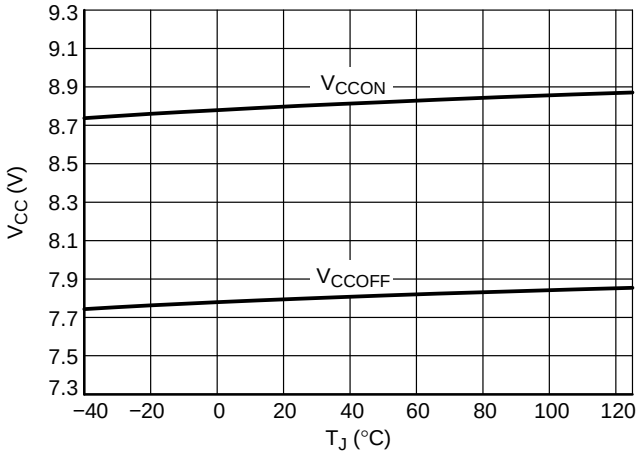


Figure 8. V_{CCON} and V_{CCOFF} Levels, ver. B, C

TYPICAL CHARACTERISTICS

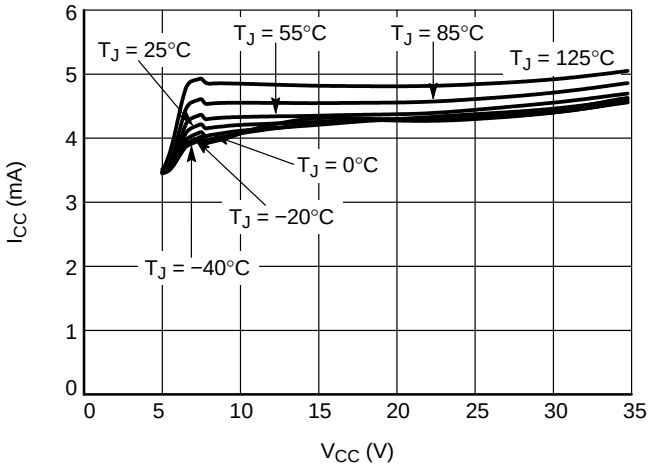


Figure 9. Current Consumption, C_{DRV} = 0 nF, f_{CS} = 500 kHz, ver. D

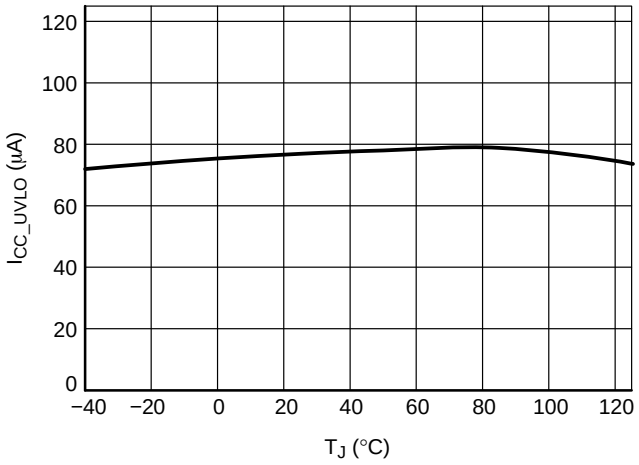


Figure 10. Current Consumption, V_{CC} = V_{CCOFF} − 0.1 V, V_{CS} = 0 V, ver. D

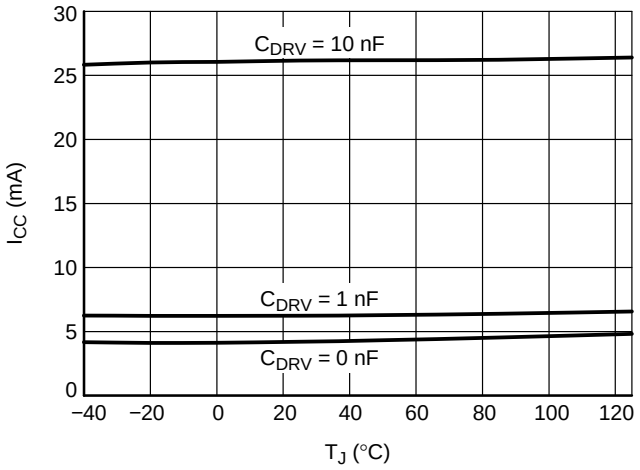


Figure 11. Current Consumption, V_{CC} = 12 V, V_{CS} = −1 to 4 V, f_{CS} = 500 kHz, ver. A

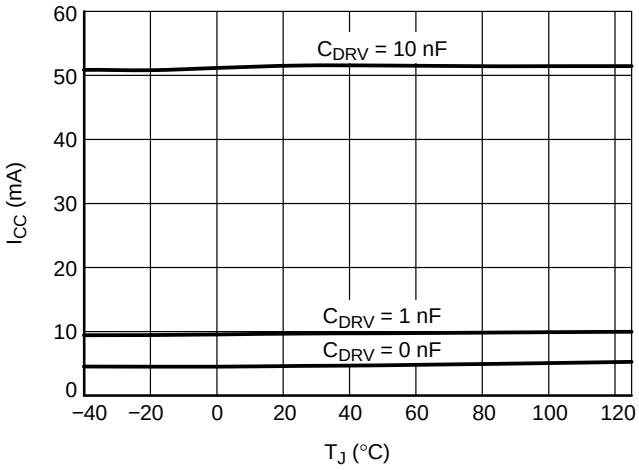


Figure 12. Current Consumption, V_{CC} = 12 V, V_{CS} = −1 to 4 V, f_{CS} = 500 kHz, ver. D

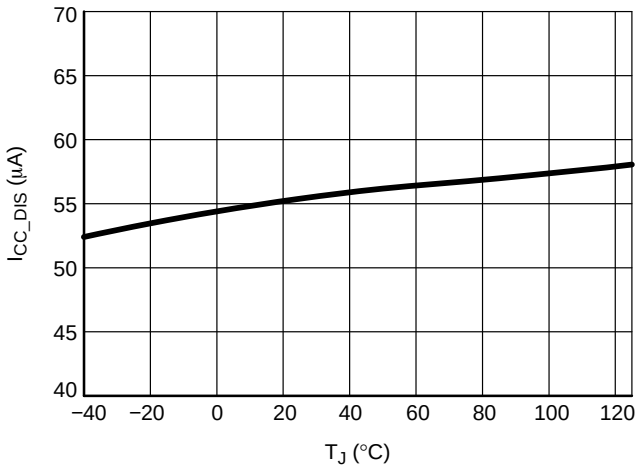


Figure 13. Current Consumption in Disable, V_{CC} = 12 V, V_{CS} = 0 V, V_{LLD} = V_{CC} − 0.1 V

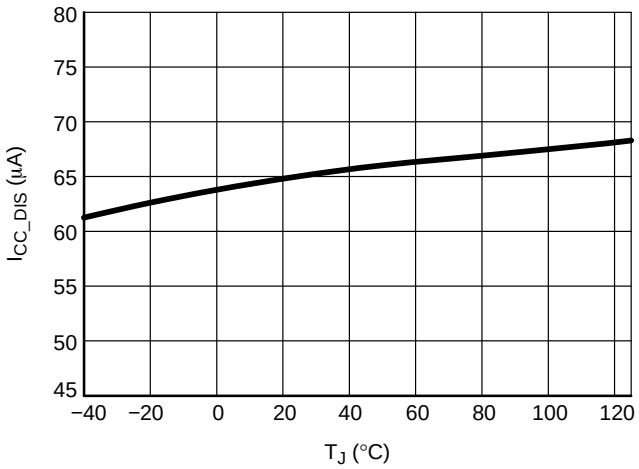


Figure 14. Current Consumption in Disable, V_{CC} = 12 V, V_{CS} = 0 V, V_{LLD} = V_{CC} − 3 V, V_{TRIG} = 5 V

TYPICAL CHARACTERISTICS

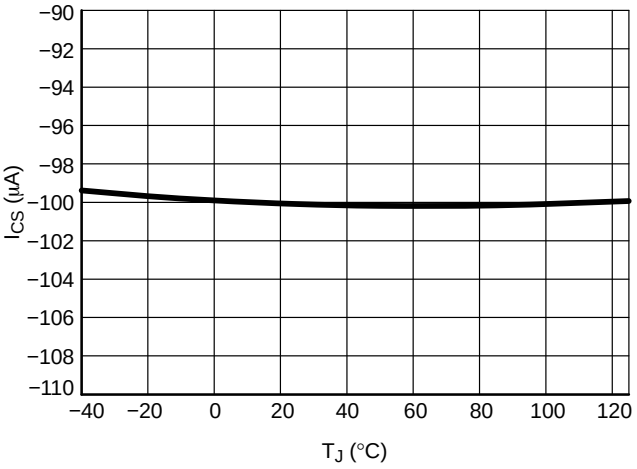


Figure 15. CS Current, V_{CS} = −20 mV

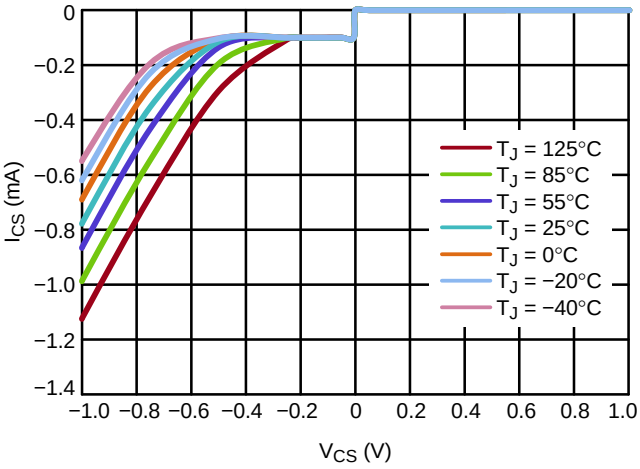


Figure 16. CS Current, V_{CC} = 12 V

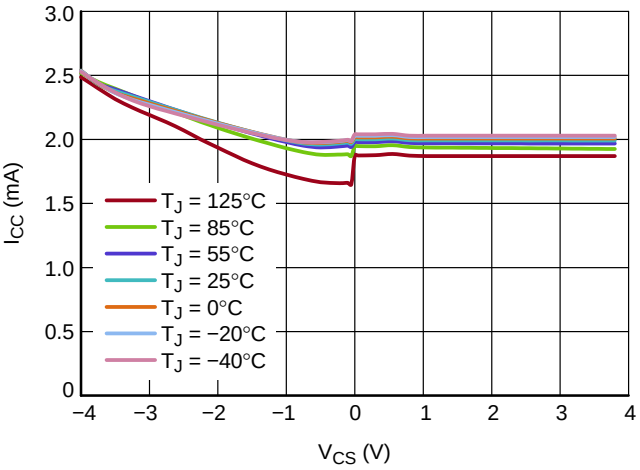


Figure 17. Supply Current vs. CS Voltage, V_{CC} = 12 V

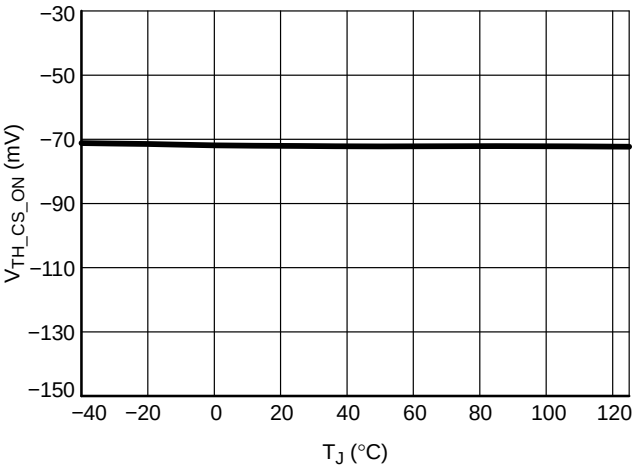


Figure 18. CS Turn−on Threshold

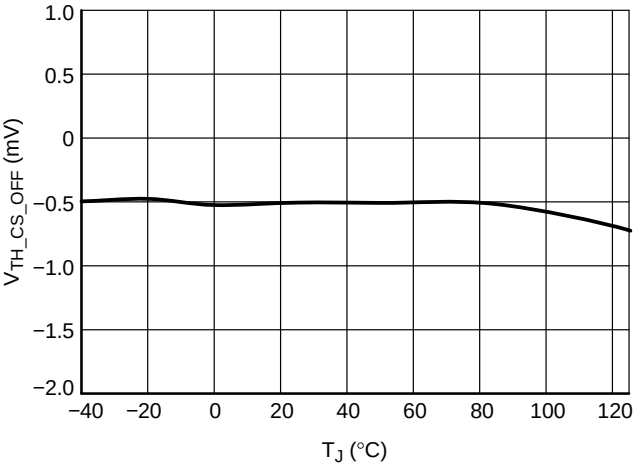


Figure 19. CS Turn−off Threshold

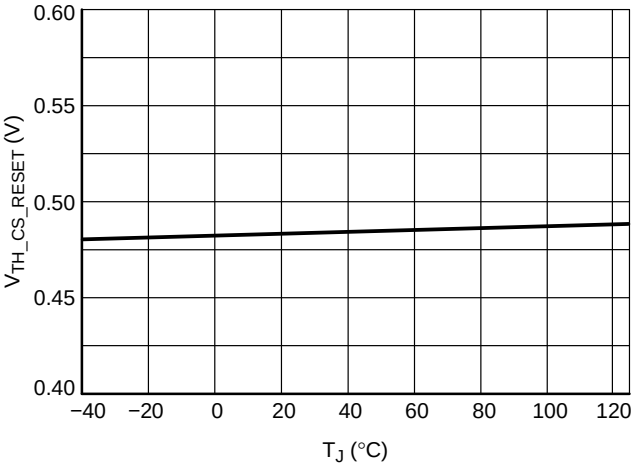


Figure 20. CS Reset Threshold

TYPICAL CHARACTERISTICS

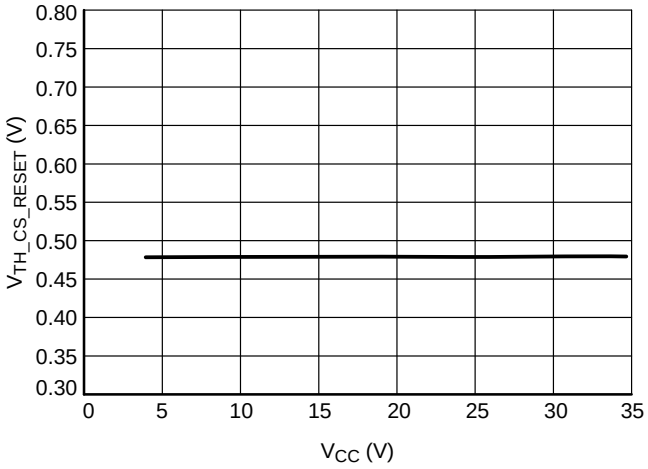


Figure 21. CS Reset Threshold

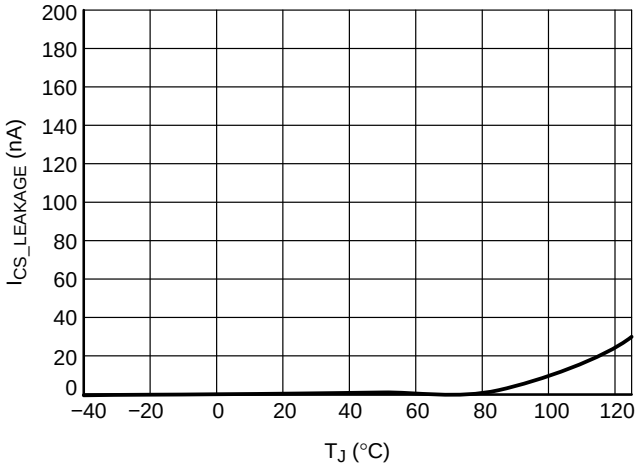


Figure 22. CS Leakage, V_{CS} = 200 V

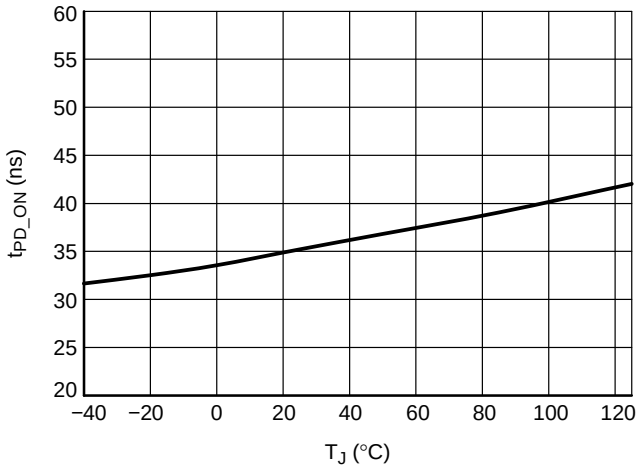


Figure 23. Propagation Delay from CS to DRV Output On

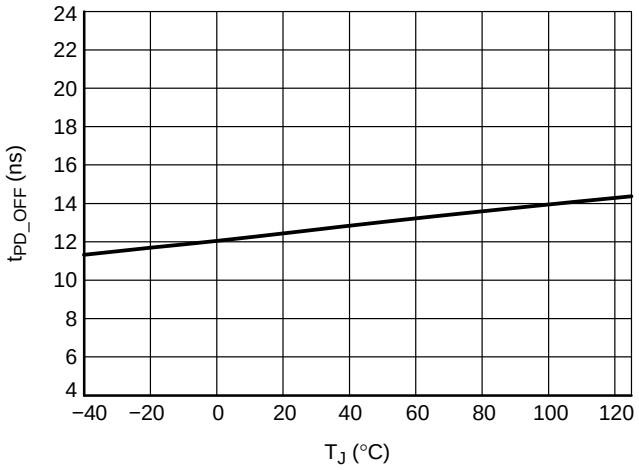


Figure 24. Propagation Delay from CS to DRV Output Off

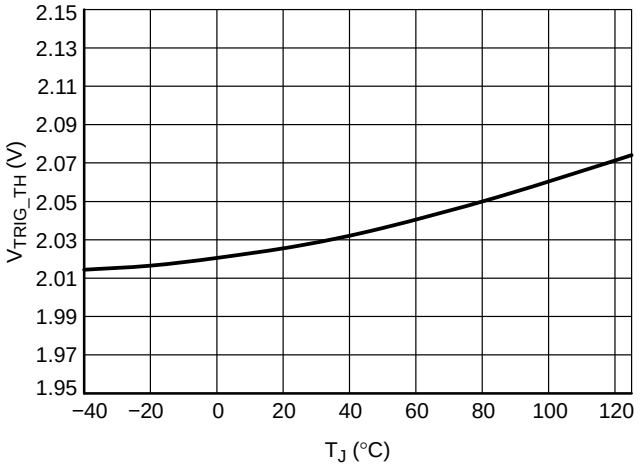


Figure 25. Trigger Threshold, V_{CC} = 12 V

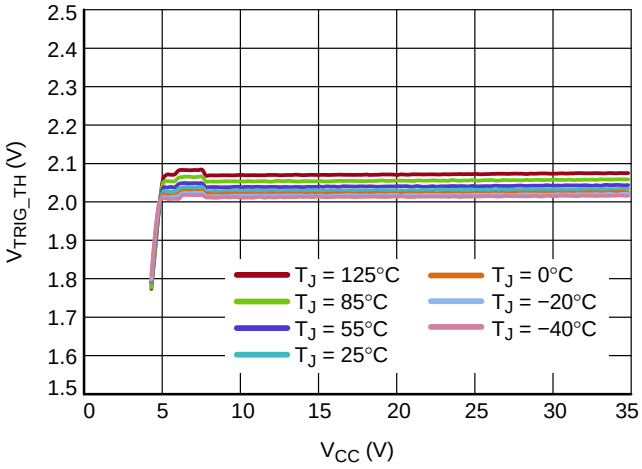


Figure 26. Trigger Threshold

TYPICAL CHARACTERISTICS

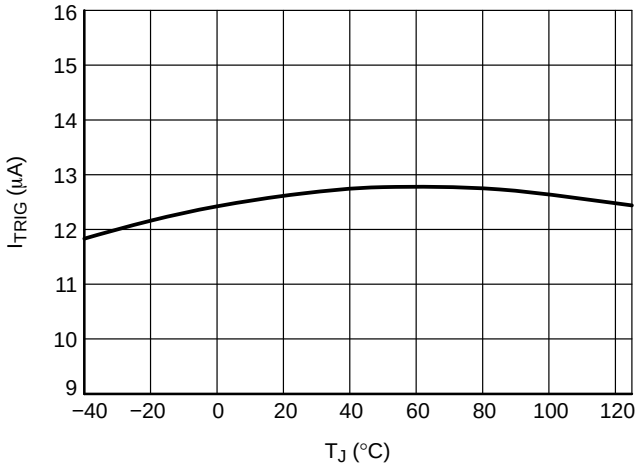


Figure 27. Trigger Pull Down Current

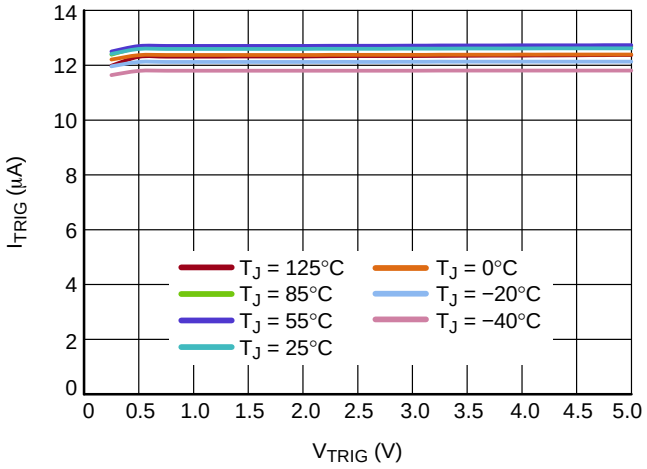


Figure 28. Trigger Pull Down Current, V_{CC} = 12 V

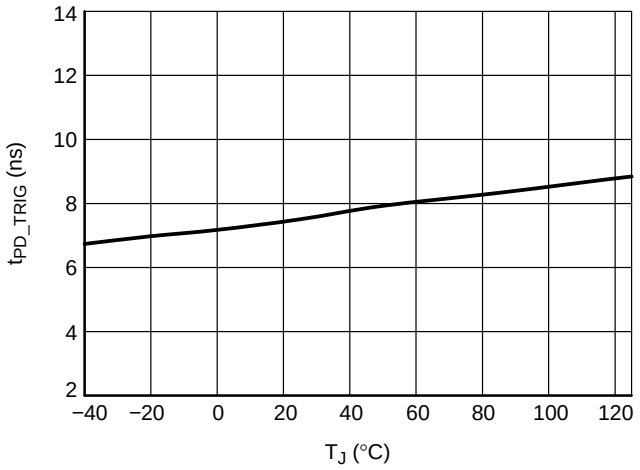


Figure 29. Propagation Delay from Trigger to Driver Output Off

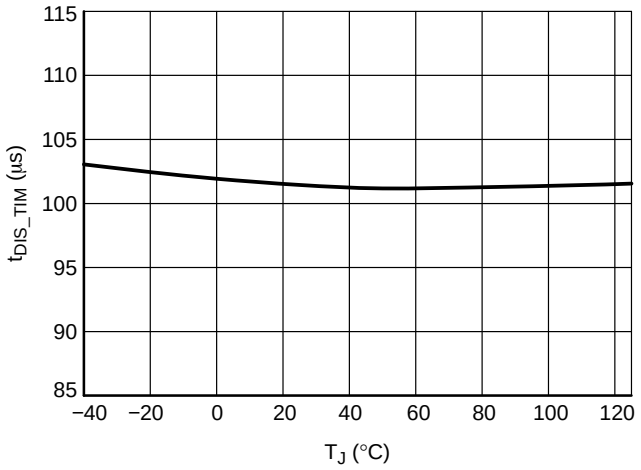


Figure 30. Delay to Disable Mode, V_{TRIG} = 5 V

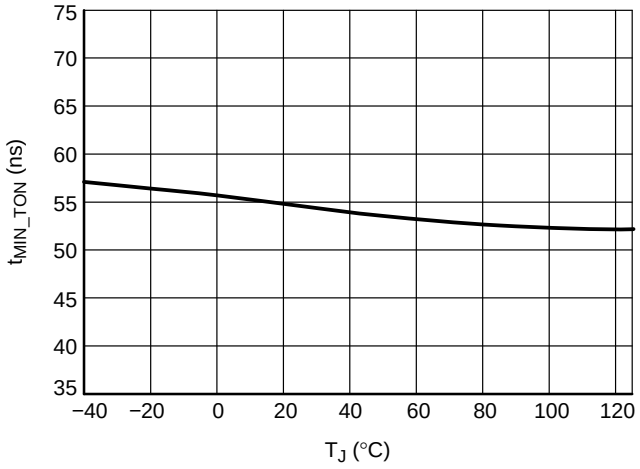


Figure 31. Minimum On−time R_{MIN_TON} = 0 Ω

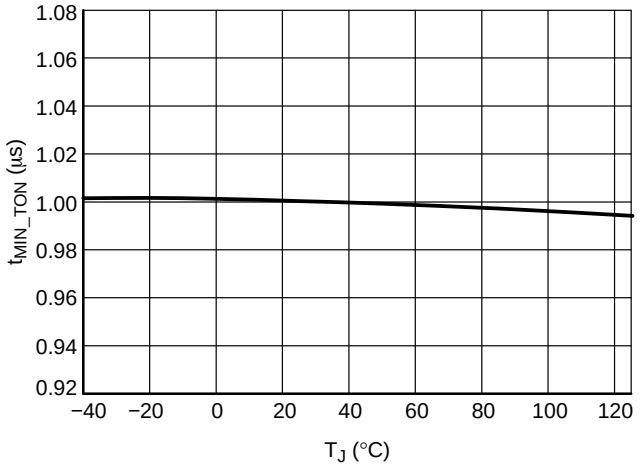


Figure 32. Minimum On−time R_{MIN_TON} = 10 kΩ

TYPICAL CHARACTERISTICS

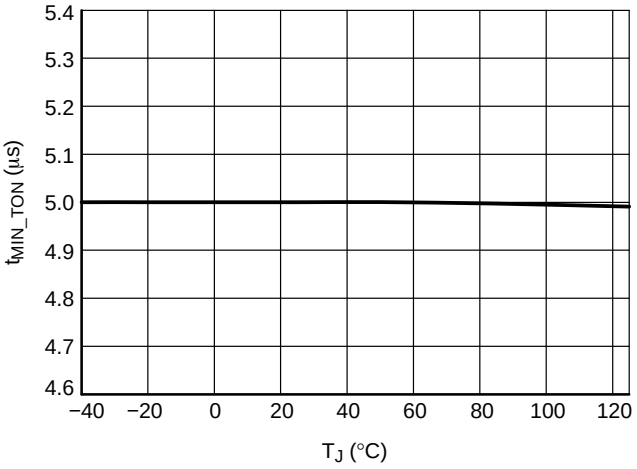


Figure 33. Minimum On−time R_{MIN_TON} = 50 kΩ

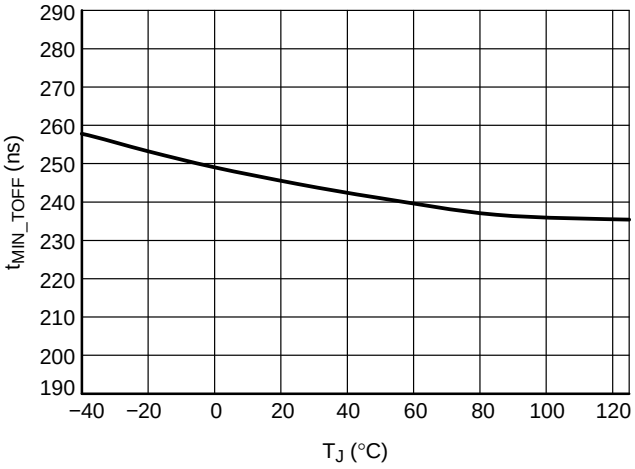


Figure 34. Minimum Off−time R_{MIN_TOFF} = 0 Ω

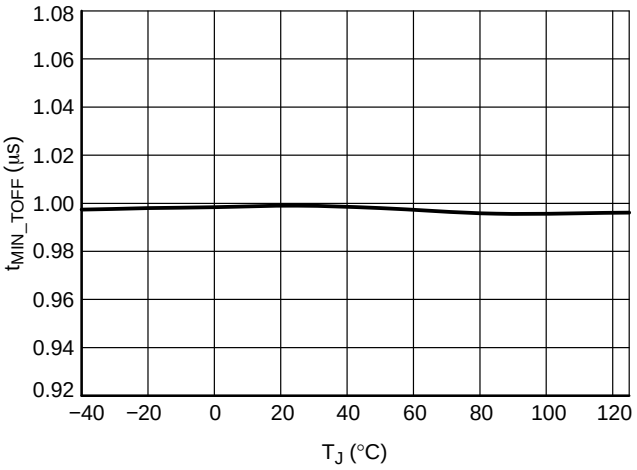


Figure 35. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

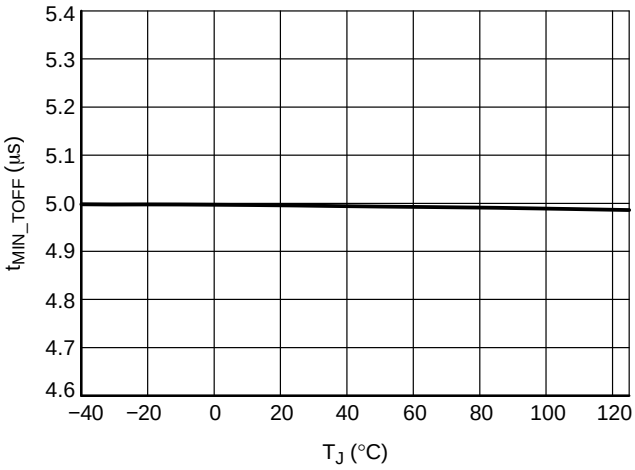


Figure 36. Minimum Off−time R_{MIN_TOFF} = 50 kΩ

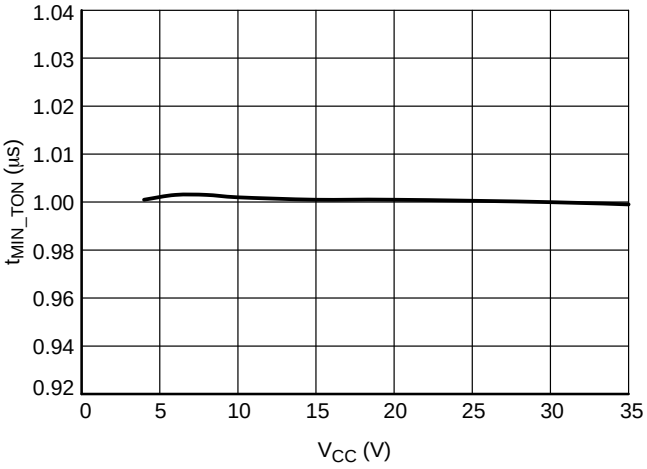


Figure 37. Minimum On−time R_{MIN_TON} = 10 kΩ

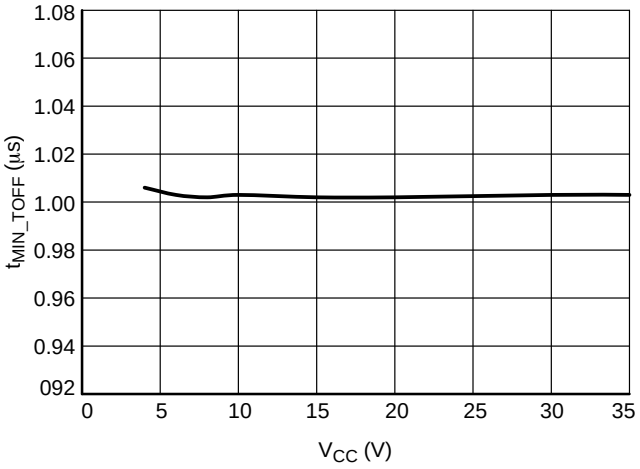


Figure 38. Minimum Off−time R_{MIN_TOFF} = 10 kΩ

TYPICAL CHARACTERISTICS

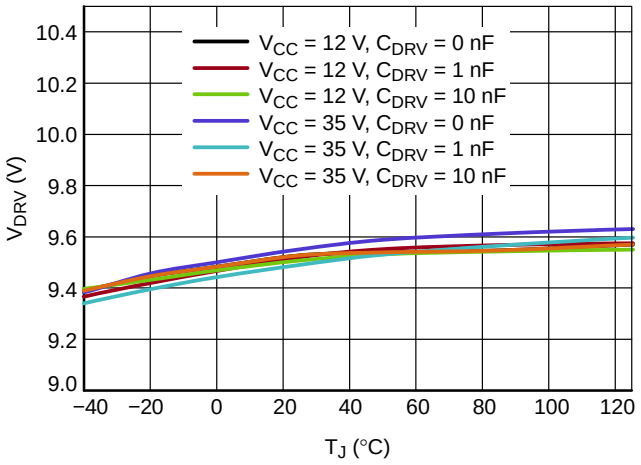


Figure 39. Driver and Output Voltage, ver. B, D and Q

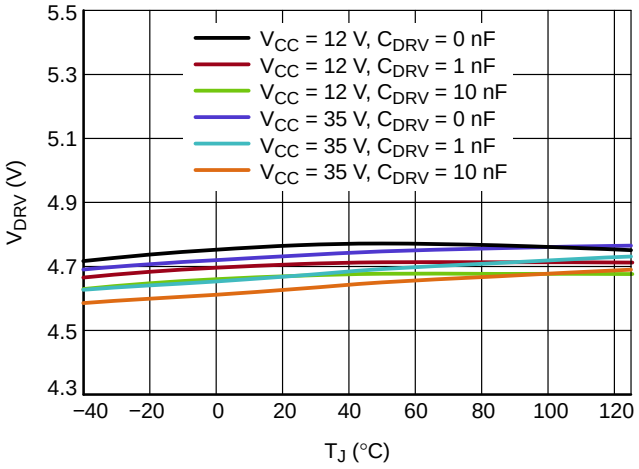


Figure 40. Driver Output Voltage, ver. A and C

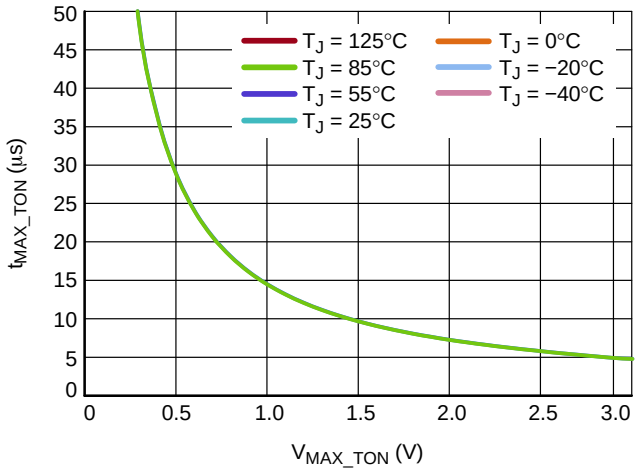


Figure 41. Maximum On−time, ver. Q

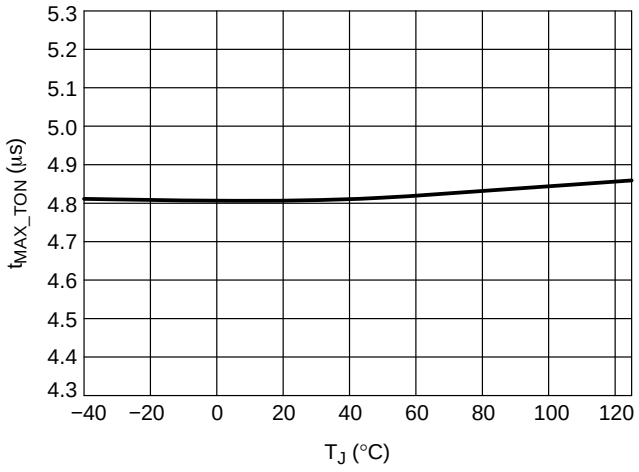


Figure 42. Maximum On−time, V_{MAX_TON} = 3 V, ver. Q

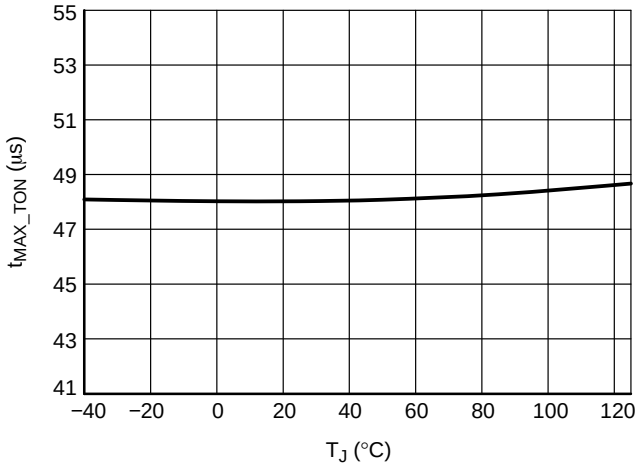


Figure 43. Maximum On−time, V_{MAX_TON} = 0.3 V, ver. Q

APPLICATION INFORMATION

General description

The NCP4305 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4305 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4305 works from an available voltage with range from 4 V (A, D & Q options) or 8 V (B & C options) to 35 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn-off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn-off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn-off thresholds in the range of −10 mV to −5 mV, the NCP4305 offers a turn-off threshold of 0 mV. When using a low $R_{DS(on)}$ SR (1 mΩ) MOSFET our competition, with a −10 mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn-off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET causing the SR MOSFET to operate in the linear region to reduce turn−off time. Thanks to the 8 A sink current of the NCP4305 significantly reduces turn off time allowing for a minimal drain source voltage to be utilized and efficiency maximized.

To overcome false triggering issues after turn-on and turn−off events, the NCP4305 provides adjustable minimum on-time and off-time blanking periods. Blanking times can be adjusted independently of IC VCC using external resistors connected to GND. If needed, blanking periods can be modulated using additional components.

An extremely fast turn−off comparator, implemented on the current sense pin, allows for NCP4305 implementation in CCM applications without any additional components or external triggering.

An ultrafast trigger input offers the possibility to further increase efficiency of synchronous rectification systems operated in CCM mode (for example, CCM flyback or forward). The time delay from trigger input to driver turn off event is t_{PD_TRIG}. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS. If the trigger input is not wanted than the trigger pin can be tied to GND or an option can be chosen to replace this pin with a MAX_TON input.

An output driver features capability to keep SR transistor closed even when there is no supply voltage for NCP4305. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may turn on transistor. NCP4305 uses this pulsing voltage at SR transistor gate (DRV pin) and uses it internally to provide enough supply to activate internal driver sink transistor. DRV voltage is pulled low (not to zero) thanks to this feature and eliminate the risk of turned on SR transistor before enough V_{CC} is applied to NCP4305.

Some IC versions include a MAX_TON circuit that helps a quasi resonant (QR) controller to work in CCM mode when a heavy load is present like in the example of a printer's motor starting up.

Finally, the NCP4305 features a special pin (LLD) that can be used to reduce gate driver voltage clamp according to application load conditions. This feature helps to reduce issues with transition from disabled driver to full driver output voltage and back. Disable state can be also activated through this pin to decrease power consumption in no load conditions. If the LLD feature is not wanted then the LLD pin can be tied to GND.

Current Sense Input

Figure 44 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. The CS pin sources current of 100 μA that creates a voltage drop on the R_{SHIFT_CS} resistor (resistor is optional, we recommend shorting this resistor). Once the voltage on the CS pin is lower than $V_{TH\_CS\_ON}$ threshold, M1 is turned−on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using the R_{MIN_TON} resistor.

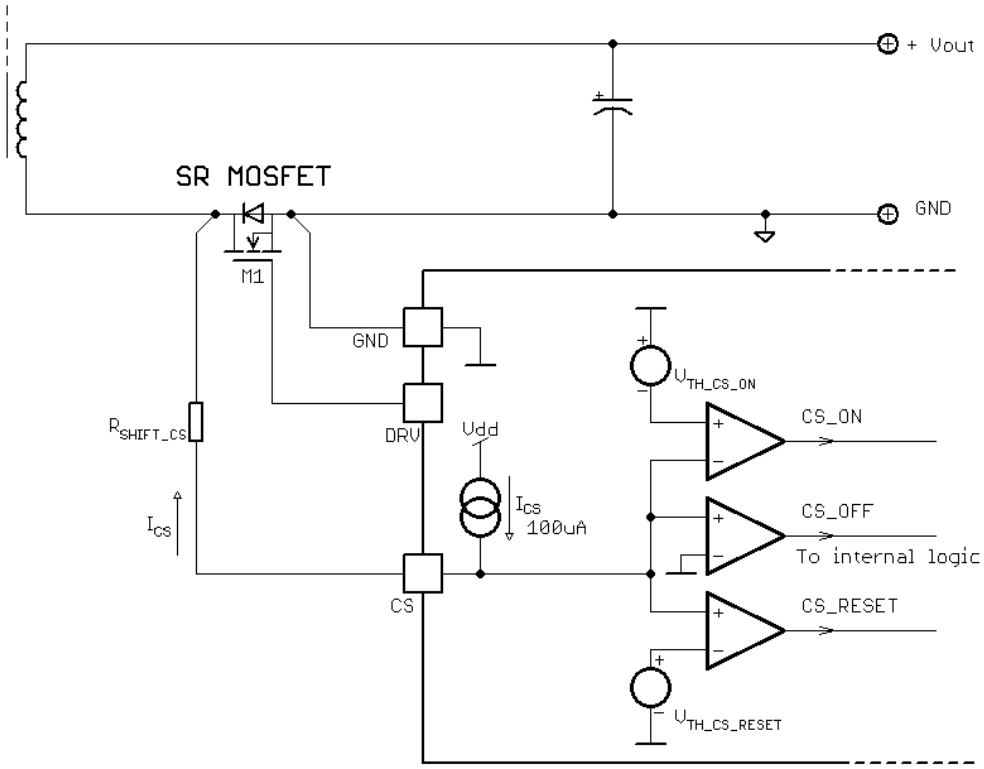


Figure 44. Current Sensing Circuitry Functionality

The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than $V_{TH\_CS\_OFF}$ (typically −0.5 mV minus any voltage dropped on the optional R_{SHIFT_CS}). For the same ringing reason, a minimum off-time timer is asserted once the V_{CS} goes above $V_{TH\_CS\_RESET}$. The minimum off-time can be externally adjusted using R_{MIN_TOFF} resistor. The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 45). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn-off. The R_{SHIFT_CS} resistor provides the designer with the possibility to modify (increase) the actual turn−on and turn−off secondary current thresholds. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH\_CS\_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH\_CS\_RESET}$.

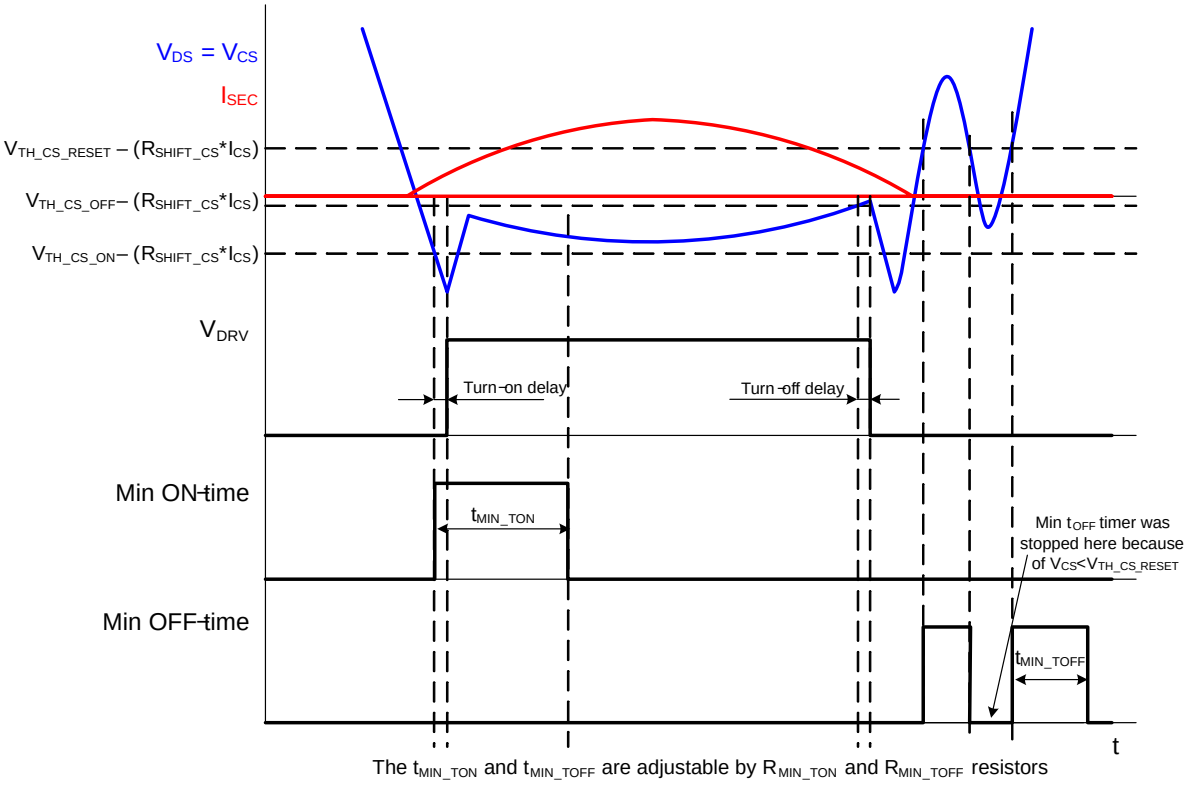


Figure 45. CS Input Comparators Thresholds and Blanking Periods Timing in LLC

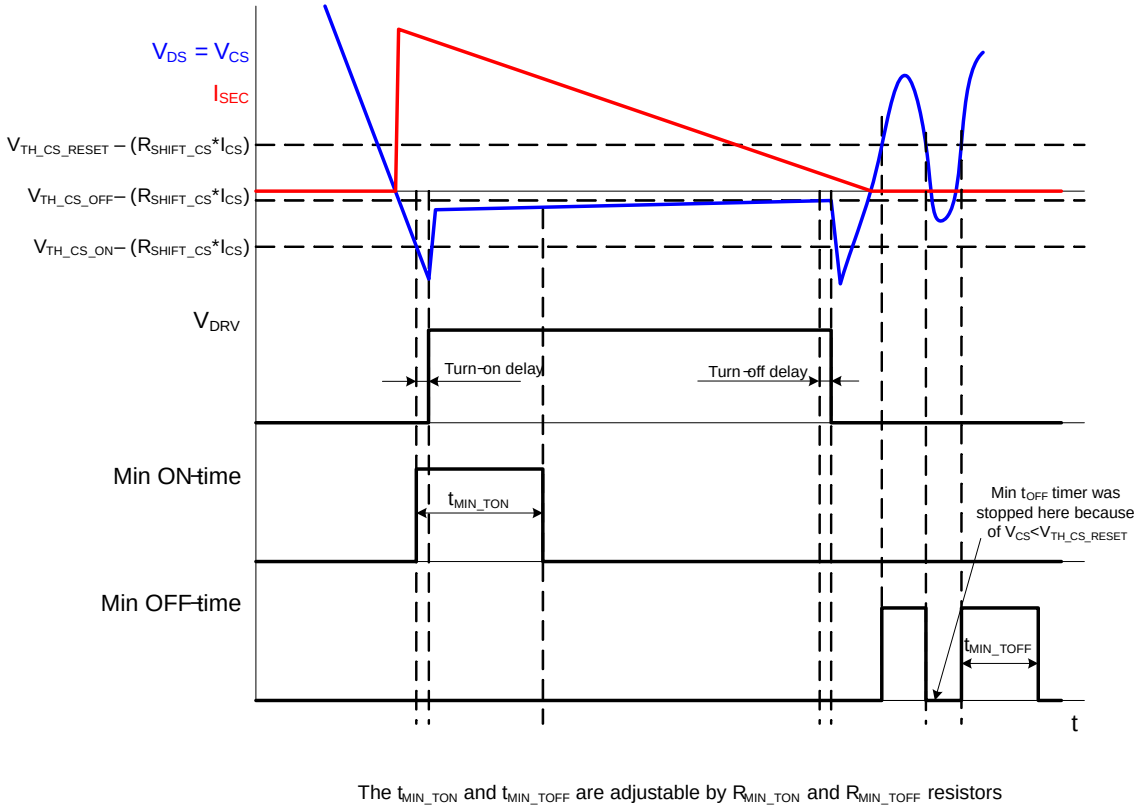


Figure 46. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

If no R_{SHIFT_CS} resistor is used, the turn-on, turn-off and $V_{TH\_CS\_RESET}$ thresholds are fully given by the CS input specification (please refer to electrical characteristics table). The CS pin offset current causes a voltage drop that is equal to:

$$V_{RSHIFT\_CS} = R_{SHIFT\_CS} * I_{CS} \quad \text{(eq. 1)}$$

Final turn−on and turn off thresholds can be then calculated as:

$$V_{CS\_TURN\_ON} = V_{TH\_CS\_ON} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 2)}$$

$$V_{CS\_TURN\_OFF} = V_{TH\_CS\_OFF} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 3)}$$

$$V_{CS\_RESET} = V_{TH\_CS\_RESET} - \left(R_{SHIFT\_CS} * I_{CS}\right) \quad \text{(eq. 4)}$$

Note that R_{SHIFT_CS} impact on turn-on and $V_{TH\_CS\_RESET}$ thresholds is less critical than its effect on the turn−off threshold.

It should be noted that when using a SR MOSFET in a through hole package the parasitic inductance of the MOSFET package leads (refer to Figure 47) causes a turn−off current threshold increase. The current that flows through the SR MOSFET experiences a high $\Delta i(t)/\Delta t$ that induces an error voltage on the SR MOSFET leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized − refer to Figure 48 for a better understanding.

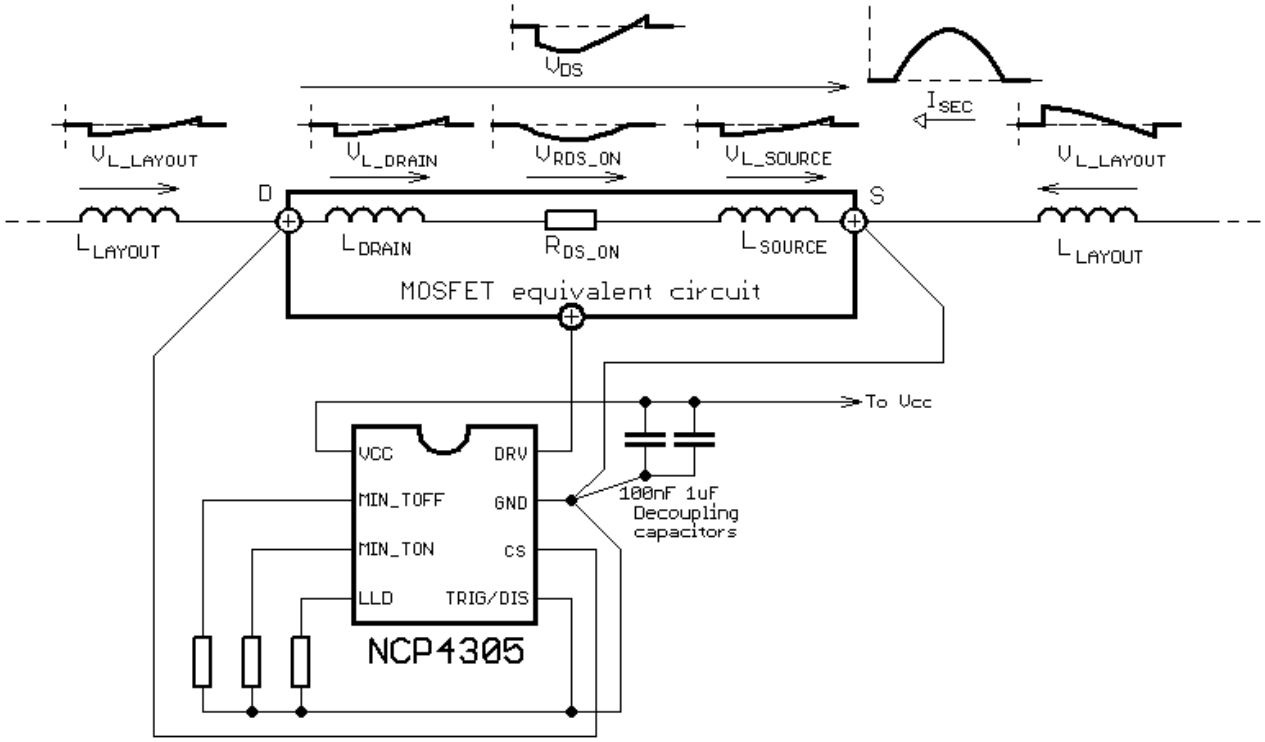


Figure 47. SR System Connection Including MOSFET and Layout Parasitic Inductances in LLC Application

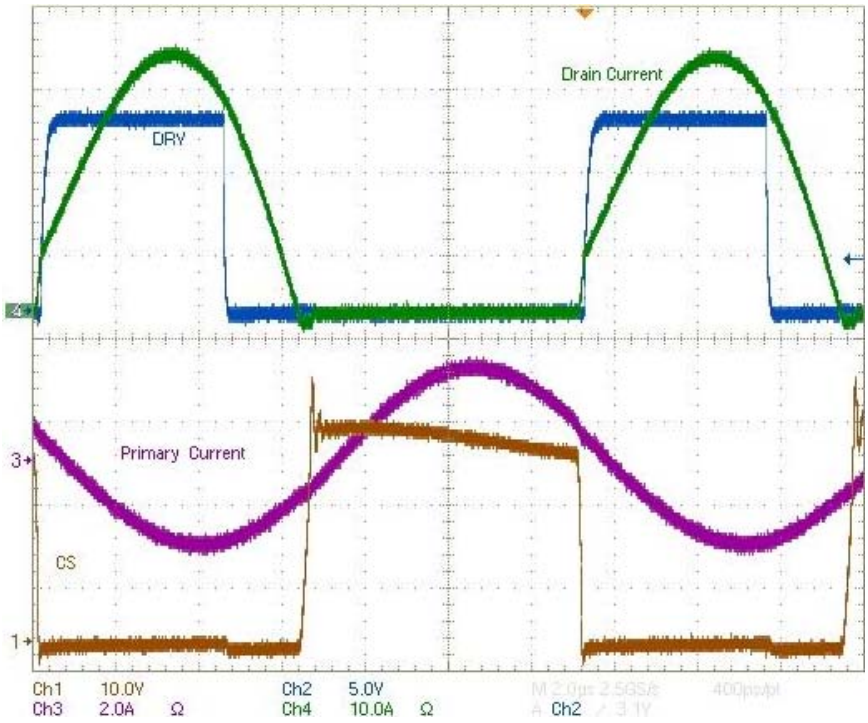


Figure 48. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads − SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs $R_{DS(on)}$ and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current $\Delta i/\Delta t$ and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 49).

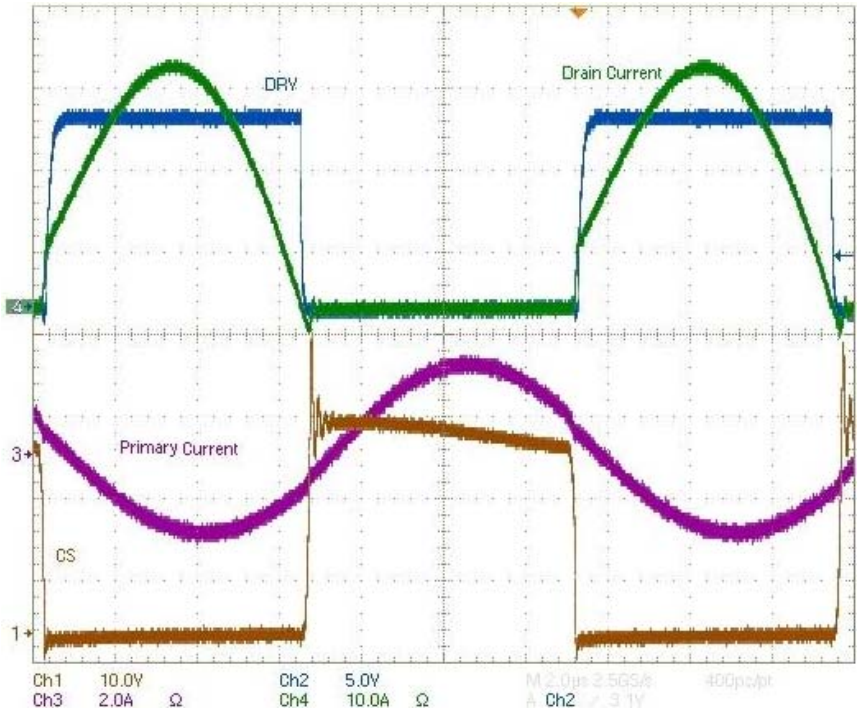


Figure 49. Waveforms from SR System Implemented in LLC Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance − SR MOSFET Channel Conduction Time is Optimized

It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn−off threshold precision is quite critical. If we consider a SR MOSFET with $R_{DS(on)}$ of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn-off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn-off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive − even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point − refer to Figure 47. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 50 and Figure 51 show examples of SR system layouts using MOSFETs in TO220 and SMT packages. It is evident that the MOSFET leads should be as short as possible to minimize parasitic inductances when using packages with leads (like TO220). Figure 51 shows how to layout design with two SR MOSFETs in parallel. It has to be noted that it is not easy task and designer has to paid lot of attention to do symmetric Kelvin connection.

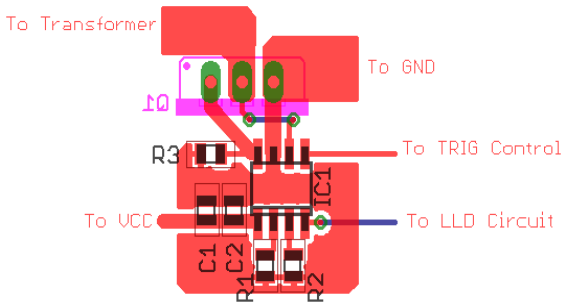


Figure 50. Recommended Layout When Using SR MOSFET in TO220 Package

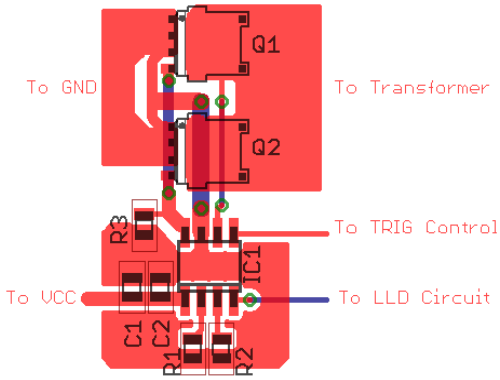


Figure 51. Recommended Layout When Using SR MOSFET in SMT Package (2x SO8 FL)

Trigger/Disable input

The NCP4305 features an ultrafast trigger input that exhibits a maximum of t_{PD_TRIG} delay from its activation to the start of SR MOSFET turn−off of process. This input can be used in applications operated in deep Continues Conduction Mode (CCM) to further increase efficiency and/or to activate disable mode of the SR driver in which the consumption of the NCP4305 is reduced to maximum of I_{CC_DIS}.

NCP4305 is capable to turn−off the SR MOSFET reliably in CCM applications just based on CS pin information only, without using the trigger input. However, natural delay of the ZCD comparator and DRV turn−off delay increase overlap between primary and secondary MOSFETs switching (also known as cross conduction). If one wants to achieve absolutely maximum efficiency with deep CCM applications, then the trigger signal coming from the primary side should be applied to the trigger pin. The trigger input then turns the SR MOSFET off slightly before the secondary winding voltage reverses. There are several possibilities for transferring the trigger signal from the primary to the secondary side − refer to Figures 66 and 67.

The trigger signal is blanked for $t_{TRIGBLANK}$ after the DRV turn−on process has begun. The blanking technique is used to increase trigger input noise immunity against the parasitic ringing that is present during the turn on process due to the SMPS layout. The trigger input is supersedes the CS input except trigger blanking period. TRIG/DIS signal turns the SR MOSFET off or prohibits its turn−on when the Trigger/Disable pin is pulled above V_{TRIG_TH}.

The SR controller enters disable mode when the trigger pin is pulled−up for more than t_{DIS_TIM}. In disable mode the IC consumption is significantly reduced. To recover from disable mode and enter normal operation, the TRIG/DIS pin is pulled low at least for t_{DIS_END}.

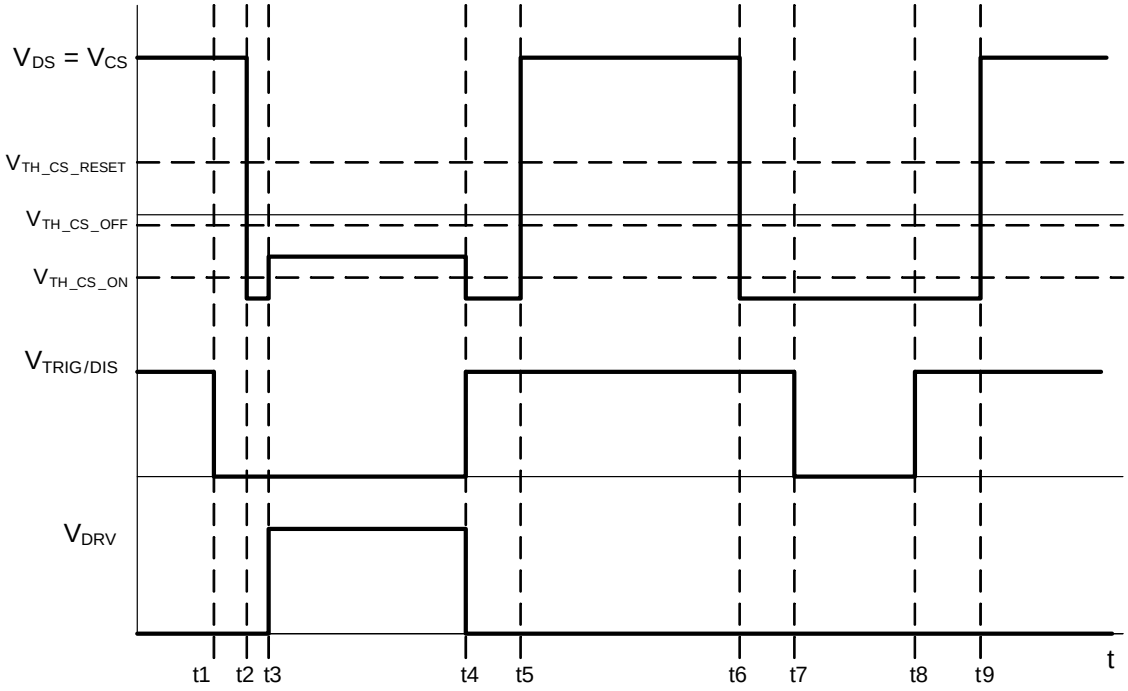


Figure 52. Trigger Input Functionality Waveforms Using the Trigger to Turn−off and Block the DRV Signal

Figure 52 shows basic Trigger/Disable input functionality. At t1 the Trigger/Disable pin is pulled low to enter into normal operation. At t2 the CS pin is dropped below the $V_{TH\_CS\_ON}$, signaling to the NCP4305 to start to turn the SR MOSFET on. At t3 the NCP4305 begins to drive the MOSFET. At t4, the SR MOSFET is conducting and the Trigger/Disable pin is pulled high. This high signal on the Trigger/Disable pin almost immediately turns off the drive to the SR MOSFET, turning off the MOSFET. The DRV is not turned−on in other case (t6) because the trigger pin is high in the time when CS pin signal crosses turn−on threshold. This figure clearly shows that the DRV can be asserted only on falling edge of the CS pin signal in case the trigger input is at low level (t2).

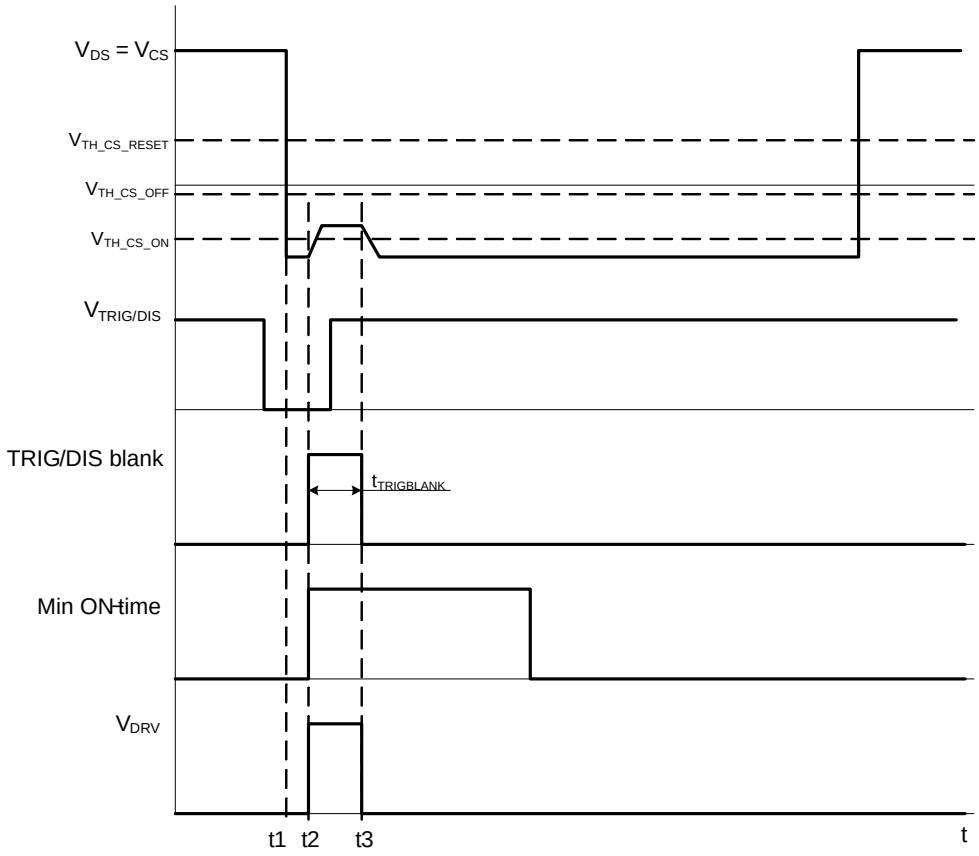


Figure 53. Trigger Input Functionality Waveforms − Trigger Blanking

In Figure 53 above, at time t1 the CS pin falls below the $V_{TH\_CS\_ON}$ while the Trigger is low setting in motion the DRV signal that appears at t2. At time t2 the DRV signal and Trigger blanking clock begin. Trigger/Disable signal goes high shortly after time t2. Due to the Trigger blanking clock (t_{TRIG_BLANK}) the Trigger's high signal does not affect the DRV signal until the $t_{TRIGBLANK}$ timer has expired. At time t3 the Trigger/Disable signal is re evaluated and the DRV signal is turned off. The TRIG/DIS input is blanked for $t_{TRIGBLANK}$ after DRV set signal to avoid undesirable behavior during SR MOSFET turn−on event. The blanking time in combination with high threshold voltage (V_{TRIG_TH}) prevent triggering on ringing and spikes that are present on the TRIG/DIS input pin during the SR MOSFET turn−on process. Controller's response to the narrow pulse on the Trigger/Disable pin is depicted in Figure 53 − this short trigger pulse enables to turn the DRV on for t_{TRIG_BLANK}. Note that this case is valid only if device not entered disable mode before.

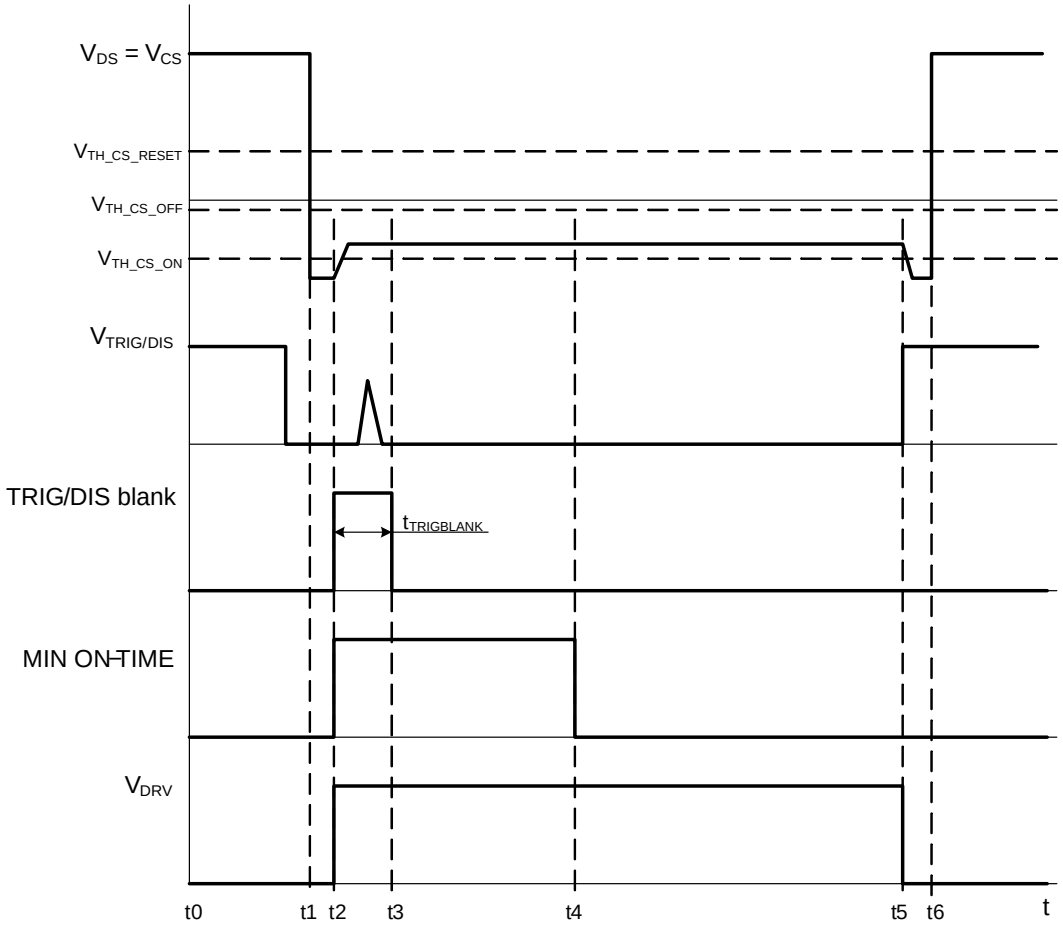


Figure 54. Trigger Input Functionality Waveforms − Trigger Blanking Acts Like a Filter

Figure 54 above shows almost the same situation as in Figure 53 with one main exception; the TRIG/DIS signal was not high after trigger blanking timer expired so the DRV signal remains high. The advantage of the trigger blanking time during DRV turn−on is evident from Figure 54 since it acts like a filter on the Trigger/Disable pin. Rising edge of the DRV signal may cause spikes on the trigger input. If it wasn't for the TRIG/DIS blanking these spikes, in combination with ultra−fast performance of the trigger logic, could turn the SR MOSFET off in an inappropriate time.

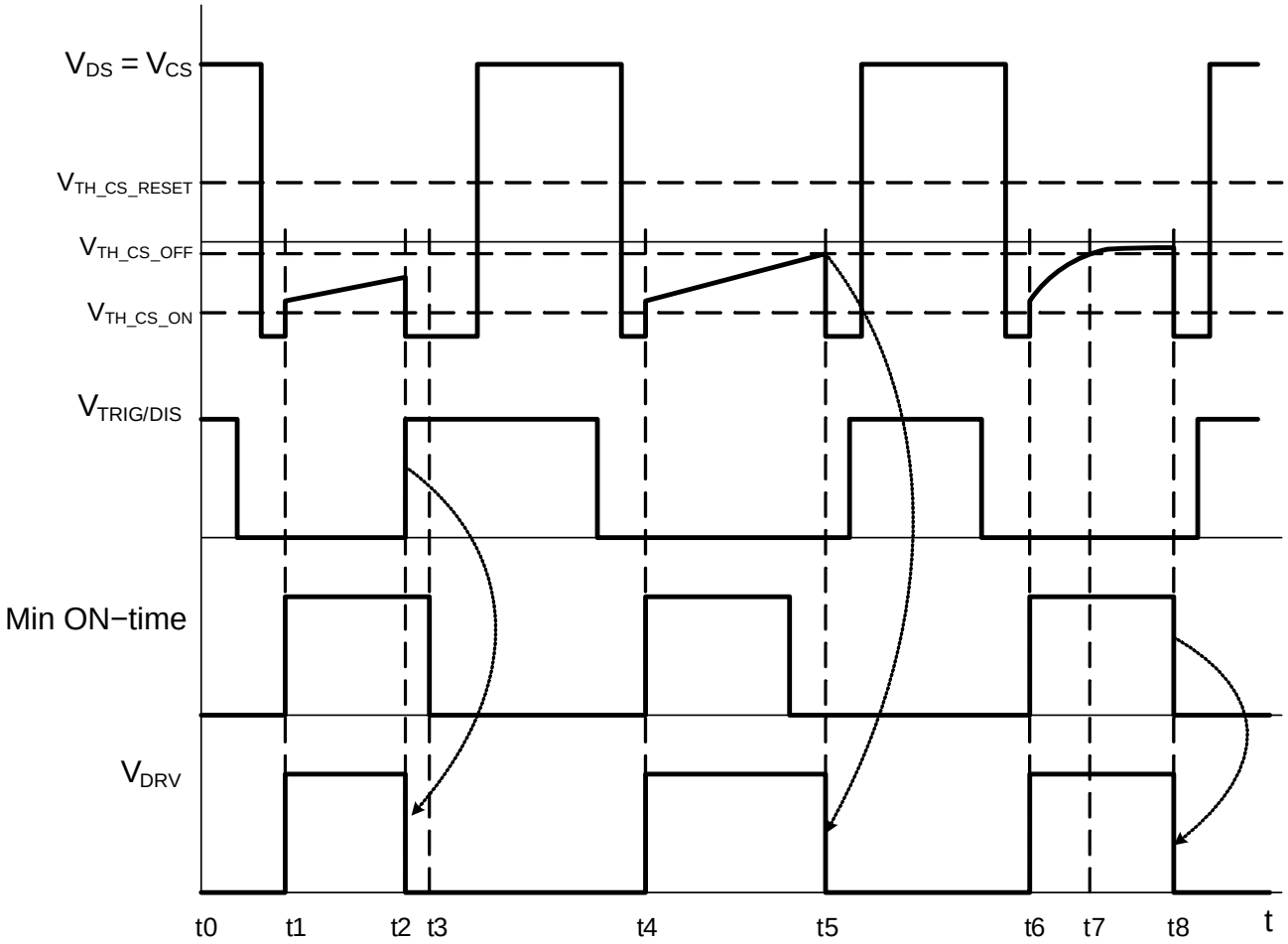


Figure 55. Trigger Input Functionality Waveforms − Trigger Over Ride, CS Turn Off and Min On−time

Figure 55 depicts all possible driver turn−off events in details when correct V_{CC} is applied. Controller driver is disabled based on trigger input signal in time t2; the trigger input overrides the minimum on−time period.

Driver is turned−off according to the CS (V_{DS}) signal (t5 marker) and when minimum on−time period elapsed already. TRIG/DIS signal needs to be LOW during this event.

If the CS (V_{DS}) voltage reaches $V_{TH\_CS\_OFF}$ threshold before minimum on−time period ends (t7) and the Trigger/Disable pin is low the DRV is turned−off on the falling edge of the minimum on−time period (t8 time marker in Figure 55). This demonstrates the fact that the Trigger over rides the minimum on−time. Minimum on−time has higher priority than the CS signal.

In Figure 56 the trigger input is low the whole time and the DRV pulses are purely a function of the CS signal and the minimum on−time. The first DRV pulse terminated based on the CS signal and another two DRV pulses are prolonged till the minimum on−time period end despite the CS signal crosses the $V_{TH\_CS\_OFF}$ threshold earlier.

If a minimum on−time is too long the situation that occurs after time marker t6 Figure 56 can occur, is not correct and should be avoided. The minimum t_{ON} period should be selected shorter to overcome situation that the SR MOSFET is turned−on for too long time. The secondary current then changes direction and energy flows back to the transformer that result in reduced application efficiency and also in excessive ringing on the primary and secondary MOSFETs.

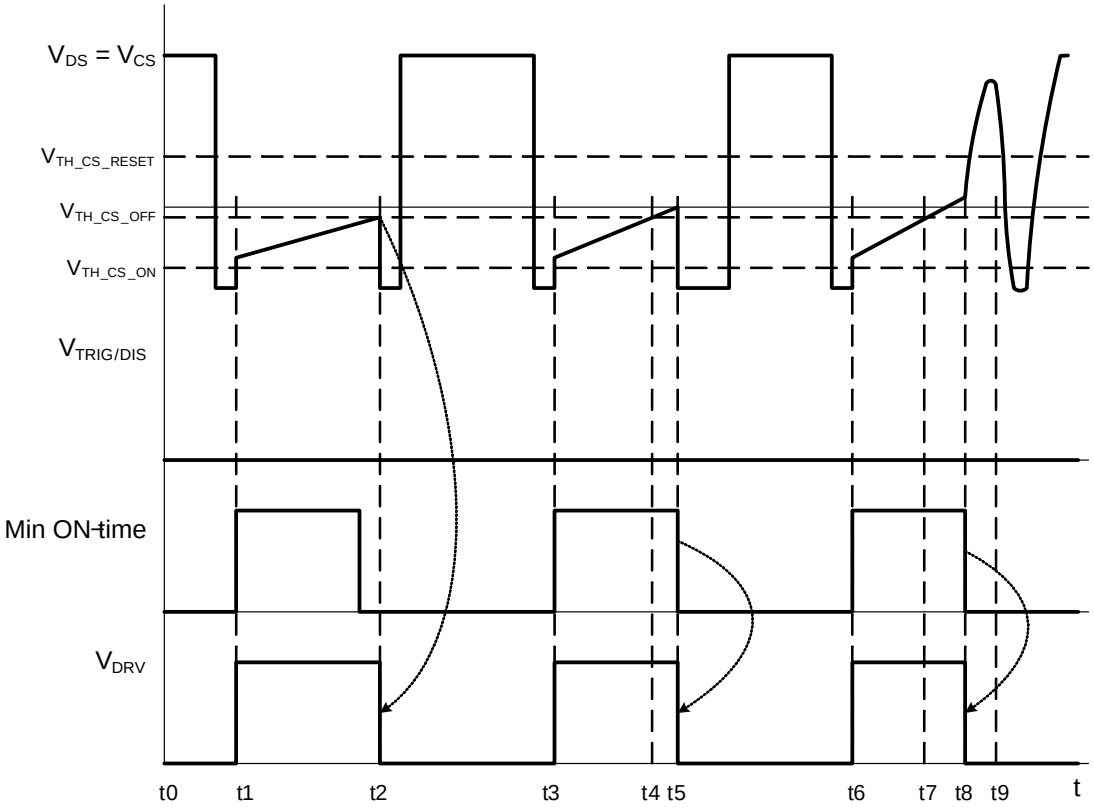


Figure 56. Minimum On−Time Priority

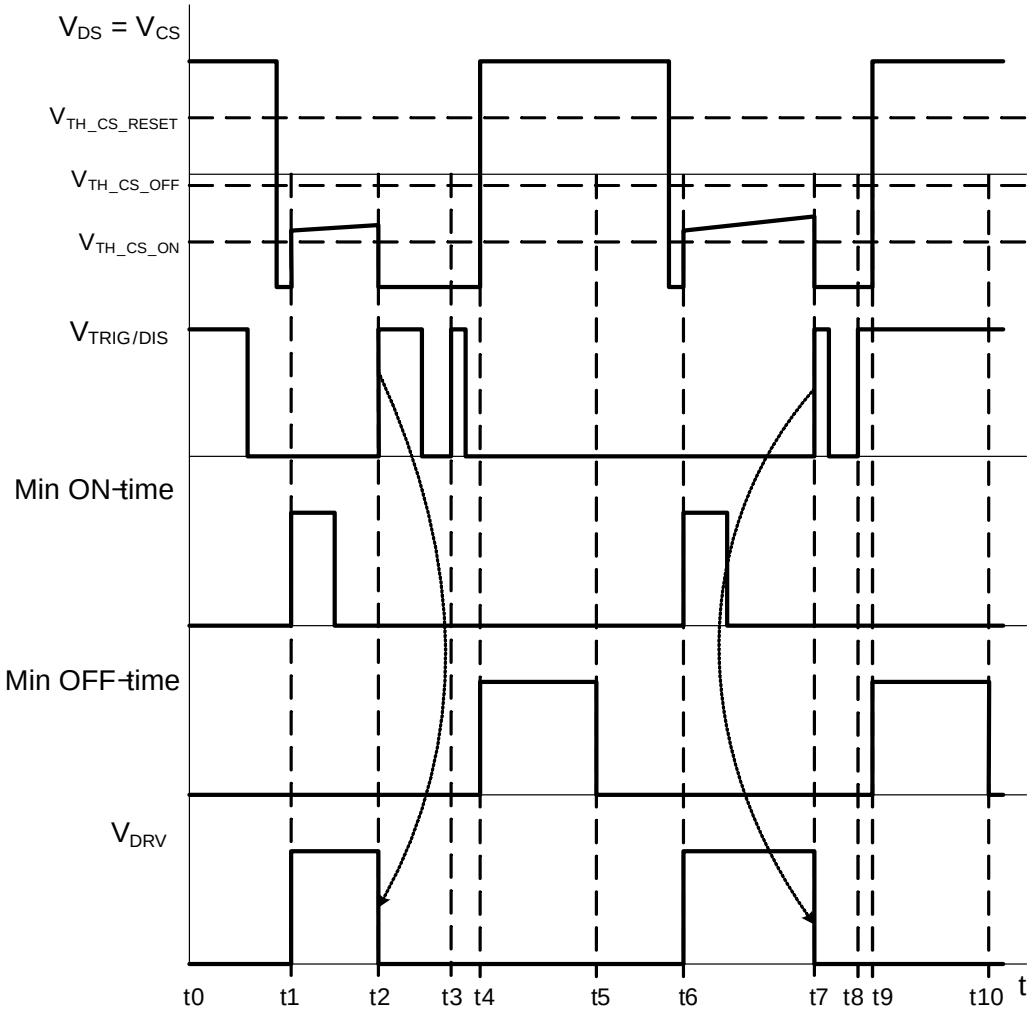


Figure 57. Trigger Input Functionality Waveforms − Two Pulses at One Cycle

Figure 57 shows IC behavior in case the trigger signal features two pulses during one cycle of the VDS (CS) signal. The trigger goes low enables the DRV just before time t1 and DRV turns−on because the VDS voltage drops under $V_{TH\_CS\_ON}$ threshold voltage. The trigger signal disables driver at time t2. The trigger drops down to LOW level in time t3, but IC waits for complete minimum off−time. Minimum off−time execution is blocked until CS pin voltage goes above $V_{TH\_CS\_RESET}$ threshold. Next cycle starts in time t6. The TRIG/DIS is low so driver is enabled and ready to be turned on when V_{DS} falls below $V_{TH\_CS\_ON}$ threshold voltage thus the driver is turned on at time t6. The trigger signal rises up to HIGH level at time t7, consequently DRV turns−off and IC waits for high CS voltage to start minimum off−time execution.

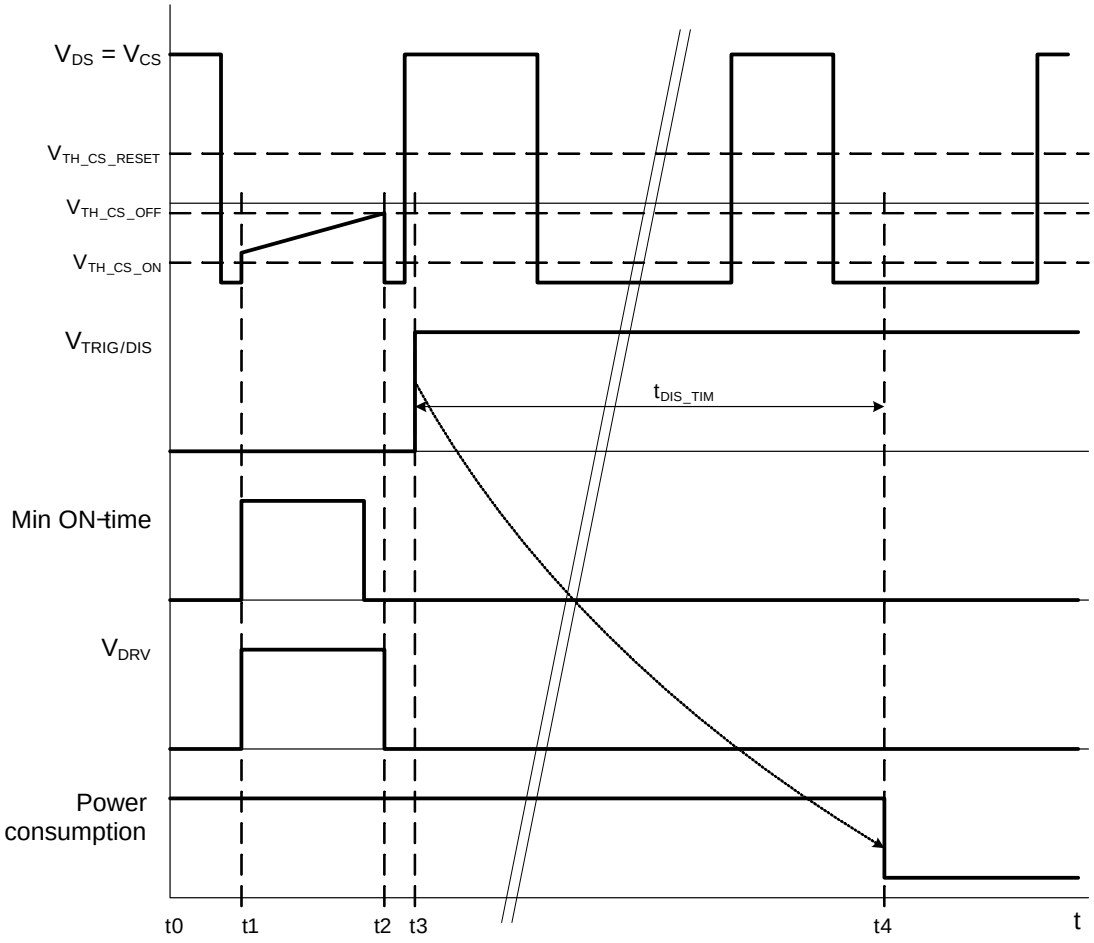


Figure 58. Trigger Input Functionality Waveforms − Disable Mode Activation

In Figure 58 above, at t2 the CS pin rises to $V_{TH\_CS\_OFF}$ and the SR MOSFET is turned−off. At t3 the TRIG/DIS signal is held high for more than t_{DIS_TIM}. NCP4305 enters disable mode after t_{DIS_TIM}. Driver output is disabled in disable mode. The DRV stays low (disabled) during transition to disable mode. Figure 59 shows disable mode transition 2nd case − i.e. when trigger rising edge comes during the trigger blank period. Figure 60 shows entering into disable mode and back to normal sequences.

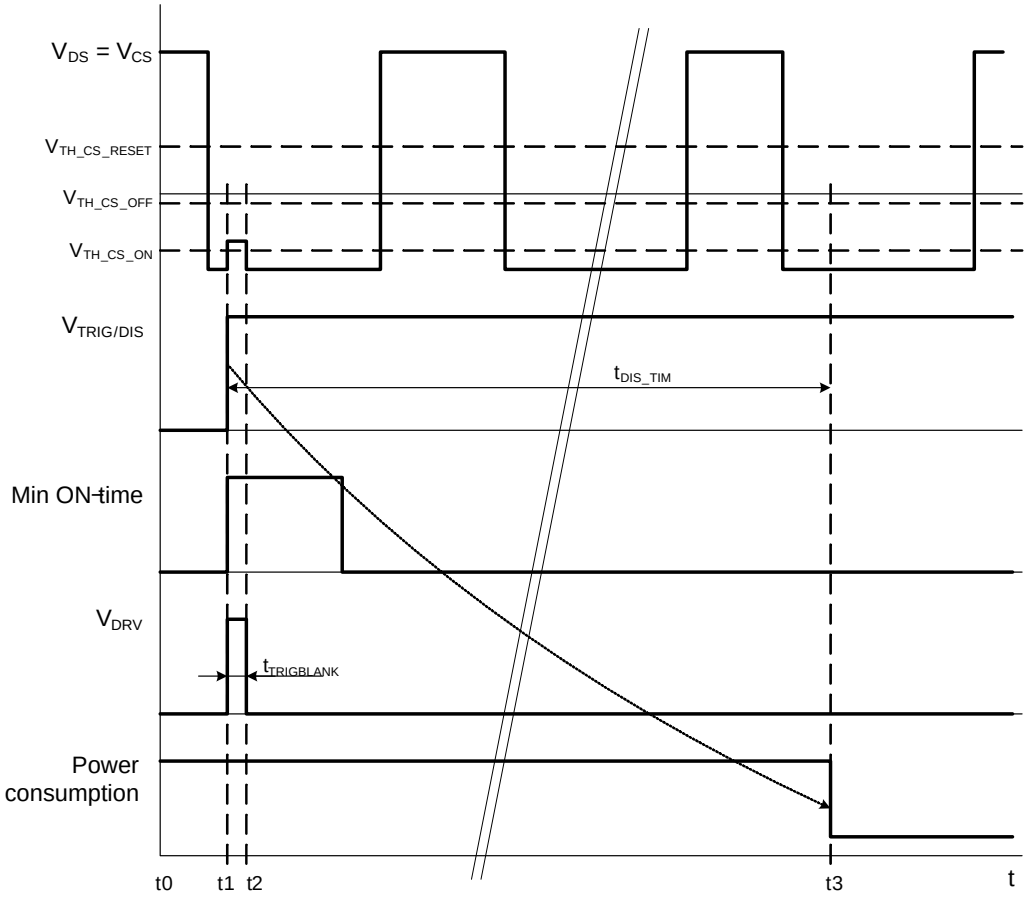


Figure 59. Trigger Input Functionality Waveforms − Disable Mode Clock Initiation

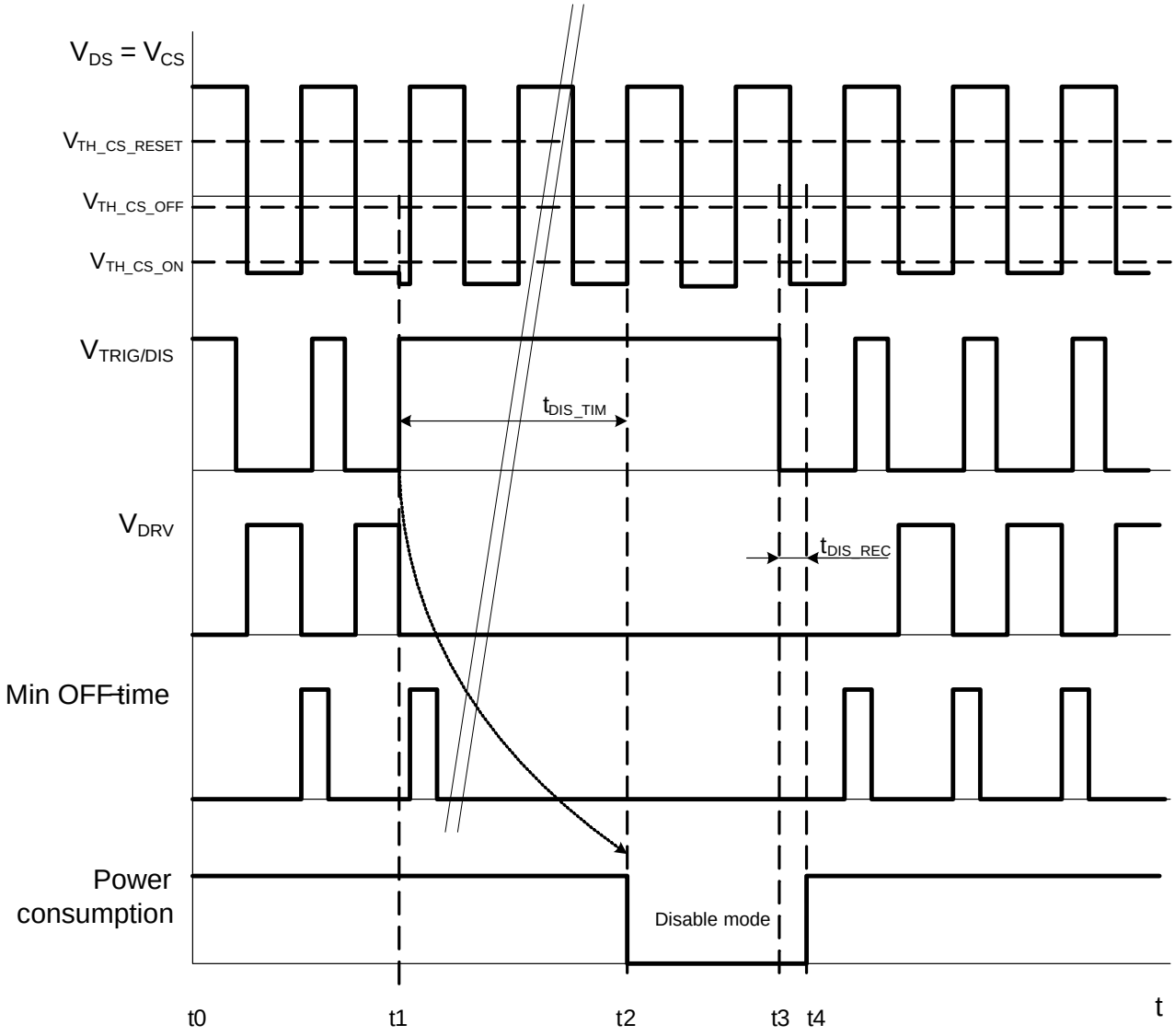


Figure 60. Trigger Input Functionality Waveforms − Disable and Normal Modes

Figures 61 and 62 shows exit from disable mode in detail. NCP4305 requires up to t_{DIS_REC} to recover all internal circuitry to normal operation mode when recovering from disable mode. The driver is then enabled after complete t_{MIN_TOFF} period when CS(V_{DS}) voltage is over $V_{TH\_CS\_RESET}$ threshold. Driver turns−on in the next cycle on CS (V_{DS}) falling edge signal only (t5 − Figure 61). The DRV stays low during recovery time period. Trigger input has to be low at least for t_{DIS_END} time to end disable mode and start with recovery. Trigger can go back high after t_{DIS_END} without recovery interruption.

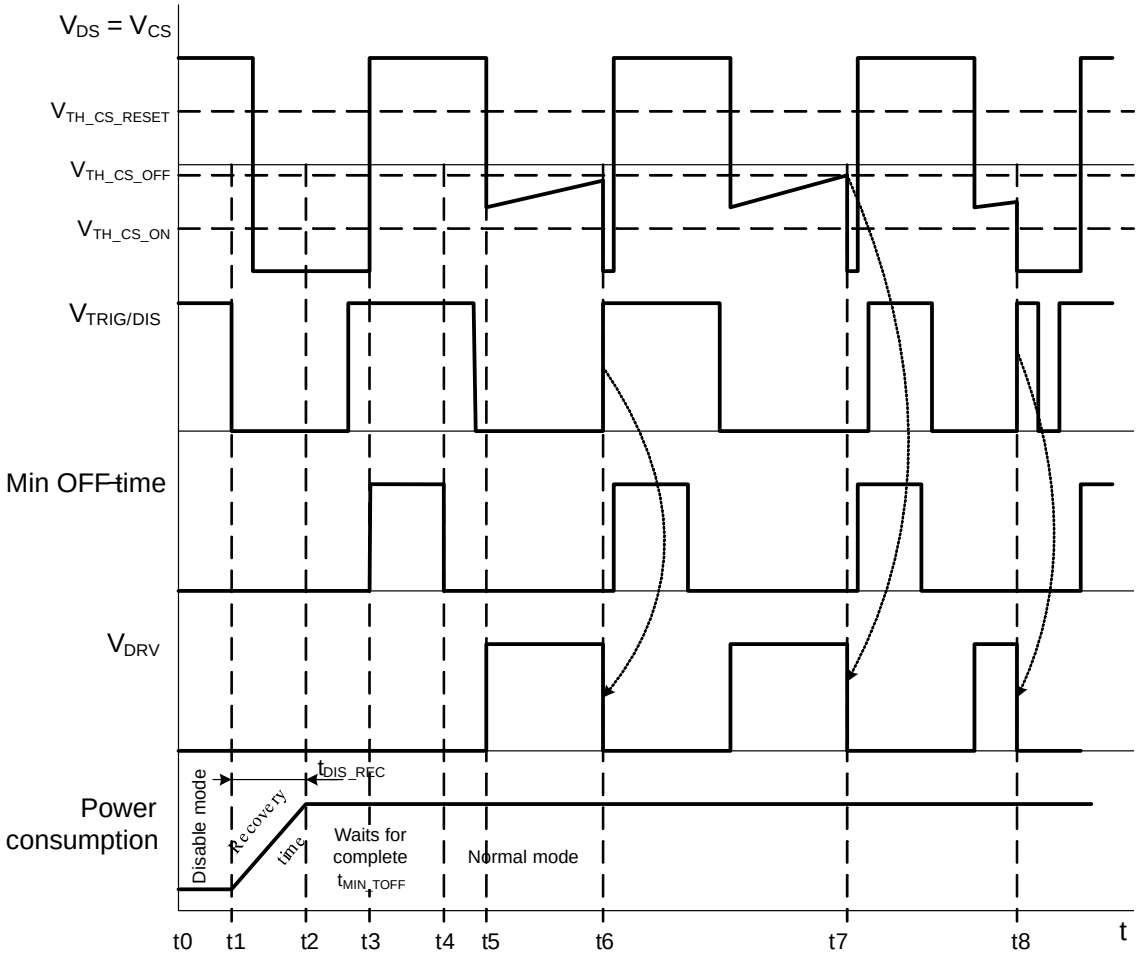


Figure 61. Trigger Input Functionality Waveforms − Exit from Disable Mode before the Falling Edge of the CS Signal

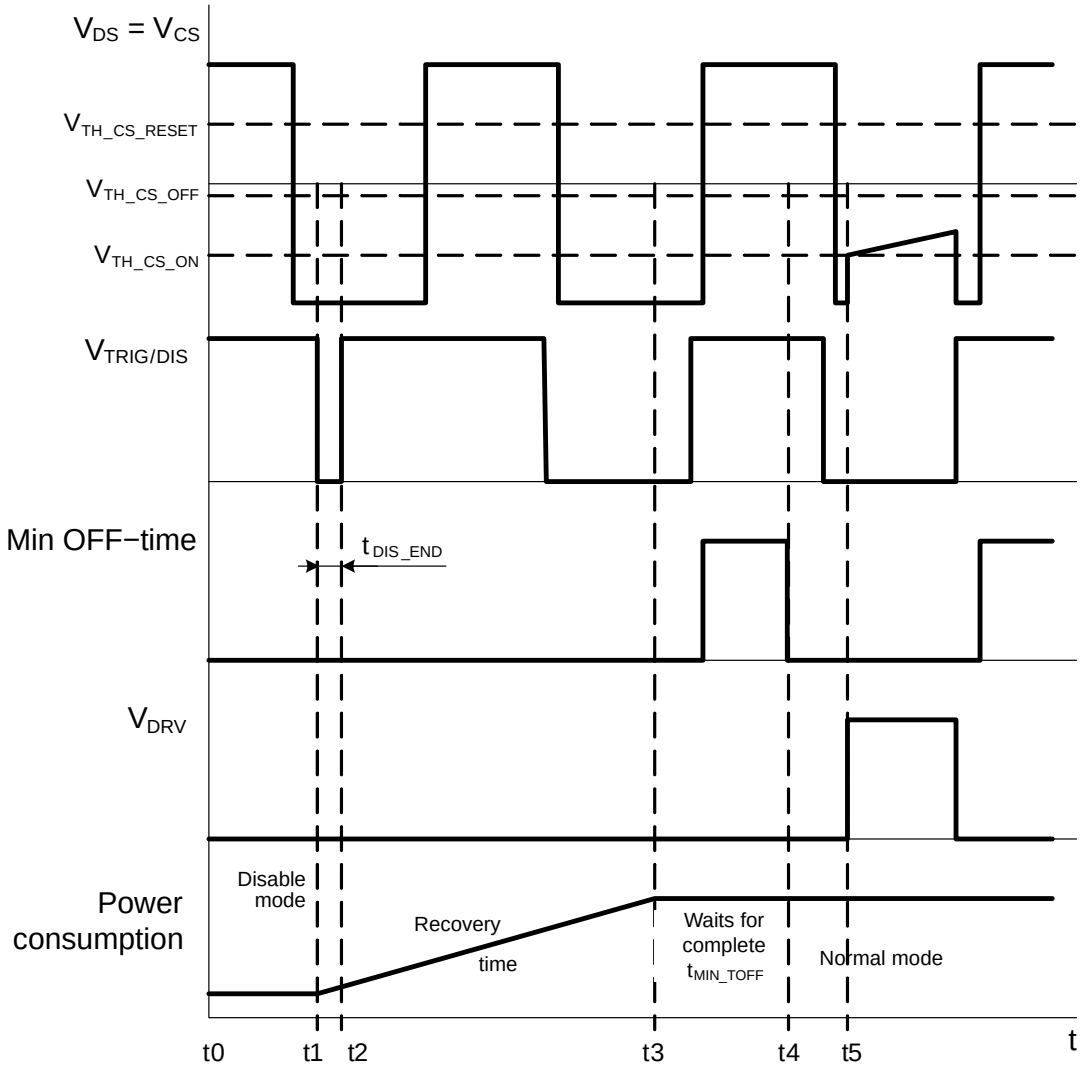


Figure 62. Trigger Input Functionality Waveforms

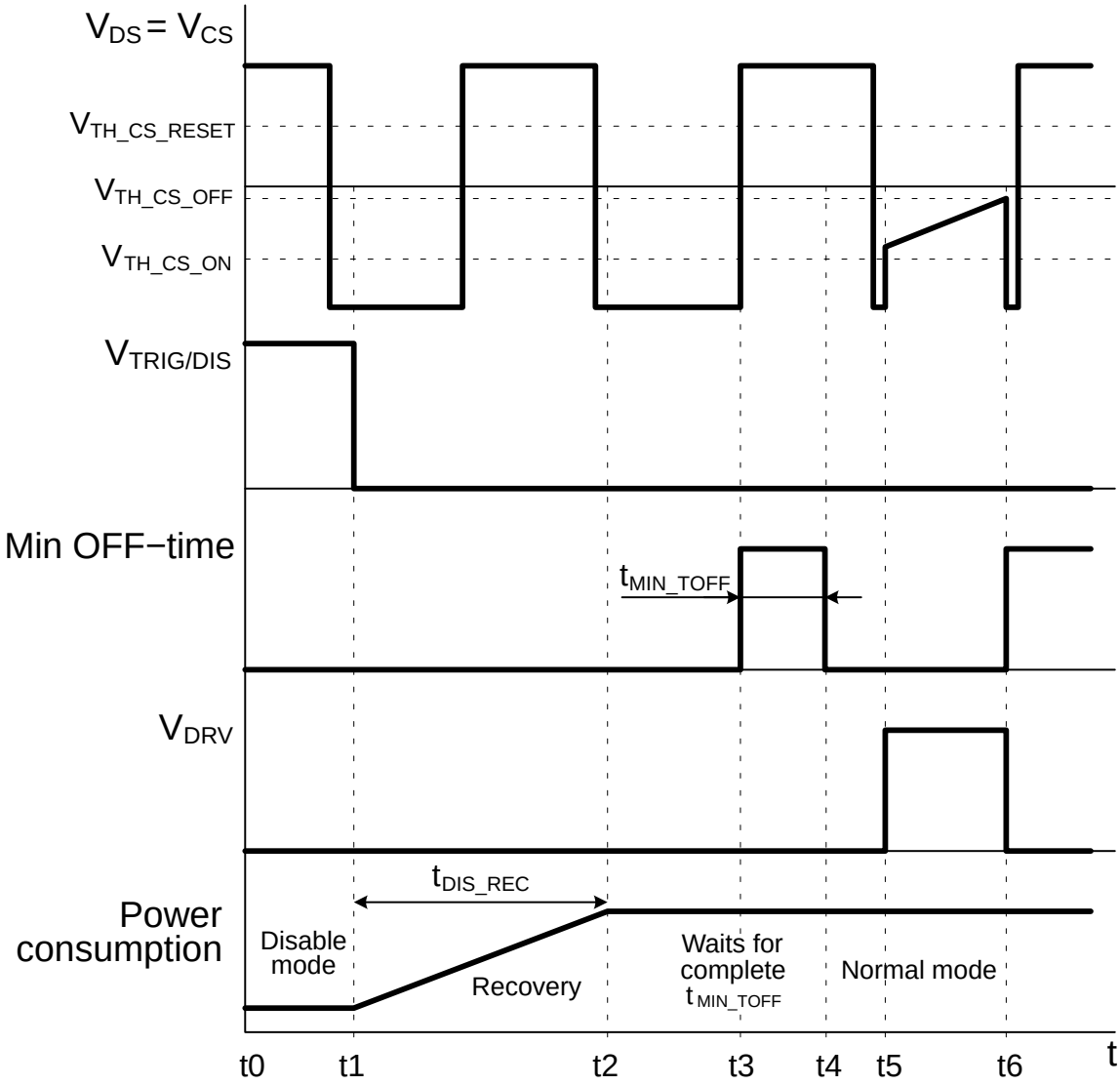


Figure 63. Trigger Input Functionality Waveforms

Figure 63 shows detail IC behavior after disable mode is ended. The trigger pin voltage goes low at t1 and after t_{DIS_REC} IC leaves disable mode (t2). V_{DS} voltage goes high again at time t3 and this event starts minimum off−time timer execution. Next V_{DS} falling edge below $V_{TH\_CS\_ON}$ level activates driver.

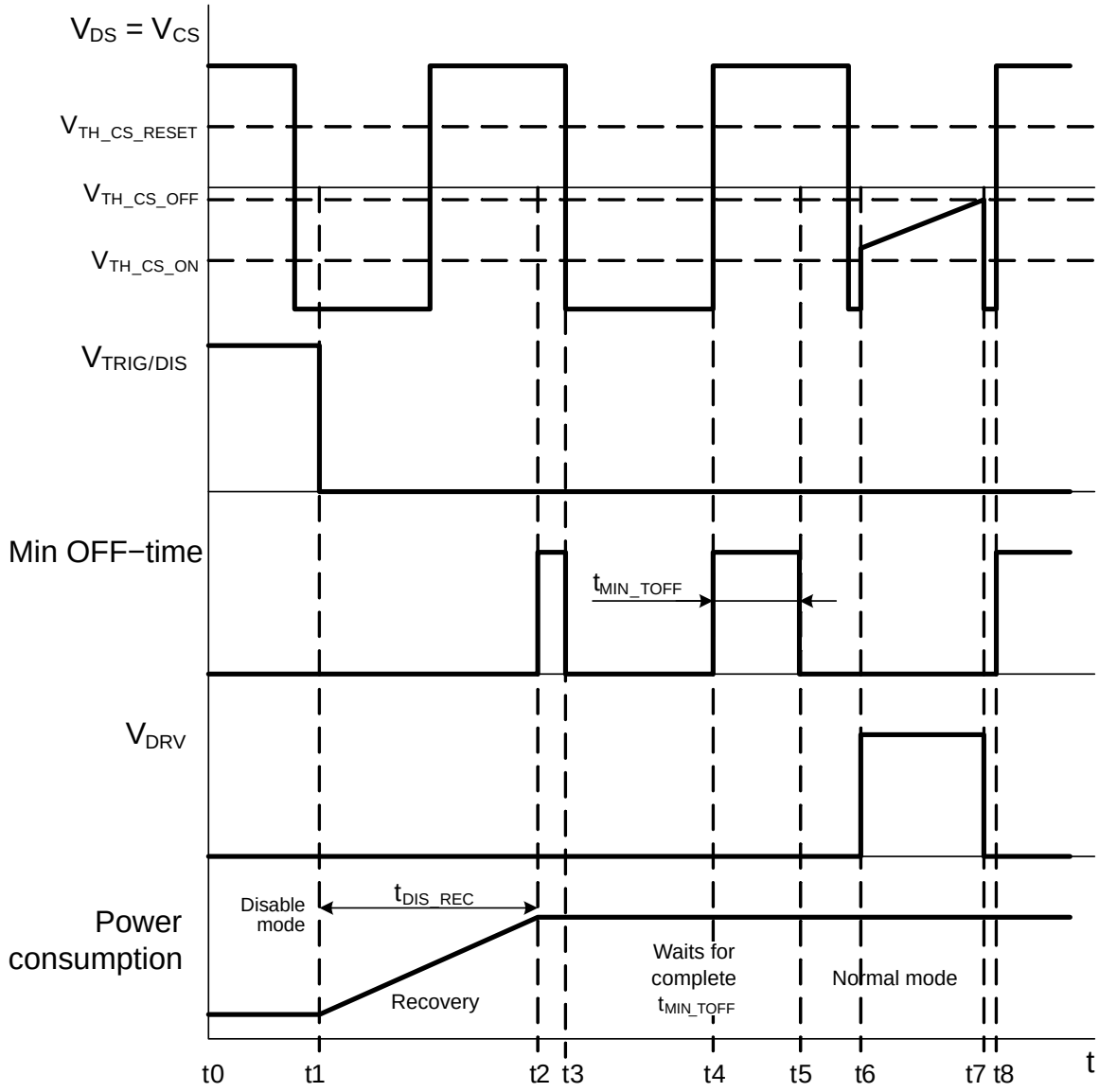


Figure 64. Trigger Input Functionality Waveforms

Different situation of leaving from disable mode is shown at Figure 64. Minimum off−time execution starts at time t2, but before time elapses V_{DS} voltage falls to negative voltage. This interrupts minimum off−time execution and the IC waits to another time when V_{DS} voltage is positive and then is again started the minimum off−time timer. The IC returns into normal mode after whole minimum off−time elapses.

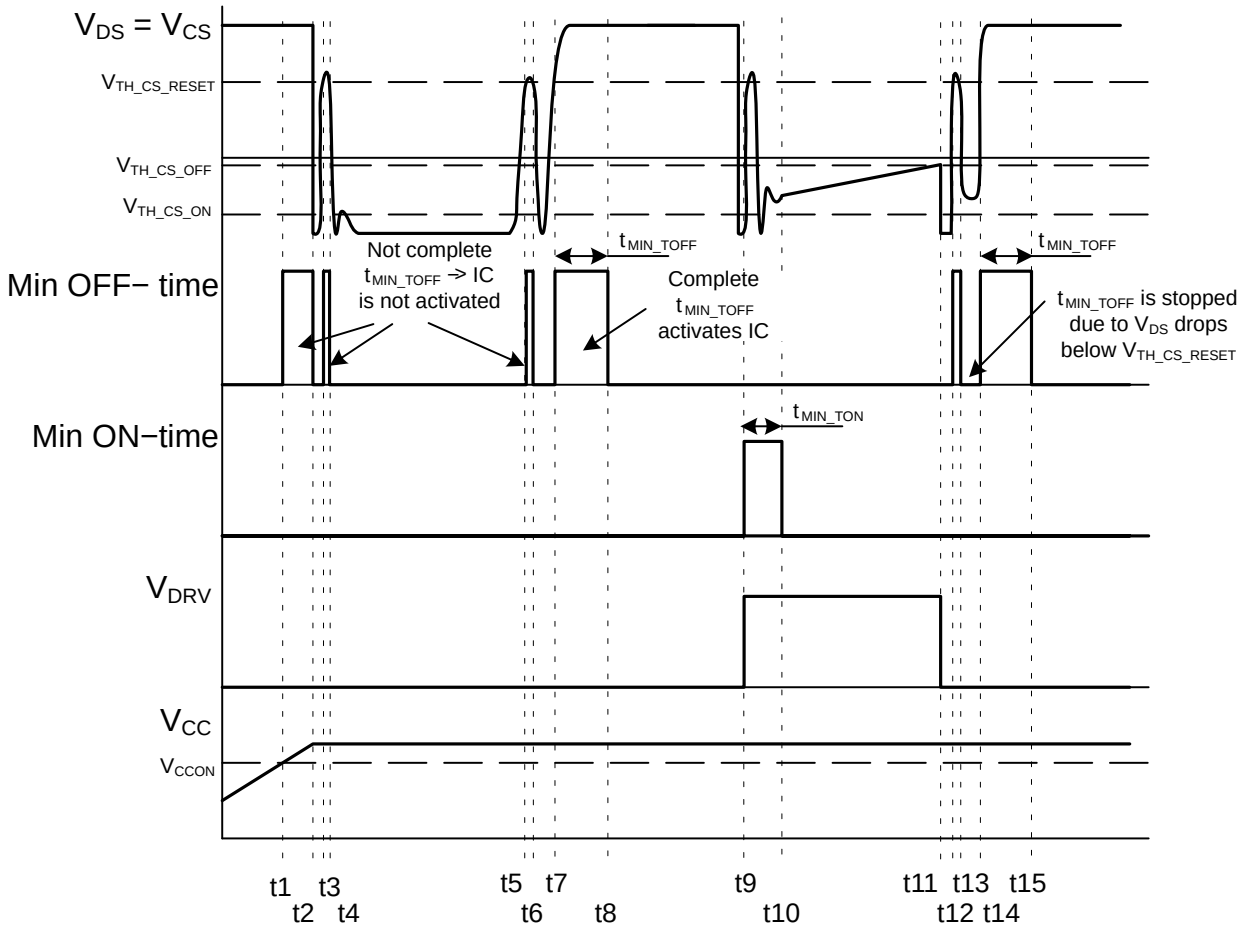


Figure 65. NCP4305 Operation after Start−Up Event

Start−up event waveforms are shown at Figure 65. A start−up event is very similar to an exit from disable mode event. The IC waits for a complete minimum off−time event (CS pin voltage is higher than $V_{TH\_CS\_RESET}$) until drive pulses can continue. Figure 65 shows how the minimum off−time timer is reset when CS voltage is oscillating through $V_{TH\_CS\_RESET}$ level. The NCP4305 starts operation at time t1 (time t1 can be seen as a wake−up event from the disable mode through TRIG/DIS or LLD pin). Internal logic waits for one complete minimum off−time period to expire before the NCP4305 can activate the driver after a start−up or wake−up event. The minimum off−time timer starts to run at time t1, because V_{CS} is higher than $V_{TH\_CS\_RESET}$. The timer is then reset, before its set minimum off−time period expires, at time t2 thanks to CS voltage lower than $V_{TH\_CS\_RESET}$ threshold. The aforementioned reset situation can be seen again at time t3, t4, t5 and t6. A complete minimum off−time period elapses between times t7 and t8 allowing the IC to activate a driver output after time t8.

The NCP4305 works very well in CCM application without any triggering method, but using some may improve overall operation. Typical application schematics of CCM flyback converters using two different primary triggering techniques can be seen in Figures 66 and 67. Both provided methods reduce the commutation losses and the SR MOSFET drain voltage spike, which results in improved efficiency.

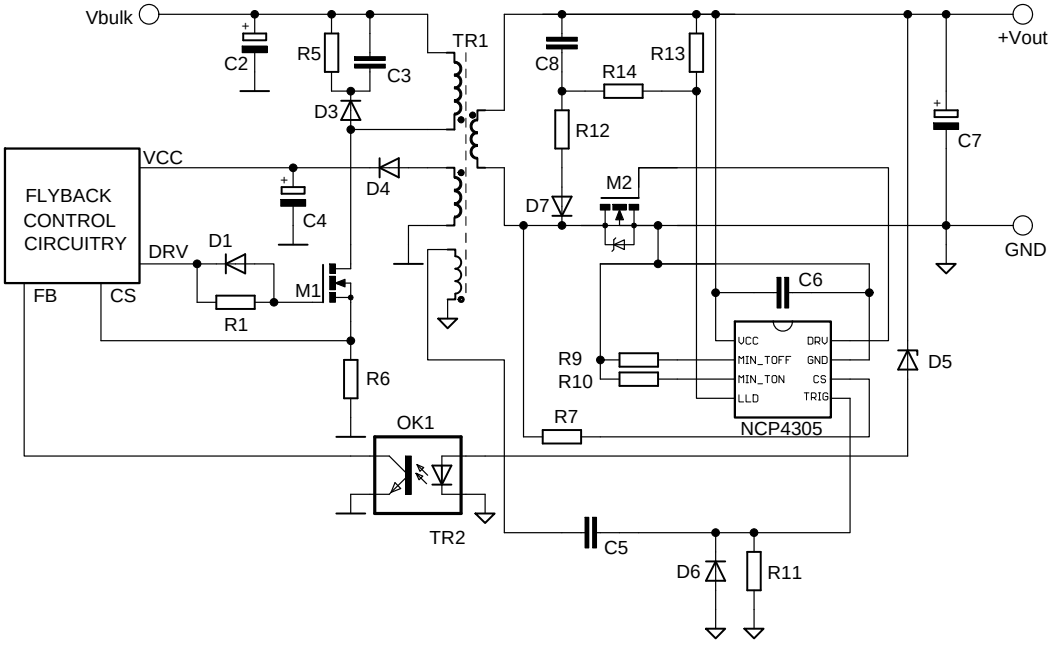


Figure 66. Primary Triggering in Deep CCM Application Using Auxiliary Winding − NCP4305A, B, C or D

The application shown in Figure 66 is simplest and the most cost effective solution for primary SR triggering. This method uses auxiliary winding made of triple insulated wire placed close to the primary winding section. This auxiliary winding provides information about primary turn−on event to the SR controller before the secondary winding reverses. This is possible thanks to the leakage between primary and secondary windings that creates natural delay in energy transfer. This technique provides approximately 0.5% efficiency improvement when the application is operated in deep CCM and a transformer that has a leakage of 1% of primary inductance is used.

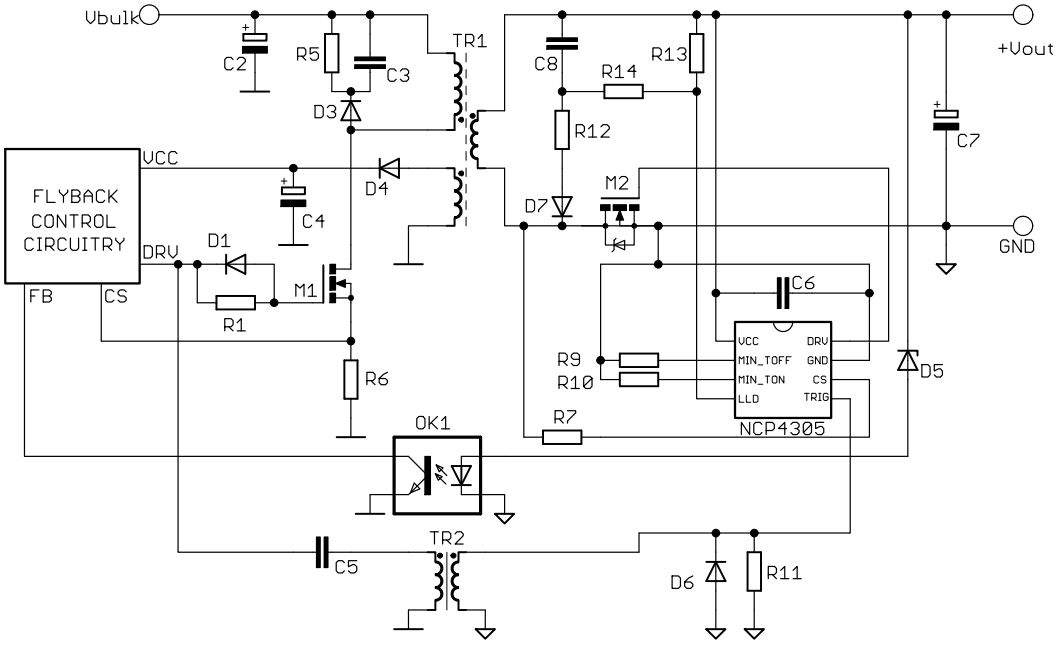


Figure 67. Primary Triggering in Deep CCM Application Using Trigger Transformer − NCP4305A, B, C or D

Application from Figure 67 uses an ultra−small trigger transformer to transfer primary turn−on information directly from the primary controller driver pin to the SR controller trigger input. Because the trigger input is rising edge sensitive, it is not necessary to transmit the entire primary driver pulse to the secondary. The coupling capacitor C5 is used to allow the trigger transformer's core to reset and also to prepare a needle pulse (a pulse with width shorter than

100 ns) to be transmitted to the NCP4305 trigger input. The advantage of needle trigger pulse usage is that the required volt−second product of the pulse transformer is very low and that allows the designer to use very small and cheap magnetic. The trigger transformer can even be prepared on a small toroidal ferrite core with outer diameter of 4 mm and four turns for primary and secondary windings to assure Lprimary = Lsecondary > 10 μH. Proper safety insulation between primary and secondary sides can be easily assured by using triple insulated wire for one or, better, both windings.

This primary triggering technique provides approximately 0.5% efficiency improvement when the application is operated in deep CCM and transformer with leakage of 1% of primary inductance is used.

It is also possible to use capacitive coupling (use additional capacitor with safety insulation) between the primary and secondary to transmit the trigger signal. We do not recommend this technique as the parasitic capacitive currents between primary and secondary may affect the trigger signal and thus overall system functionality.

Minimum t_{ON} and t_{OFF} Adjustment

The NCP4305 offers an adjustable minimum on−time and off−time blanking periods that ease the implementation of a synchronous rectification system in any SMPS topology. These timers avoid false triggering on the CS input after the MOSFET is turned on or off.

The adjustment of minimum t_{ON} and t_{OFF} periods are done based on an internal timing capacitance and external resistors connected to the GND pin − refer to Figure 68 for a better understanding.

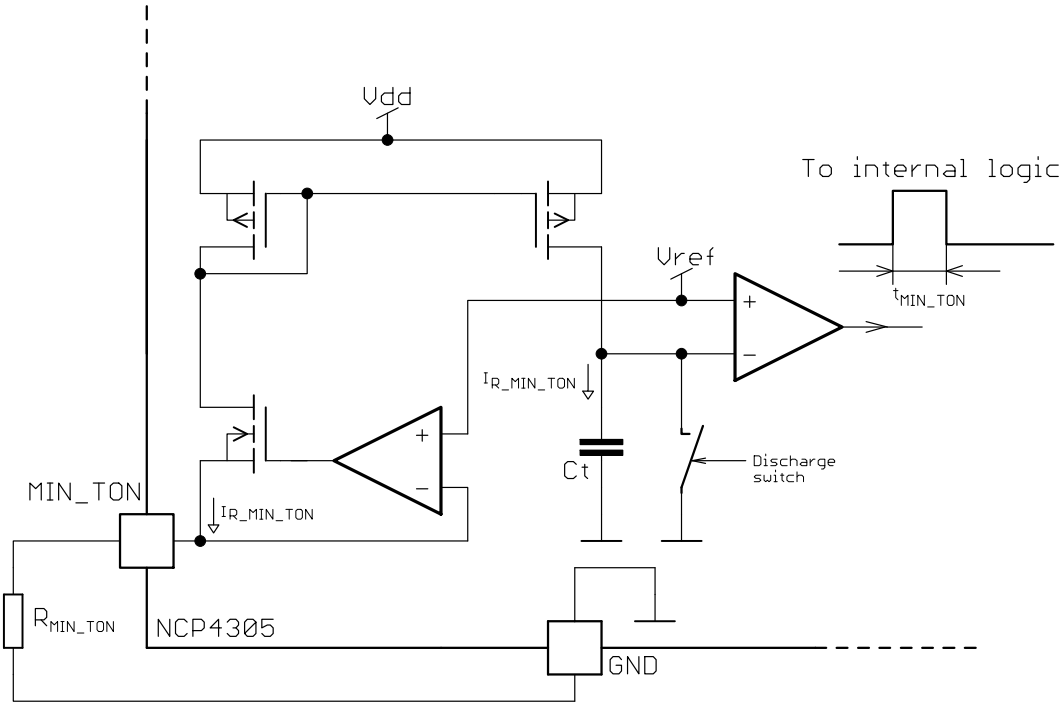


Figure 68. Internal Connection of the MIN_TON Generator (the MIN_TOFF Works in the Same Way)

Current through the MIN_TON adjust resistor can be calculated as:

$$I_{R\_MIN\_TON} = \frac{V_{ref}}{R_{Ton\_min}} \quad \text{(eq. 5)}$$

If the internal current mirror creates the same current through R_{MIN_TON} as used the internal timing capacitor (Ct) charging, then the minimum on−time duration can be calculated using this equation.

$$t_{MIN\_TON} = C_t \frac{V_{ref}}{I_{R\_MIN\_TON}} = C_t \frac{V_{ref}}{\frac{V_{ref}}{R_{MIN\_TON}}} = C_t \cdot R_{MIN\_TON} \quad \text{(eq. 6)}$$

The internal capacitor size would be too large if $I_{R\_MIN\_TON}$ was used. The internal current mirror uses a proportional current, given by the internal current mirror ratio. One can then calculate the MIN_TON and MIN_TOFF blanking periods using below equations:

$$t_{MIN\_TON} = 1.00 * 10^{-4} * R_{MIN\_TON}\ [\mu s] \quad \text{(eq. 7)}$$

$$t_{MIN\_TOFF} = 1.00 * 10^{-4} * R_{MIN\_TOFF}\ [\mu s] \quad \text{(eq. 8)}$$

Note that the internal timing comparator delay affects the accuracy of Equations 7 and 8 when MIN_TON/ MIN_TOFF times are selected near to their minimum possible values. Please refer to Figures 69 and 70 for measured minimum on and off time charts.

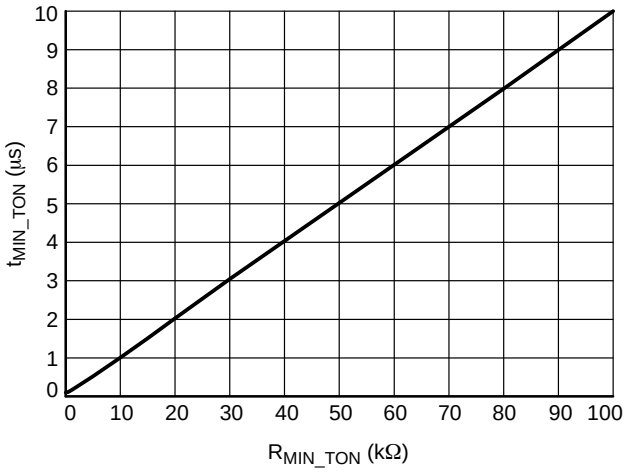


Figure 69. MIN_TON Adjust Characteristics

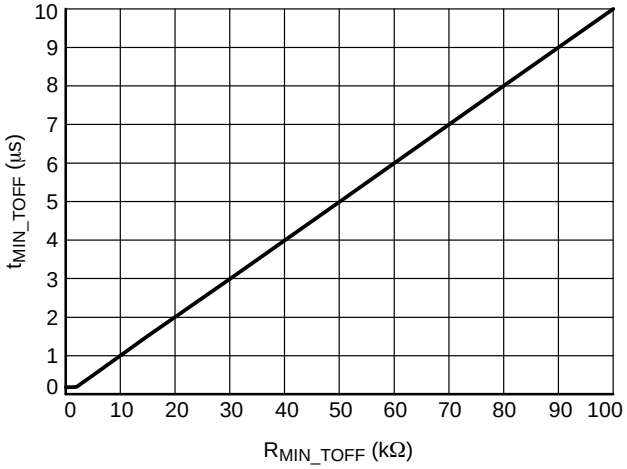


Figure 70. MIN_TOFF Adjust Characteristics

The absolute minimum t_{ON} duration is internally clamped to 55 ns and minimum t_{OFF} duration to 245 ns in order to prevent any potential issues with the MIN_TON and/or MIN_TOFF pins being shorted to GND.

The NCP4305 features dedicated anti−ringing protection system that is implemented with a MIN_TOFF blank generator. The minimum off−time one−shot generator is restarted in the case when the CS pin voltage crosses $V_{TH\_CS\_RESET}$ threshold and MIN_TOFF period is active. The total off-time blanking period is prolonged due to the ringing in the application (refer to Figure 45).

Some applications may require adaptive minimum on and off time blanking periods. With NCP4305 it is possible to modulate blanking periods by using an external NPN transistor − refer to Figure 71. The modulation signal can be derived based on the load current, feedback regulator voltage or other application parameter.

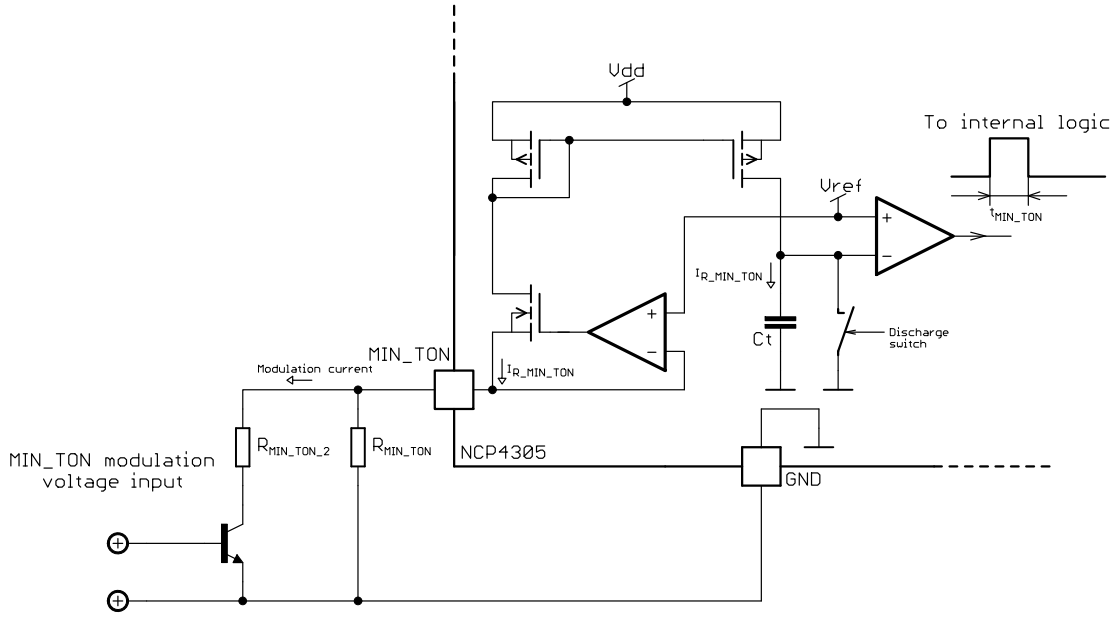


Figure 71. Possible Connection for MIN_T_{ON} and MIN_T_{OFF} Modulation

Maximum t_{ON} adjustment

The NCP4305Q offers an adjustable maximum on−time (like the min_t_{ON} and min_t_{OFF} settings shown above) that can be very useful for QR controllers at high loads. Under high load conditions the QR controller can operate in CCM thanks to this feature. The NCP4305Q version has the ability to turn−off the DRV signal to the SR MOSFET before the secondary side current reaches zero. The DRV signal from the NCP4305Q can be fed to the primary side through a pulse transformer (see Figure 4 for detail) to a transistor on the primary side to emulate a ZCD event before an actual ZCD event occurs. This feature helps to keep the minimum switching frequency up so that there is better energy transfer through the transformer (a smaller transformer core can be used). Also another advantage is that the IC controls the SR MOSFET and turns off from secondary side before the primary side is turned on in CCM to ensure no cross conduction. By controlling the SR MOSFET's turn off before the primary side turn off, producing a zero cross conduction operation, this will improve efficiency.

The Internal connection of the MAX_TON feature is shown in Figure 72. Figure 72 shows a method that allows for a modification of the maximum on−time according to output voltage. At a lower V_{OUT}, caused by hard overload or at startup, the maximum on−time should be longer than at nominal voltage. Resistor R_A can be used to modulate maximum on−time according to V_{OUT} or any other parameter.

The operational waveforms at heavy load in QR type SMPS are shown in Figure 73. After t_{MAX_TON} time is exceeded, the synchronous switch is turned off and the secondary current is conducted by the diode. Information about turned off SR MOSFET is transferred by the DRV pin through a small pulse transformer to the primary side where it acts on the ZCD detection circuit to allow the primary switch to be turned on. Secondary side current disappears before the primary switch is turned on without a possibility of cross current condition.

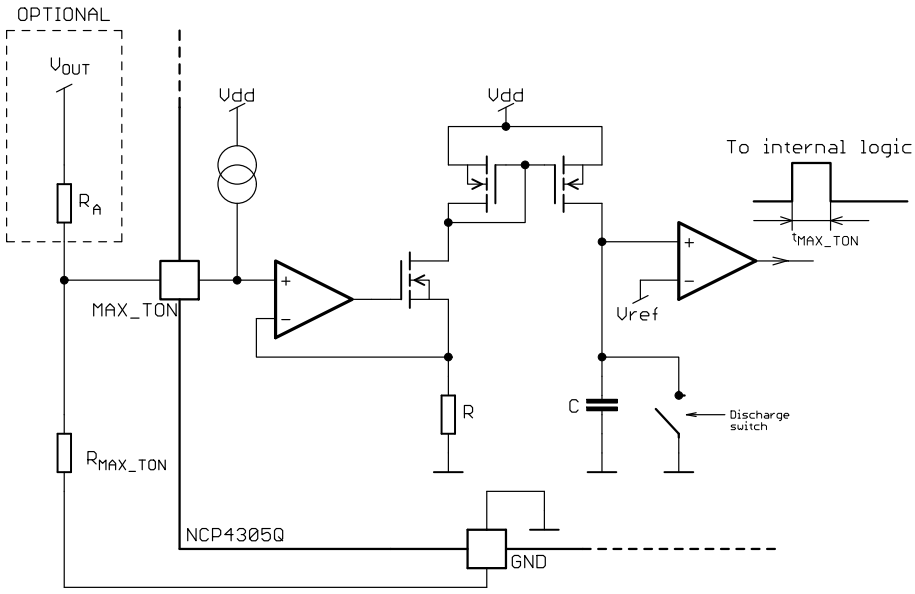


Figure 72. Internal Connection of the MAX_TON Generator, NCP4305Q

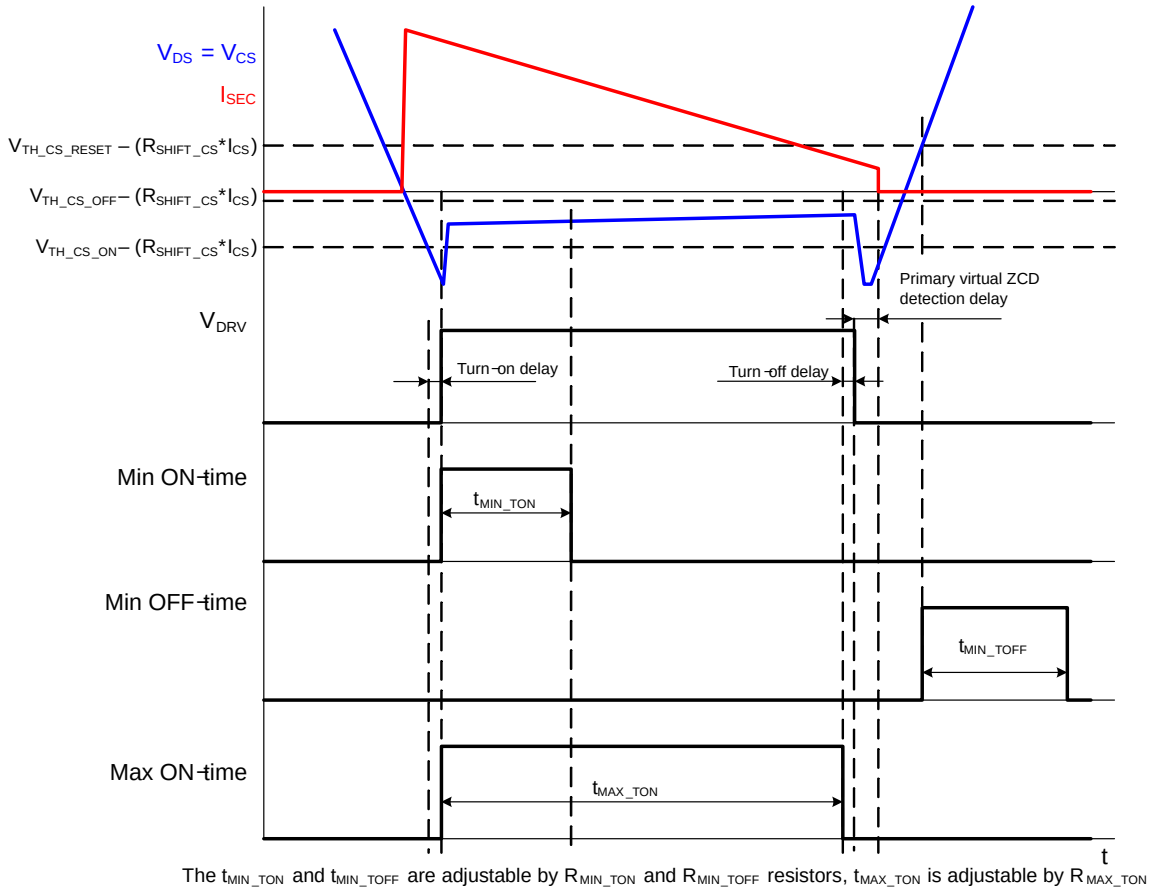


Figure 73. Function of MAX_TON Generator in Heavy Load Condition

Adaptive Gate Driver Clamp and automatic Light Load Turn−off

As synchronous rectification system significantly improves efficiency in most of SMPS applications during medium or full load conditions. However, as the load reduces into light or no−load conditions the SR MOSFET driving losses and SR controller consumption become more critical. The NCP4305 offers two key features that help to optimize application efficiency under light load and no load conditions:

1st − The driver clamp voltage is modulated and follows the output load condition. When the output load decreases the driver clamp voltage decreases as well. Under heavy load conditions the SR MOSFET's gate needs to be driven very hard to optimize the performance and reduce conduction losses. During light load conditions it is not as critical to drive the SR MOSFET's channel into such a low R_{DSON} state. This adaptive gate clamp technique helps to optimize efficiency during light load conditions especially in LLC applications where the SR MOSFETs with high input capacitance are used.

Driver voltage modulation improves the system behavior when SR controller state is changed in and out of normal or disable modes. Soft transient between drop at body diode and drop at MOSFET's $R_{DS(on)}$ only improves stability during load transients.

2nd − In extremely low load conditions or no load conditions the NCP4305 fully disables driver output and reduces the internal power consumption when output load drops below the level where skip−mode takes place.

Both features are controlled by voltage at LLD pin. The LLD pin voltage characteristic is shown in Figure 74. Driver voltage clamp is a linear function of the voltage difference between the VCC and LLD pins from V_{LLD_REC} point up to V_{LLD_MAX}. A disable mode is available, where the IC current consumption is dramatically reduced, when the difference of $V_{CC} - V_{LLD}$ voltage drops below V_{LLD_DIS}. When the voltage difference between the $V_{CC} - V_{LLD}$ pins increase above V_{LLC_REC} the disable mode ends and the IC regains normal operation. It should be noted that there are also some time delays to enter and exit from the disable mode. Time waveforms are shown at Figure 75. There is a time, t_{LLD_DISH}, that the logic ignores changes from disable mode to normal or reversely. There is also some time $t_{LLD\_DIS\_R}$ that is needed after an exit from the disable mode to assure proper internal block biasing before SR controller starts work normally.

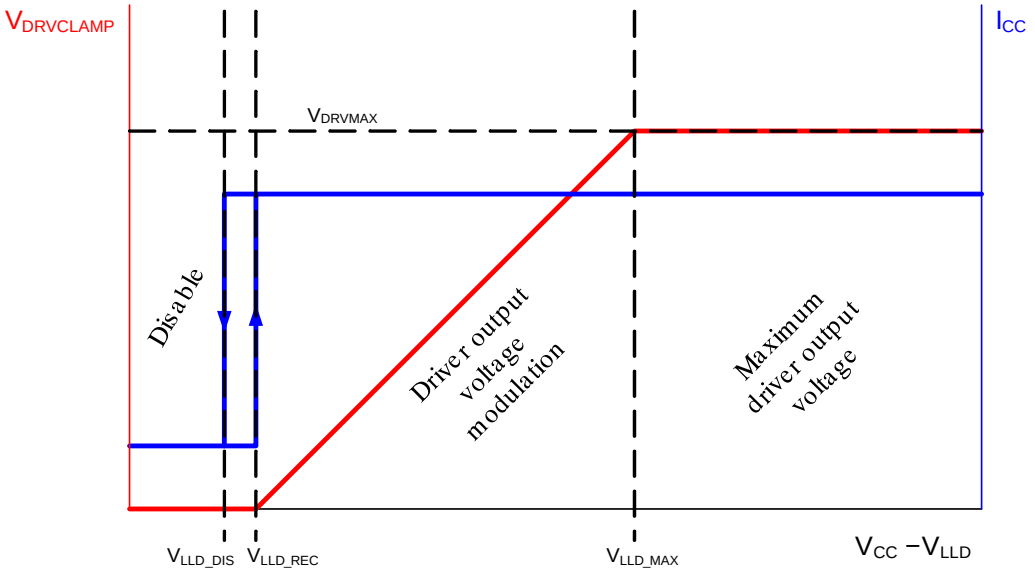


Figure 74. LLD Voltage to Driver Clamp and Current Consumption Characteristic (DRV Unloaded)

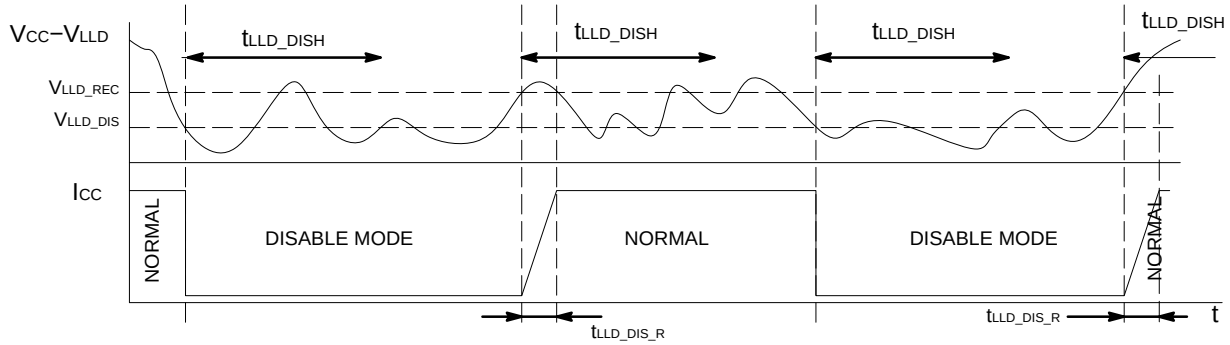


Figure 75. LLD Pin Disable Behavior in Time Domain

The two main SMPS applications that are using synchronous rectification systems today are flyback and LLC topologies. Different light load detection techniques are used in NCP4305 controller to reflect differences in operation of both mentioned applications.

Detail of the light load detection implementation technique used in NCP4305 in flyback topologies is displayed at Figure 76. Using a simple and cost effective peak detector implemented with a diode D1, resistors R1 through R3 and capacitors C2 and C3, the load level can be sensed. Output voltage of this detector on the LLD pin is referenced to controller VCC with an internal differential amplifier in NCP4305. The output of the differential amplifier is then used in two places. First the output is used in the driver block for gate drive clamp voltage adjustment. Next, the output signal is evaluated by a no−load detection comparator that activates IC disable mode in case the load is disconnected from the application output.

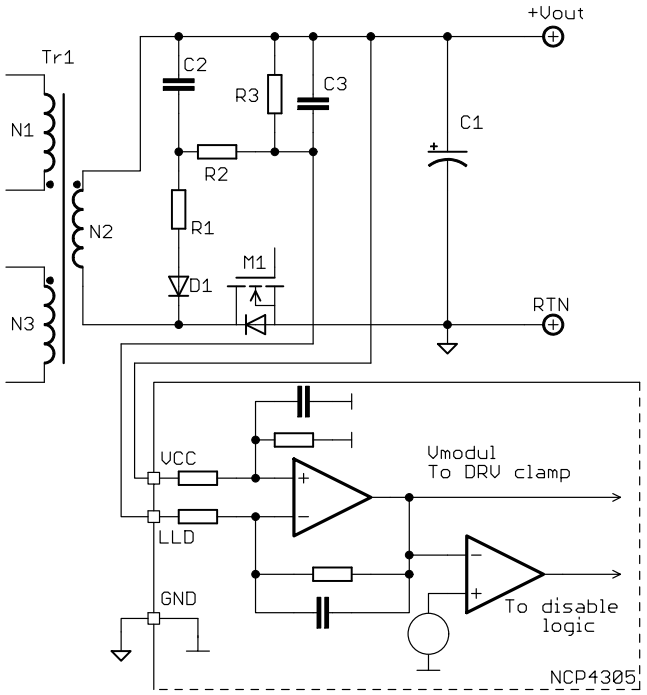


Figure 76. NCP4305 Light Load and No Load Detection Principle in Flyback Topologies

Operational waveforms related to the flyback LLD circuitry are provided in Figure 77. The SR MOSFET drain voltage drops to ~ 0 V when I_{SEC} current is flowing. When the SR MOSFET is conducting the capacitor C2 charges−up, causing the difference between the LLD pin and VCC pin to increase, and drop the LLD pin voltage. As the load decreases the secondary side currents flows for a shorter a shorter time. C2 has less time to accumulate charge and the voltage on the C2 decreases, because it is discharged by R2 and R3. This smaller voltage on C2 will cause the LLD pin voltage to increase towards V_{CC} and the difference between LLD and V_{CC} will go to zero. The output voltage then directly reduces DRV clamp voltage down from its maximum level. The DRV is then fully disabled when IC enters disable mode. The IC exits from disable mode when difference between LLD voltage and V_{CC} increases over V_{LLD_REC}. Resistors R2 and R3 are also used for voltage level adjustment and with capacitor C3 form low pass filter that filters relatively high speed ripple at C2. This low pass filter also reduces speed of state change of the SR controller from normal to disable mode or reversely. Time constant should be higher than feedback loop time constant to keep whole system stable.

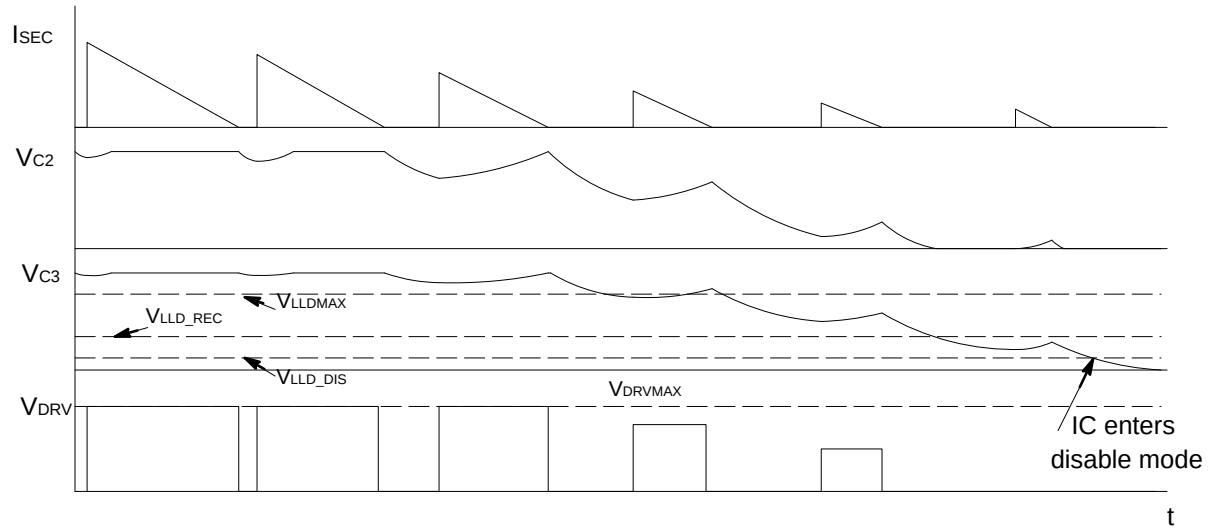


Figure 77. NCP4305 Driver Clamp Modulation Waveforms in Flyback Application Entering into Light/No Load Condition

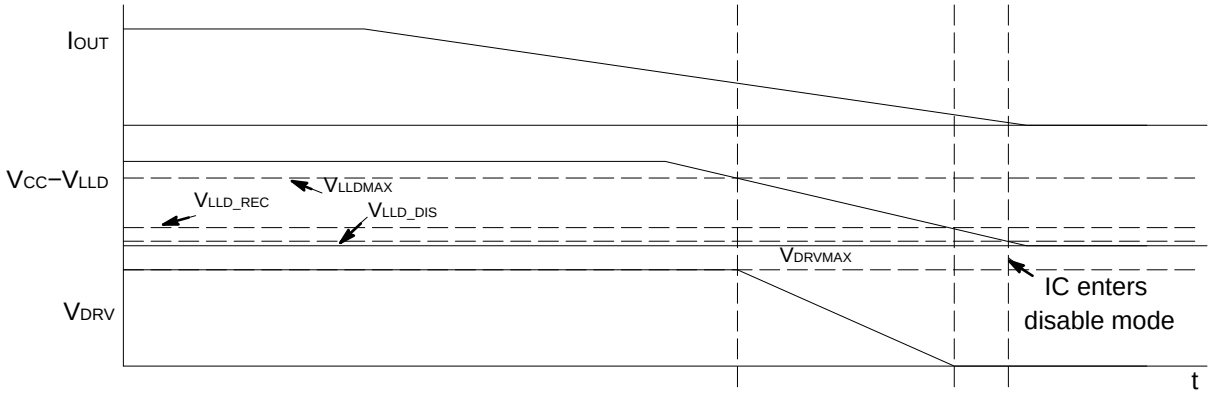


Figure 78. NCP4305 Driver Clamp Modulation Circuitry Transfer Characteristic in Flyback Application

The technique used for LLD detection in LLC is similar to the LLD detection method used in a flyback with the exception the D1 and D2 OR−ing diodes are used to measure the total duty cycle to see if it is operating in skip mode.

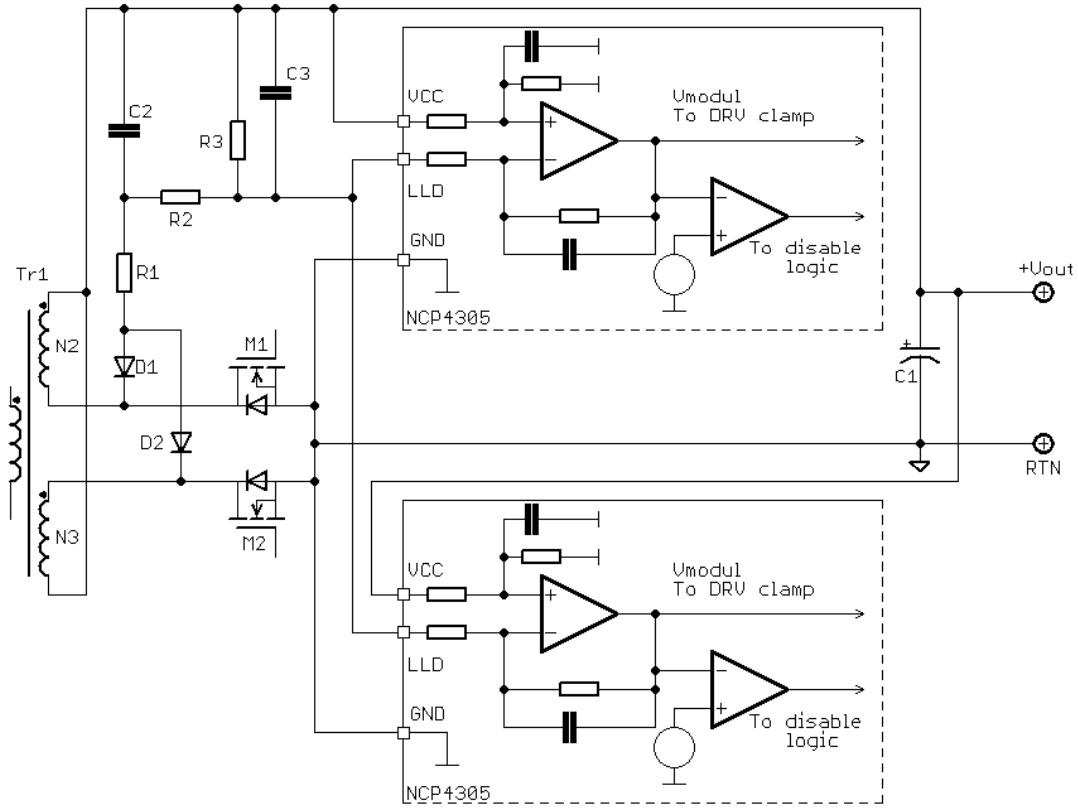


Figure 79. NCP4305 Light Load Detection in LLC Topology

The driver clamp modulation waveforms of NCP4305 in LLC are provided in Figure 80. The driver clamp voltage clips to its maximum level when LLC operates in normal mode. When the LLC starts to operate in skip mode the driver clamp voltage begins to decrease. The specific output current level is determined by skip duty cycle and detection circuit consists of R1, R2, R3, C2, C3 and diodes D1, D2. The NCP4305 enters disable mode in low load condition, when $V_{CC}-V_{LLD}$ drops below V_{LLD_DIS} (0.9 V). Disable mode ends when this voltage increase above V_{LLD_REC} (1.0 V) Figure 81 shows how LLD voltage modulates the driver output voltage clamp.

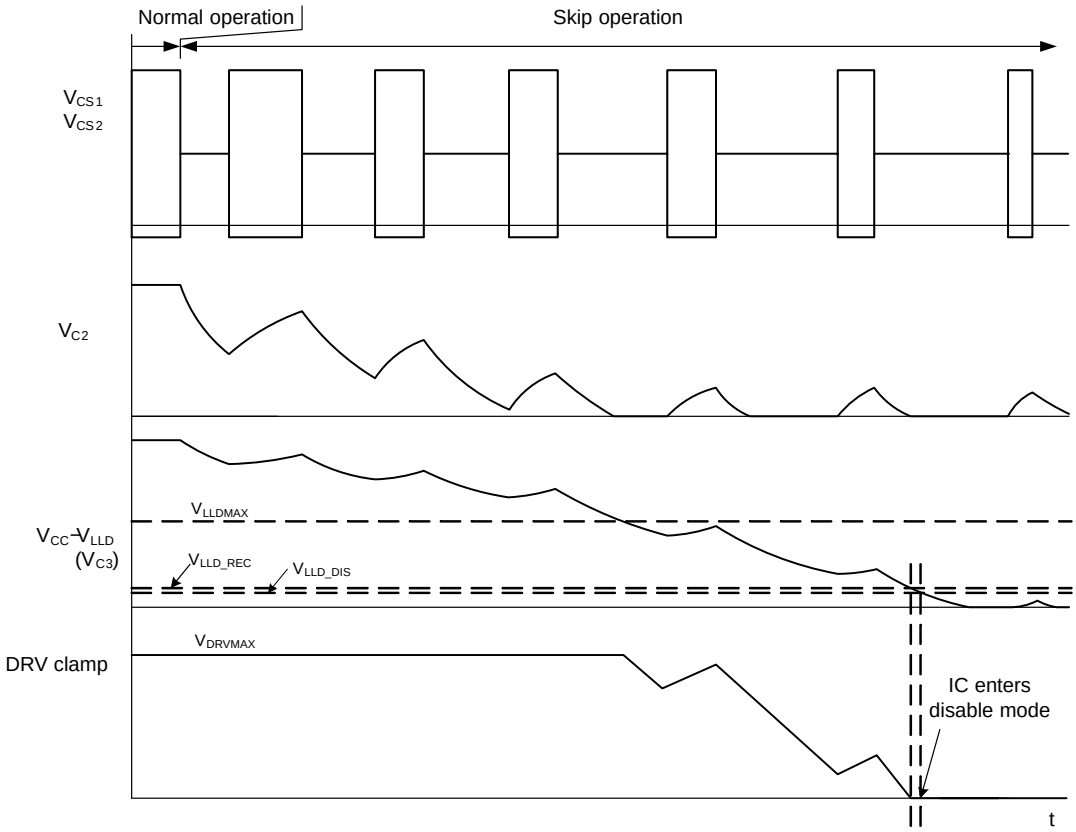


Figure 80. NCP4305 Driver Clamp Modulation Waveforms in LLC Application

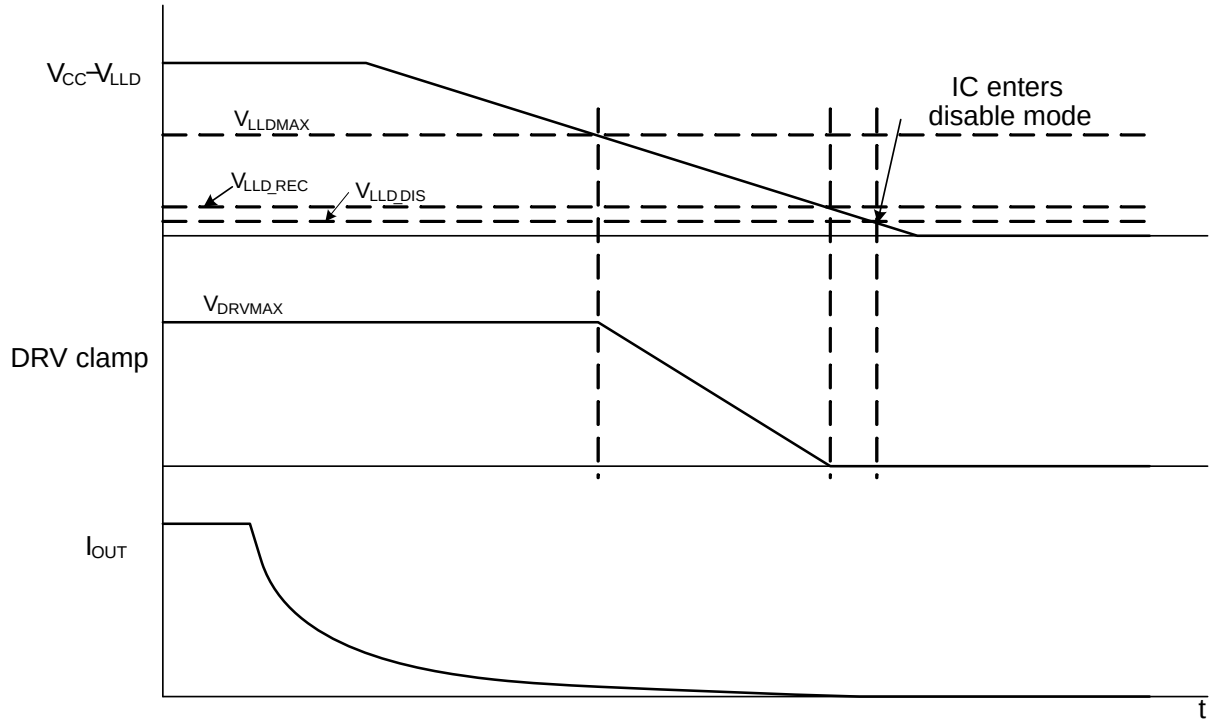


Figure 81. NCP4305 Driver Clamp Modulation Circuitry Characteristic in LLC Application

There exist some LLC applications where behavior described above is not the best choice. These applications transfer significant portion of energy in a few first pulses in skip burst. It is good to keep SR fully working during skip mode to improve efficiency. There can be still saved some energy using LLD function by activation disable mode between skip bursts. Simplified schematic for this LLD behavior is shown in Figure 46. Operation waveforms for this option are provided in Figure 83. Capacitor C2 is charged to maximum voltage when LLC is switching. When there is no switching in skip, capacitor C2 is discharged by R2 and when LLD voltage referenced to VCC falls below V_{LLD_DIS} IC enters disable mode. Disable mode is ended when LLC starts switching.

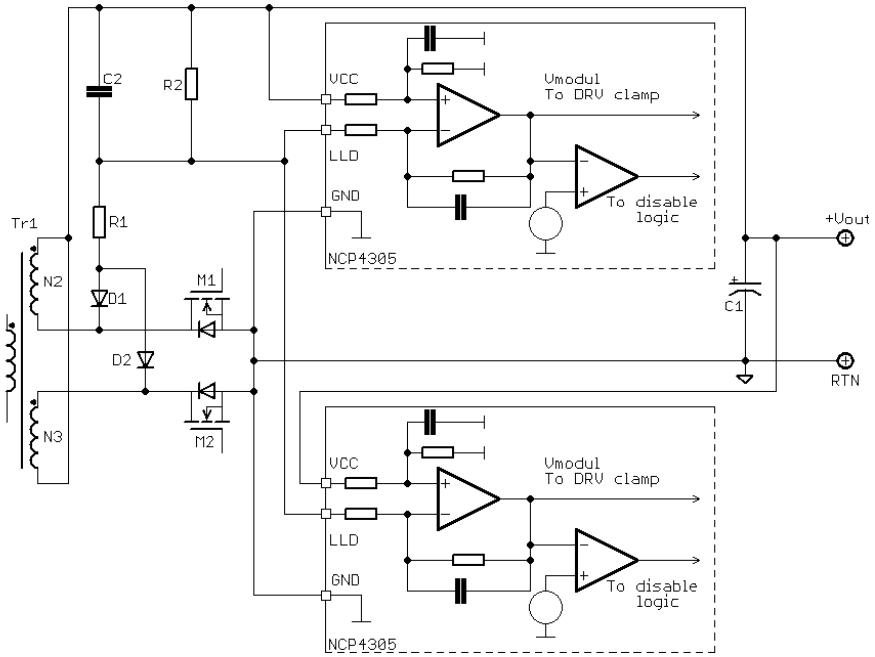


Figure 82. NCP4305 Light Load Detection in LLC Application − Other Option

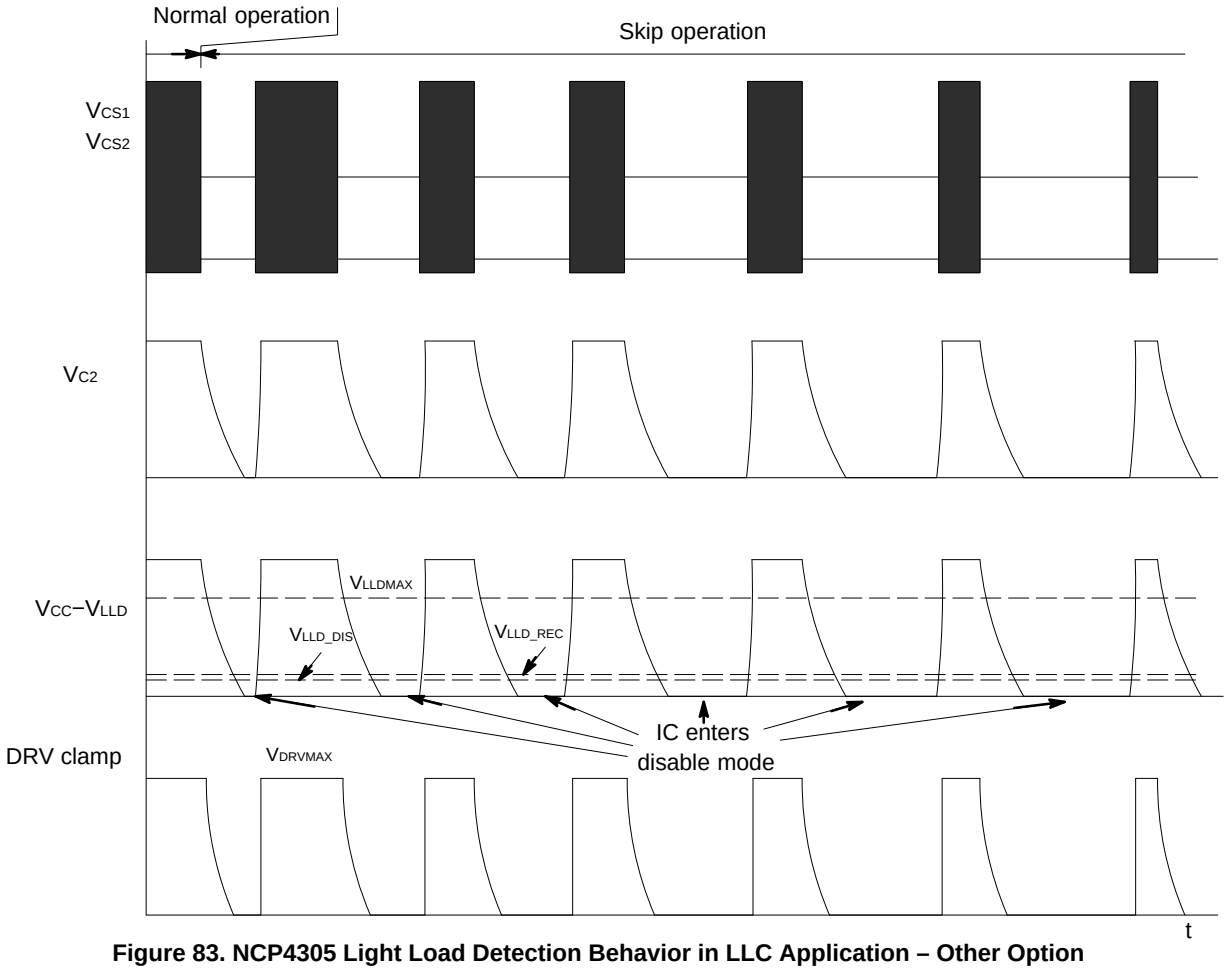


Figure 83. NCP4305 Light Load Detection Behavior in LLC Application – Other Option

Power Dissipation Calculation

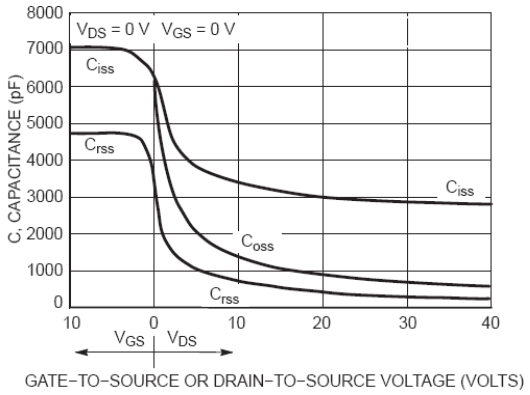
It is important to consider the power dissipation in the MOSFET driver of a SR system. If no external gate resistor is used and the internal gate resistance of the MOSFET is very low, nearly all energy losses related to gate charge are dissipated in the driver. Thus it is necessary to check the SR driver power losses in the target application to avoid over temperature and to optimize efficiency.

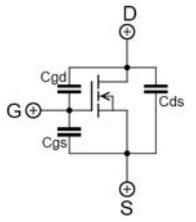
In SR systems the body diode of the SR MOSFET starts conducting before SR MOSFET is turned−on, because there is some delay from $V_{TH\_CS\_ON}$ detect to turn−on the driver. On the other hand, the SR MOSFET turn off process always starts before the drain to source voltage rises up significantly. Therefore, the MOSFET switch always operates under Zero Voltage Switching (ZVS) conditions when in a synchronous rectification system.

The following steps show how to approximately calculate the power dissipation and DIE temperature of the NCP4305 controller. Note that real results can vary due to the effects of the PCB layout on the thermal resistance.

Step 1 − MOSFET Gate−to Source Capacitance:

During ZVS operation the gate to drain capacitance does not have a Miller effect like in hard switching systems because the drain to source voltage does not change (or its change is negligible).





$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{rss} = C_{gd}$$

$$C_{oss} = C_{ds} + C_{gd}$$

Figure 84. Typical MOSFET Capacitances Dependency on V_{DS} and V_{GS} Voltages

Therefore, the input capacitance of a MOSFET operating in ZVS mode is given by the parallel combination of the gate to source and gate to drain capacitances (i.e. C_{iss} capacitance for given gate to source voltage). The total gate charge, Q_{g_total}, of most MOSFETs on the market is defined for hard switching conditions. In order to accurately calculate the driving losses in a SR system, it is necessary to determine the gate charge of the MOSFET for operation specifically in a ZVS system. Some manufacturers define this parameter as Q_{g_ZVS}. Unfortunately, most datasheets do not provide this data. If the C_{iss} (or Q_{g_ZVS}) parameter is not available then it will need to be measured. Please note that the input capacitance is not linear (as shown Figure 84) and it needs to be characterized for a given gate voltage clamp level.

Step 2 − Gate Drive Losses Calculation:

Gate drive losses are affected by the gate driver clamp voltage. Gate driver clamp voltage selection depends on the type of MOSFET used (threshold voltage versus channel resistance). The total power losses (driving loses and conduction losses) should be considered when selecting the gate driver clamp voltage. Most of today's MOSFETs for SR systems feature low $R_{DS(on)}$ for 5 V V_{GS} voltage. The NCP4305 offers both a 5 V gate clamp and a 10 V gate clamp for those MOSFET that require higher gate to source voltage.

The total driving loss can be calculated using the selected gate driver clamp voltage and the input capacitance of the MOSFET:

$$P_{DRV\_total} = V_{CC} \cdot V_{CLAMP} \cdot C_{g\_ZVS} \cdot f_{SW} \quad \text{(eq. 9)}$$

Where:

V_{CC}	is the NCP4305 supply voltage
V_{CLAMP}	is the driver clamp voltage
C_{g_ZVS}	is the gate to source capacitance of the MOSFET in ZVS mode
f_{sw}	is the switching frequency of the target application

The total driving power loss won't only be dissipated in the IC, but also in external resistances like the external gate resistor (if used) and the MOSFET internal gate resistance (Figure 50). Because NCP4305 features a clamped driver, it's high side portion can be modeled as a regular driver switch with equivalent resistance and a series voltage source. The low side driver switch resistance does not drop immediately at turn−off, thus it is necessary to use an equivalent value ($R_{DRV\_SIN\_EQ}$) for calculations. This method simplifies power losses calculations and still provides acceptable accuracy. Internal driver power dissipation can then be calculated using Equation 10:

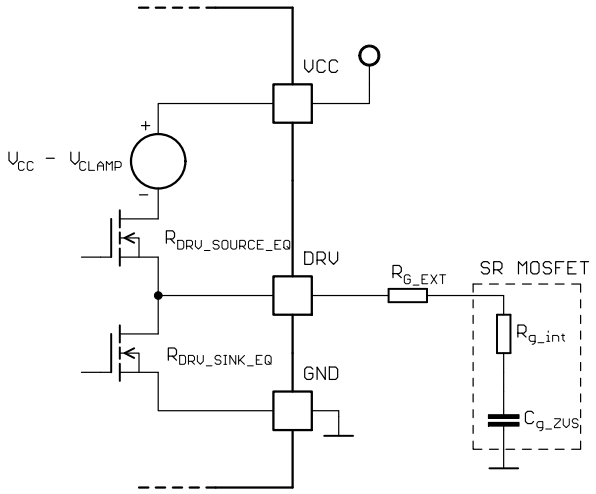


Figure 85. Equivalent Schematic of Gate Drive Circuitry

$$P_{DRV\_IC} = \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{CLAMP}^{\ 2} \cdot f_{SW} \cdot \left(\frac{R_{DRV\_SINK\_EQ}}{R_{DRV\_SINK\_EQ} + R_{G\_EXT} + R_{g\_int}} \right) + C_{g\_ZVS} \cdot V_{CLAMP} \cdot f_{SW} \cdot \left(V_{CC} - V_{CLAMP} \right)$$

(eq. 10)

$$+ \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{CLAMP}^{\ 2} \cdot f_{SW} \cdot \left(\frac{R_{DRV\_SOURCE\_EQ}}{R_{DRV\_SOURCE\_EQ} + R_{G\_EXT} + R_{g\_int}} \right)$$

Where:

$R_{DRV\_SINK\_EQ}$	is the NCP4305x driver low side switch equivalent resistance (0.5 Ω)
$R_{DRV\_SOURCE\_EQ}$	is the NCP4305x driver high side switch equivalent resistance (1.2 Ω)
R_{G_EXT}	is the external gate resistor (if used)
R_{g_int}	is the internal gate resistance of the MOSFET

Step 3 − IC Consumption Calculation:

In this step, power dissipation related to the internal IC consumption is calculated. This power loss is given by the I_{CC} current and the IC supply voltage. The I_{CC} current depends on switching frequency and also on the selected min t_{ON} and t_{OFF} periods because there is current flowing out from the min t_{ON} and t_{OFF} pins. The most accurate method for calculating these losses is to measure the I_{CC} current when C_{DRV} = 0 nF and the IC is switching at the target frequency with given MIN_TON and MIN_TOFF adjust resistors. IC consumption losses can be calculated as:

$$P_{CC} = V_{CC} \cdot I_{CC} \quad \text{(eq. 11)}$$

Step 4 − IC Die Temperature Arise Calculation:

The die temperature can be calculated now that the total internal power losses have been determined (driver losses plus internal IC consumption losses). The package thermal resistance is specified in the maximum ratings table for a 35 μm thin copper layer with no extra copper plates on any pin (i.e. just 0.5 mm trace to each pin with standard soldering points are used).

The DIE temperature is calculated as:

$$T_{DIE} = \left(P_{DRV\_IC} + P_{CC} \right) \cdot R_{\theta J-A} + T_A \quad \text{(eq. 12)}$$

Where:

P_{DRV_IC}	is the IC driver internal power dissipation
P_{CC}	is the IC control internal power dissipation
$R_{\theta JA}$	is the thermal resistance from junction to ambient
T_A	is the ambient temperature

PRODUCT OPTIONS

OPN	Package	UVLO [V]	DRV clamp [V]	Pin 5 function	Usage
NCP4305ADR2G	SOIC8	4.5	4.7	TRIG	LLC, CCM flyback, DCM flyback, forward, QR, QR with primary side CCM control
NCP4305AMTTWG	WDFN8	4.5	4.7	TRIG	
NCP4305DDR2G	SOIC8	4.5	9.5	TRIG	
NCP4305DMNTWG	DFN8	4.5	9.5	TRIG	
NCP4305DMTTWG	WDFN8	4.5	9.5	TRIG	
NCP4305QDR2G	SOIC8	4.5	9.5	MAX_TON	QR with forced CCM from secondary side

ORDERING INFORMATION

Device	Package	Package marking	Packing	Shipping†
NCP4305ADR2G	SOIC8	NCP4305A	SOIC−8 (Pb−Free)	2500 /Tape & Reel
NCP4305DDR2G		NCP4305D		
NCP4305QDR2G		NCP4305Q		
NCP4305AMTTWG	WDFN8	5A	WDFN−8 (Pb−Free)	3000 /Tape & Reel
NCP4305DMTTWG		5D		
NCP4305DMNTWG	DFN8	4305D	DFN−8 (Pb−Free)	4000 /Tape & Reel

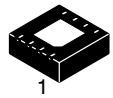
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

DFN8, 4x4
CASE 488AF−01
ISSUE C

DATE 15 JAN 2009



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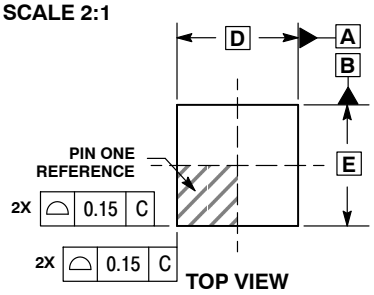
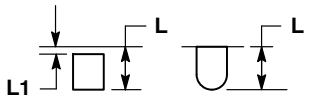
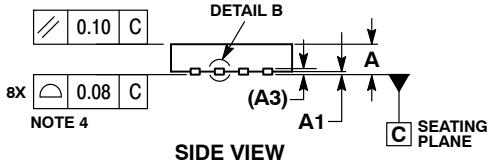
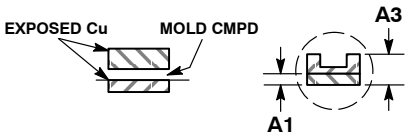


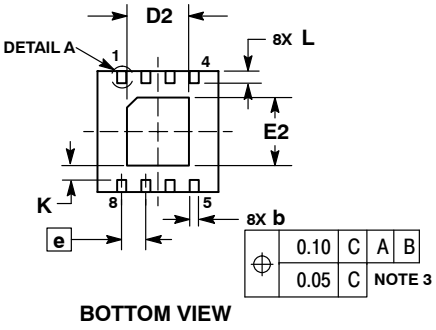




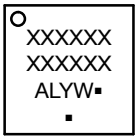


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



GENERIC MARKING DIAGRAM*

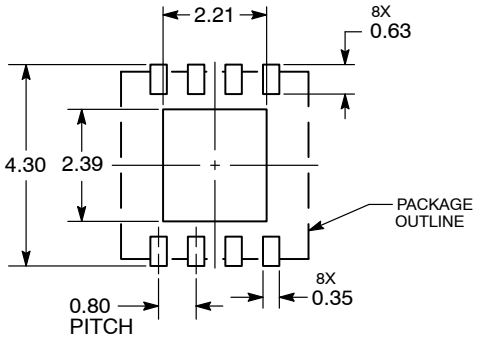


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON15232D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DFN8, 4X4, 0.8P	PAGE 1 OF 1

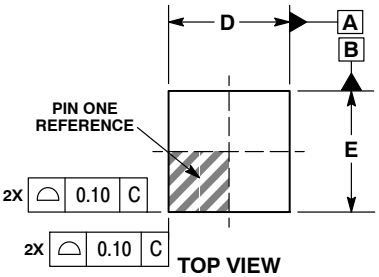
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

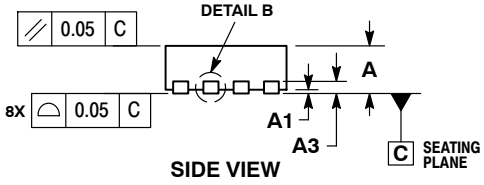
SCALE 4:1

WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O

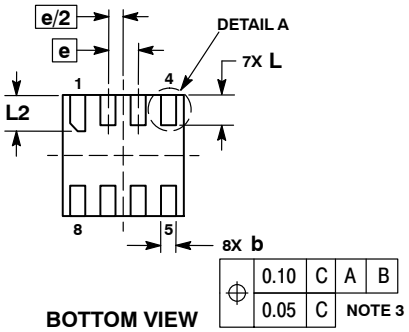
DATE 26 FEB 2010



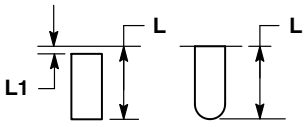
TOP VIEW



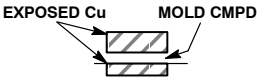
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

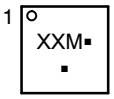


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

GENERIC MARKING DIAGRAM*

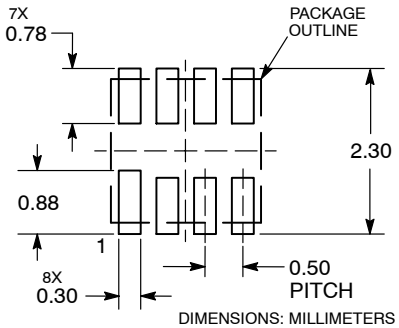


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON48654E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8, 2X2, 0.5 P**	**PAGE 1 OF 1**

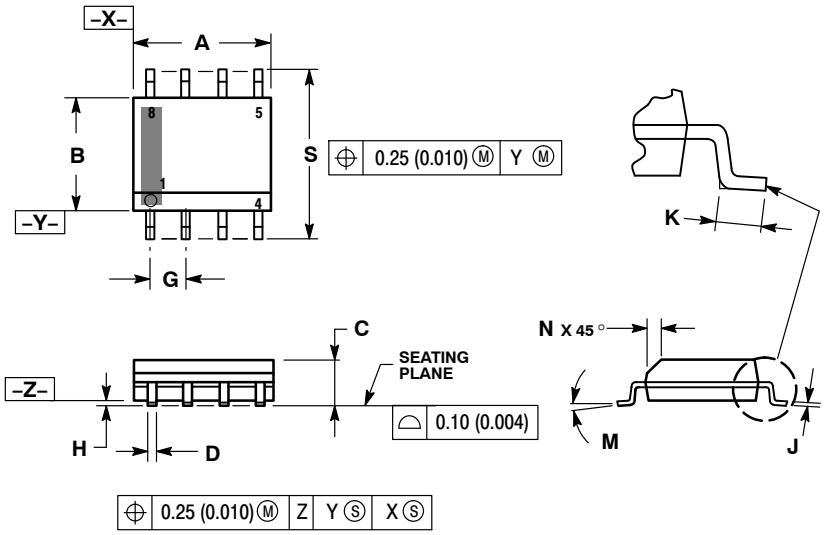
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

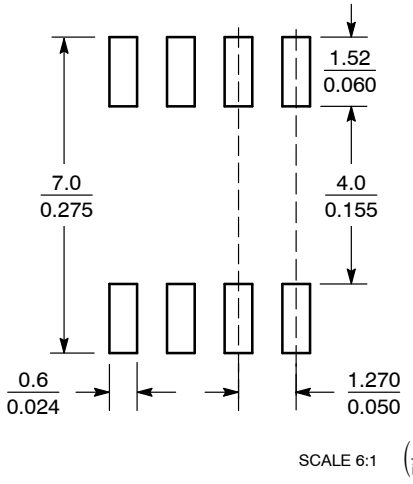
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

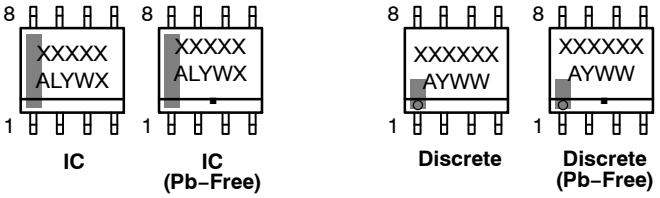
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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