NCP4620

150 mA, 10 V, Low Dropout Regulator

The NCP4620 is a CMOS Linear voltage regulator with 150 mA output current capability. The device is capable of operating with input voltages up to 10 V, with high output voltage accuracy and low temperature−drift coefficient. The NCP4620 is easy to use, with output current fold−back protection and a thermal shutdown circuit included. A Chip Enable function is included to save power by lowering supply current.

Features

- Operating Input Voltage Range: 2.6 V to 10 V
- Output Voltage Range: 1.2 V to 6.0 V (available in 0.1 V steps)
- Output Voltage Accuracy: ±1.0%
- Low Supply Current: 23 μA
- Low Dropout: 165 mV (I_{OUT} = 100 mA, V_{OUT} = 3.3 V)
  400 mV (I_{OUT} = 150 mA, V_{OUT} = 2.8 V)
- High PSRR: 70 dB at 1 kHz
- Line Regulation 0.02%/V Typ
- Current Fold Back Protection
- Thermal Shutdown Protection
- Stable with Ceramic Capacitors
- Available in SC−70 and SOT23 Packages
- These are Pb−Free Devices*

Typical Applications

- Battery products powered by 2 Lithium Ion cells
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Toys, industrial applications

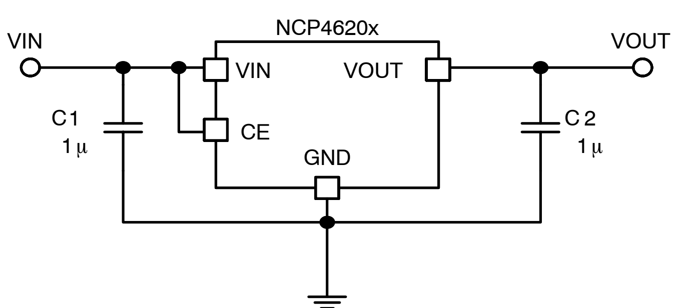

Figure 1. Typical Application Schematic

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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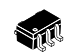
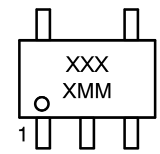
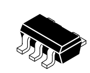
http://onsemi.com

MARKING DIAGRAMS

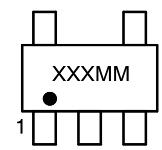


SC−70
CASE 419A





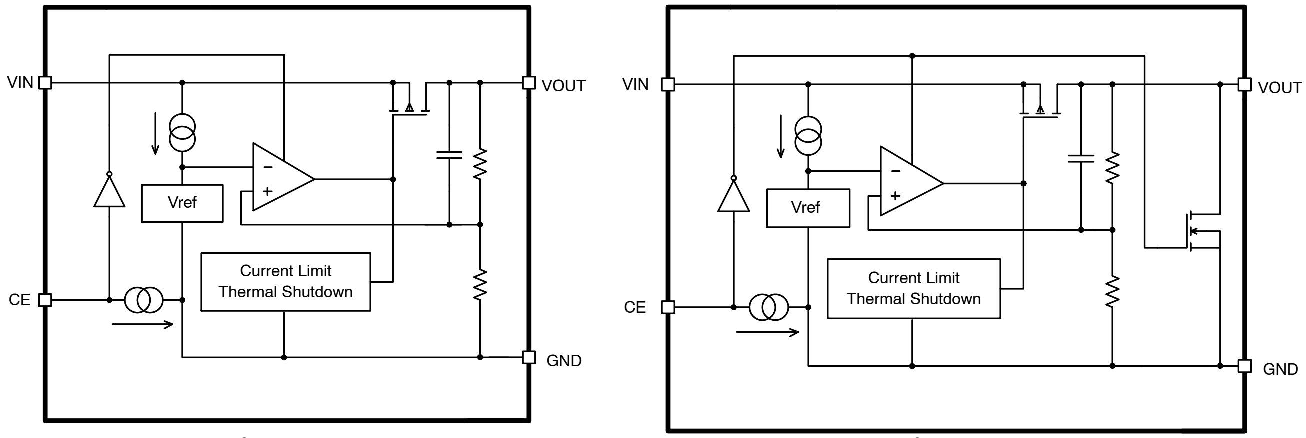
SOT−23−5
CASE 1212



XXXX, XXX= Specific Device Code
MM = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.



NCP4620Hxxxx NCP4620Dxxxx

Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SC−70	Pin No. SOT23	Pin Name	Description
5	1	VIN	Input pin
3	2	GND	Ground
1	3	CE	Chip enable pin (Active “H”)
4	5	VOUT	Output pin
2	4	NC	No connection

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	12.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	12.0	V
Output Current	I_{OUT}	165	mA
Power Dissipation − SC−70	P_D	380	mW
Power Dissipation − SOT23		420	
Operating Temperature	T_A	−40 to +85	°C
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	−55 to +125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 0.47$ μF, unless otherwise noted. Typical values are at $T_A = +25°C$.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.6		10	V
Output Voltage	$T_A = +25°C$	$V_{OUT} > 1.5$ V $V_{OUT} \le 1.5$ V	V_{OUT}	x0.99 −15		x1.01 15	V mV
	$-40°C \le T_A \le 85°C$	$V_{OUT} > 1.5$ V $V_{OUT} \le 1.5$ V		x0.974 −40		x1.023 35	V mV
Output Voltage Temp. Coefficient	$-40°C \le T_A \le 85°C$				±80		ppm/°C
Line Regulation	$V_{OUT(NOM)} + 0.5$ V or 2.6 V (whichever is higher) $\le V_{IN} \le 10$ V		$Line_{Reg}$		0.02	0.2	%/V
Load Regulation	$I_{OUT} = 0.1$ mA to 150 mA		$Load_{Reg}$		5	40	mV
Dropout Voltage	$I_{OUT} = 150$ mA	$1.2\text{ V} \le V_{OUT} < 1.3$ V $1.3\text{ V} \le V_{OUT} < 1.5$ V $1.5\text{ V} \le V_{OUT} < 1.8$ V $1.8\text{ V} \le V_{OUT} < 2.3$ V $2.3\text{ V} \le V_{OUT} < 3.0$ V $3.0\text{ V} \le V_{OUT} < 4.0$ V $4.0\text{ V} \le V_{OUT} < 6.0$ V	V_{DO}		 0.40 0.30 0.25	1.40 1.30 1.10 0.80 0.58 0.48 0.40	V
Output Current			I_{OUT}	150			mA
Short Current Limit	$V_{OUT} = 0$ V		I_{SC}		40		mA
Quiescent Current			I_Q		23	40	μA
Standby Current	$V_{IN} = 10$ V, $V_{CE} = 0$ V, $T_A = 25°C$		I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	1.7			V
	CE Input Voltage “L”		V_{CEL}			0.8	
CE Pull Down Current			I_{CEPD}		0.3		μA
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1$ V or 3.0 V whichever is higher, $\Delta V_{IN} = 0.2$ V_{pk-pk}, $I_{OUT} = 30$ mA, f = 1 kHz		PSRR		70		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, $I_{OUT} = 30$ mA, $V_{OUT} = 1.5$ V, $V_{IN} = 2.6$ V		V_N		90		μV_{rms}
Low Output N−ch Tr. On Resistance	$V_{IN} = 7$ V, $V_{CE} = 0$ V		R_{LOW}		250		Ω
Thermal Shutdown Temperature			T_{TSD}		165		°C
Thermal Shutdown Release			T_{TSR}		110		°C

TYPICAL CHARACTERISTICS

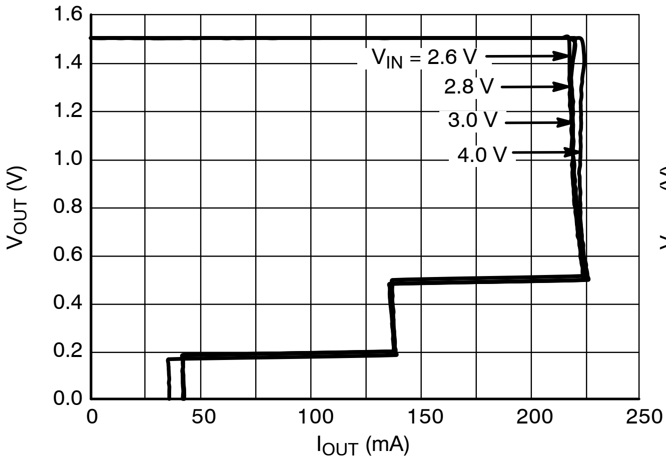


Figure 3. Output Voltage vs. Output Current 1.5 V Version (T_J = 25°C)

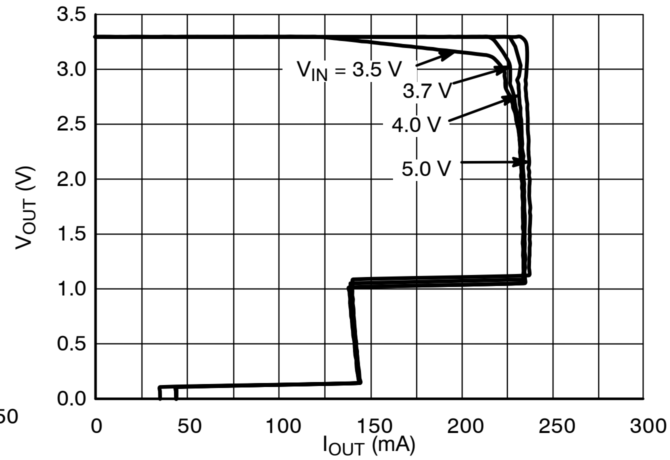


Figure 4. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

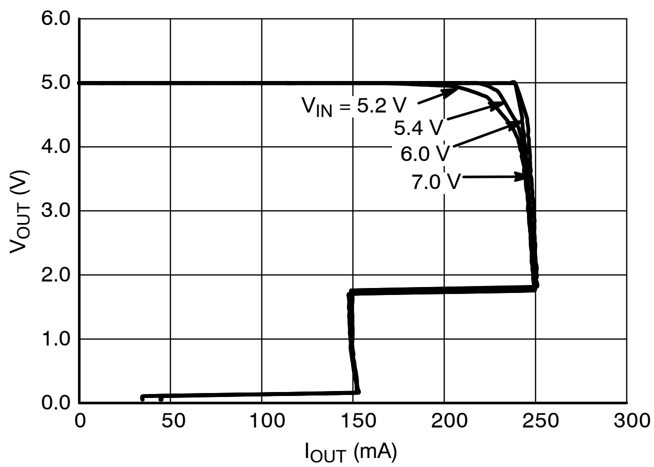


Figure 5. Output Voltage vs. Output Current 5.0 V Version (T_J = 25°C)

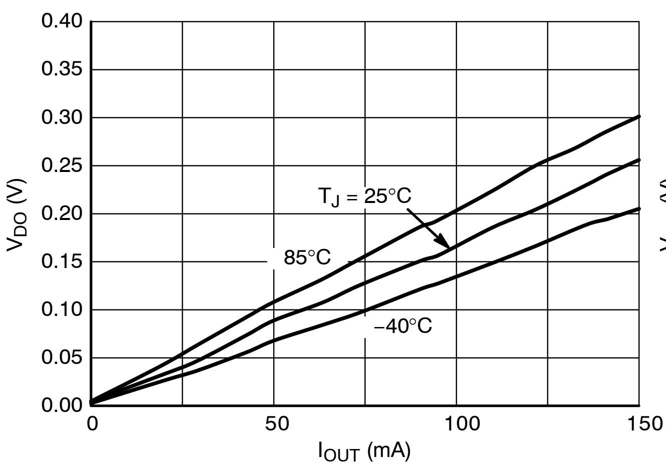


Figure 6. Dropout Voltage vs. Output Current 3.3 V Version

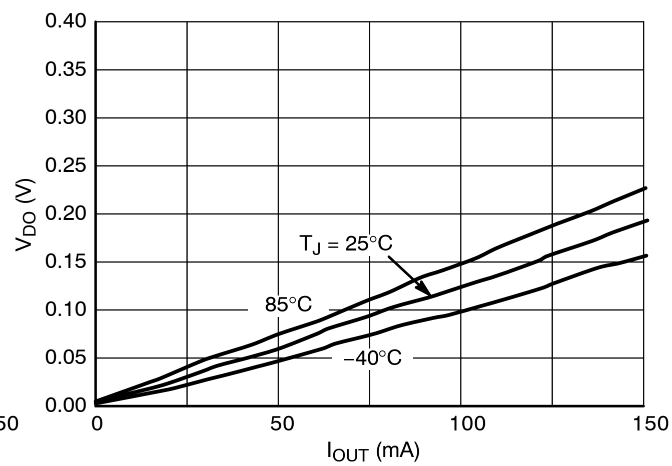


Figure 7. Dropout Voltage vs. Output Current 5.0 V Version

TYPICAL CHARACTERISTICS

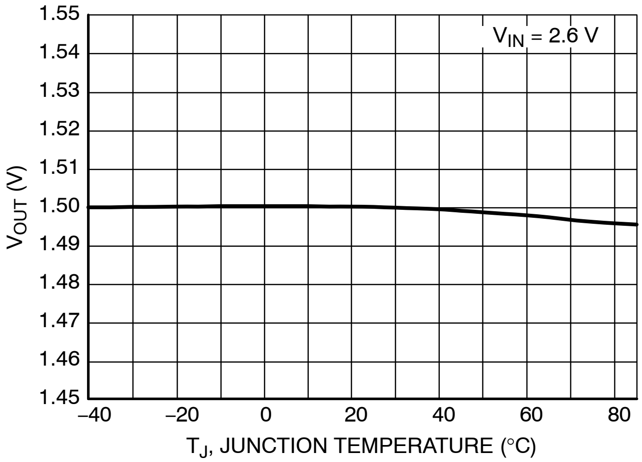


Figure 8. Output Voltage vs. Temperature, 1.5 V Version

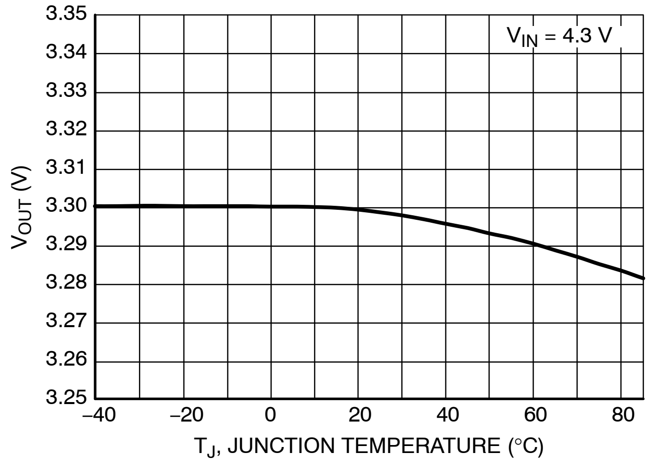


Figure 9. Output Voltage vs. Temperature, 3.3 V Version

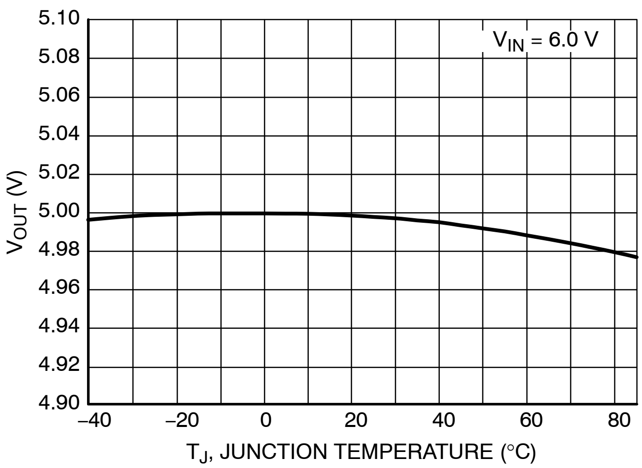


Figure 10. Output Voltage vs. Temperature, 5.0 V Version

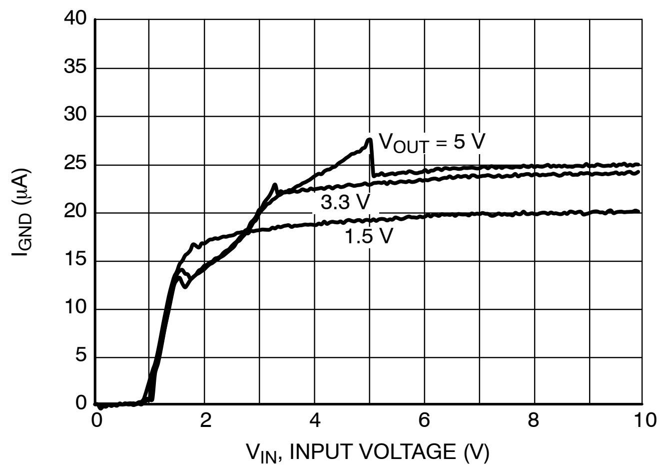


Figure 11. Supply Current vs. Input Voltage

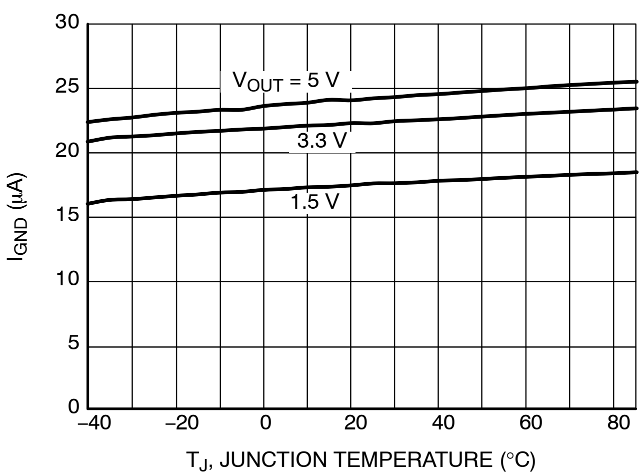


Figure 12. Supply Current vs. Temperature

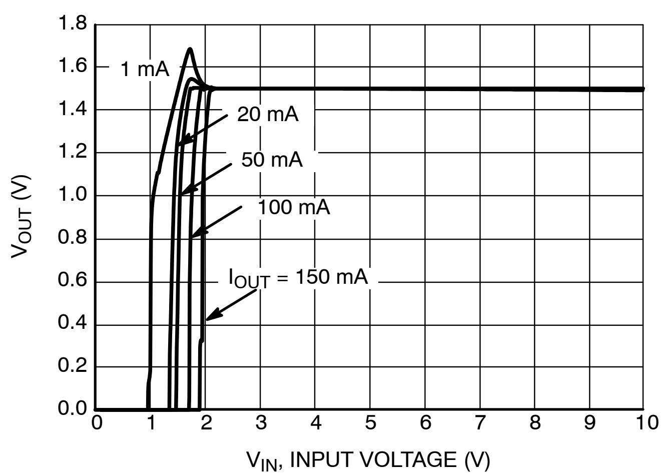


Figure 13. Output Voltage vs. Input Voltage, 1.5 V Version

TYPICAL CHARACTERISTICS

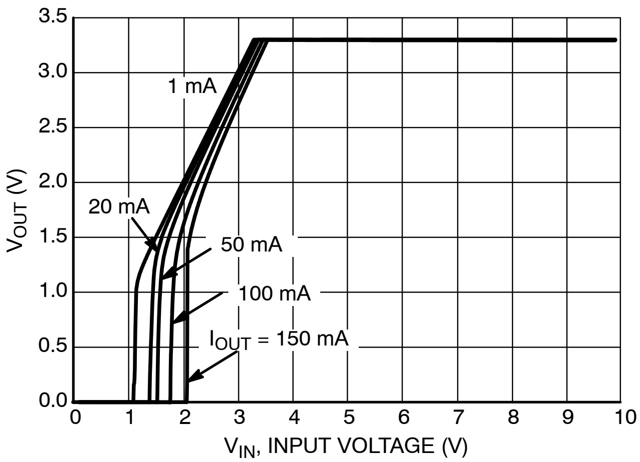


Figure 14. Output Voltage vs. Input Voltage, 3.3 V Version

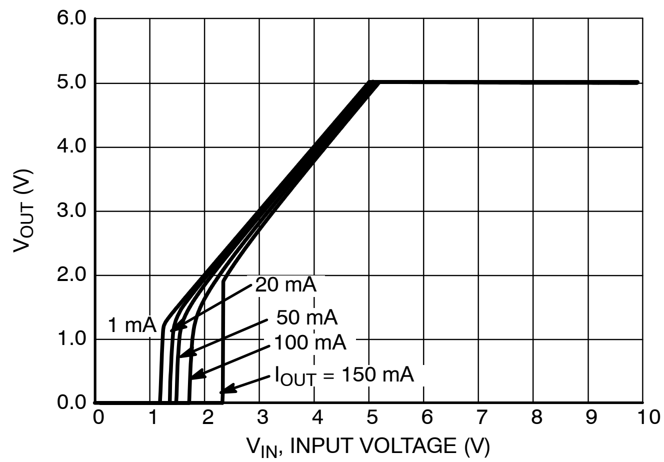


Figure 15. Output Voltage vs. Input Voltage, 5.0 V Version

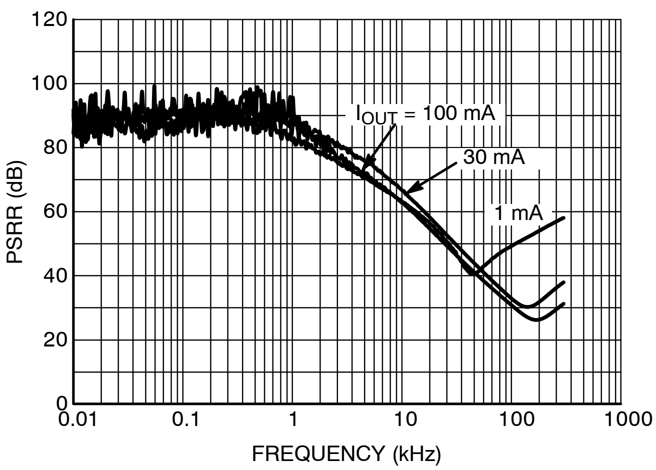


Figure 16. PSRR, 1.5 V Version, V_{IN} = 3.5 V

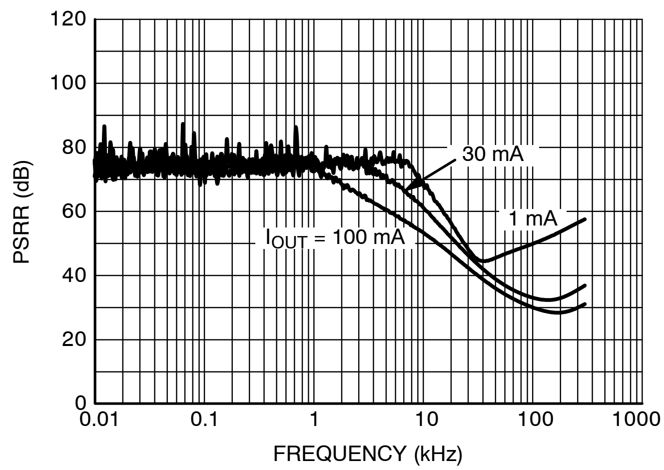


Figure 17. PSRR, 3.3 V Version, V_{IN} = 5.3 V

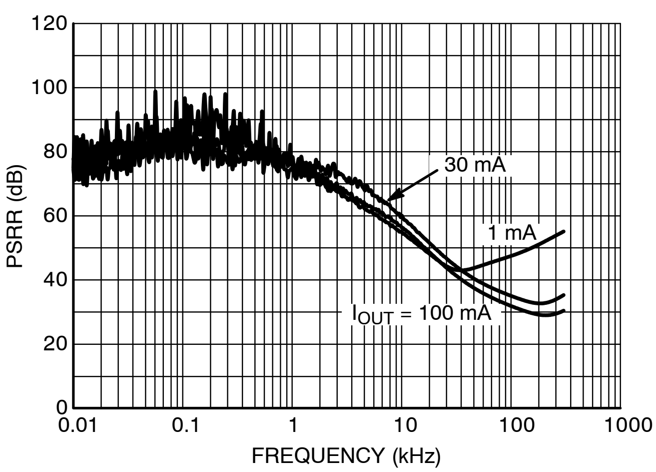


Figure 18. PSRR, 5.0 V Version, V_{IN} = 7.0 V

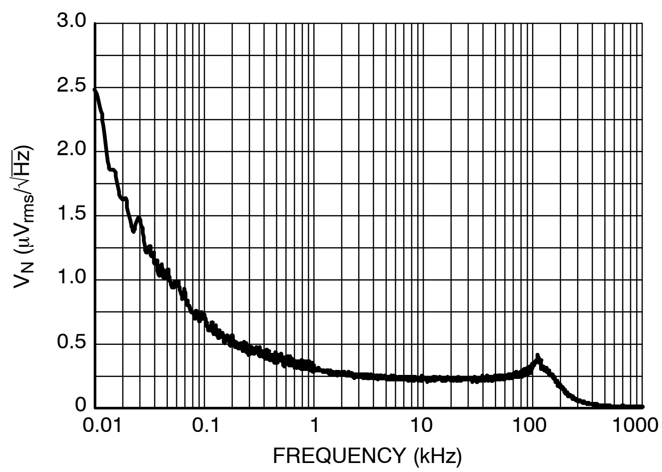


Figure 19. Output Voltage Noise, 1.5 V Version, V_{IN} = 2.6 V, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

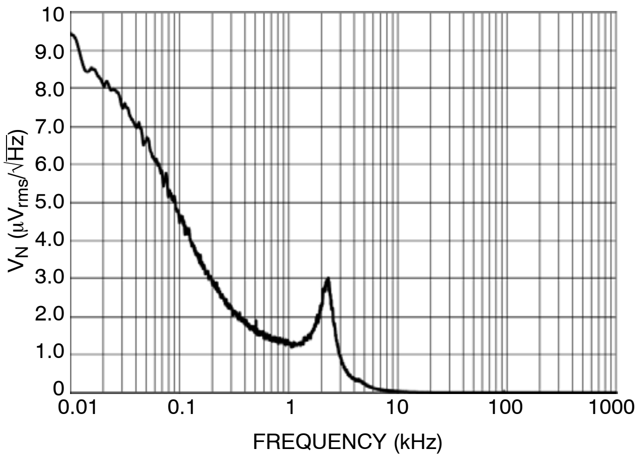


Figure 20. Output Voltage Noise, 3.3 V Version, V_{IN} = 4.3 V, I_{OUT} = 30 mA

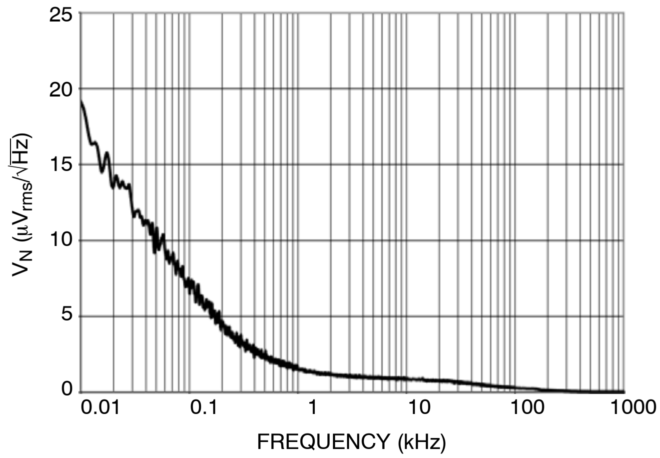


Figure 21. Output Voltage Noise, 5.0 V Version, V_{IN} = 6.0 V, I_{OUT} = 30 mA

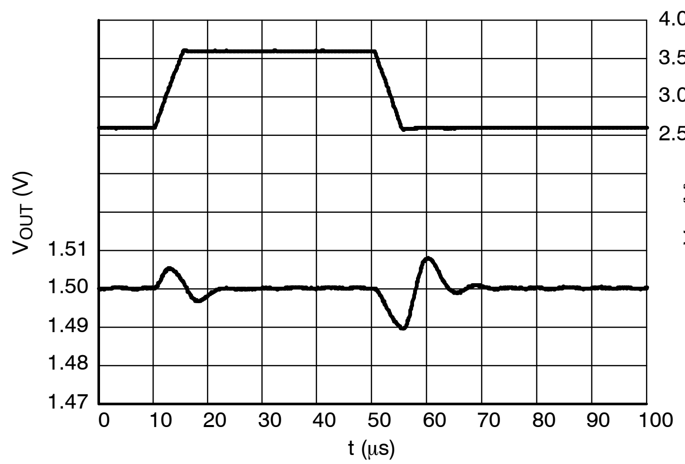


Figure 22. Line Transients, 1.5 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

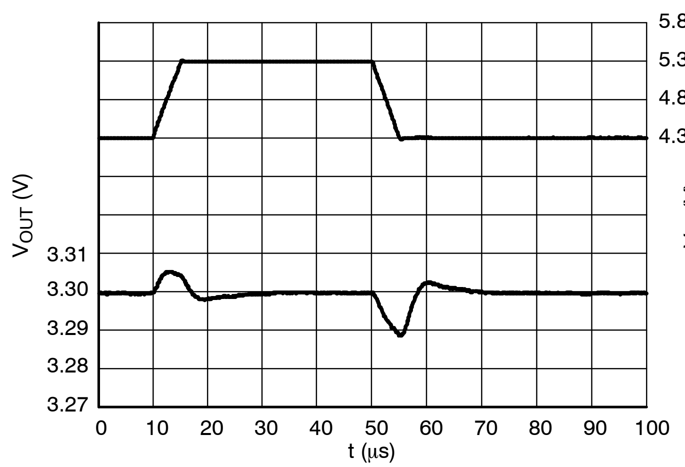


Figure 23. Line Transients, 3.3 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

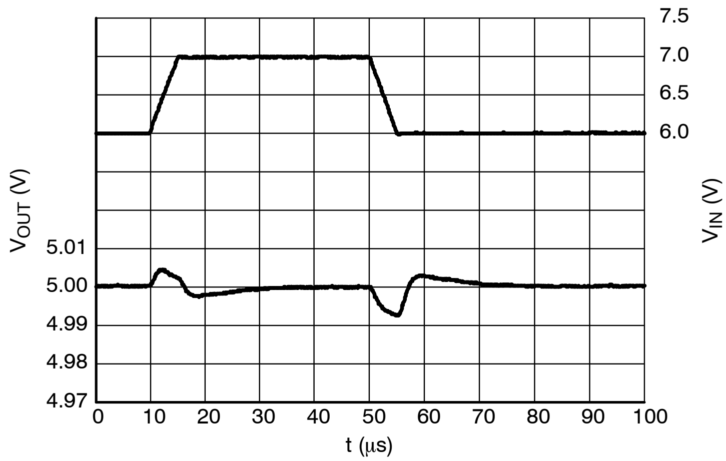


Figure 24. Line Transients, 5.0 V version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30$ mA

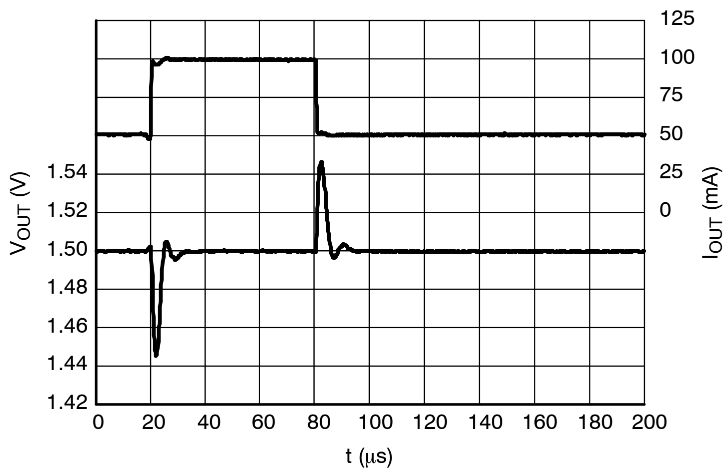


Figure 25. Load Transients, 1.5 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.6$ V

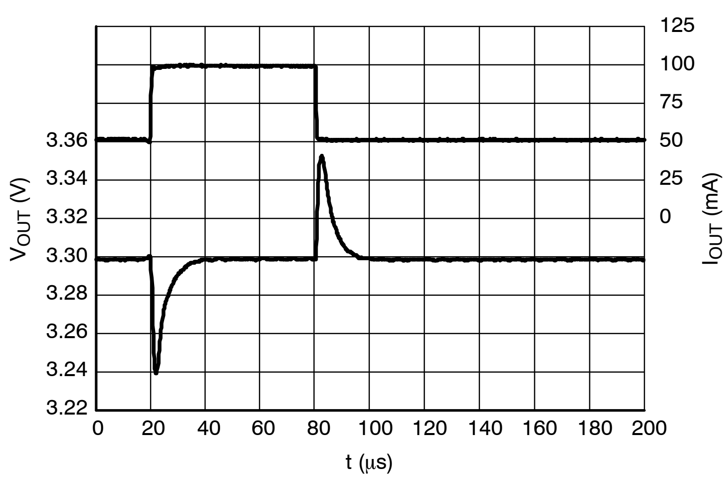


Figure 26. Load Transients, 3.3 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 4.3$ V

TYPICAL CHARACTERISTICS

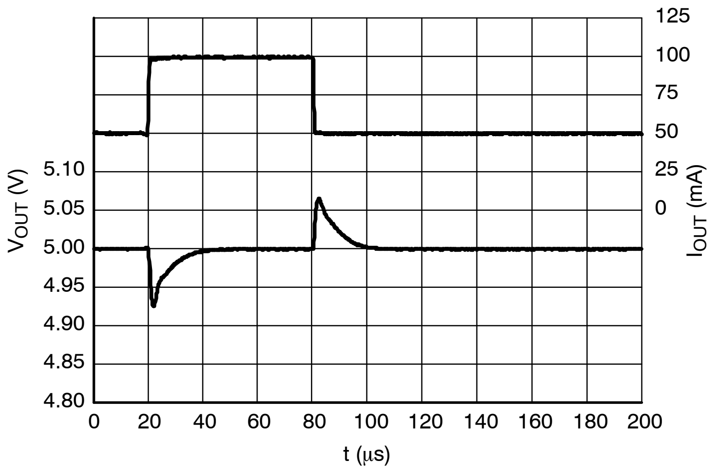


Figure 27. Load Transients, 5.0 V Version, I_{OUT} = 50 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 6.0 V

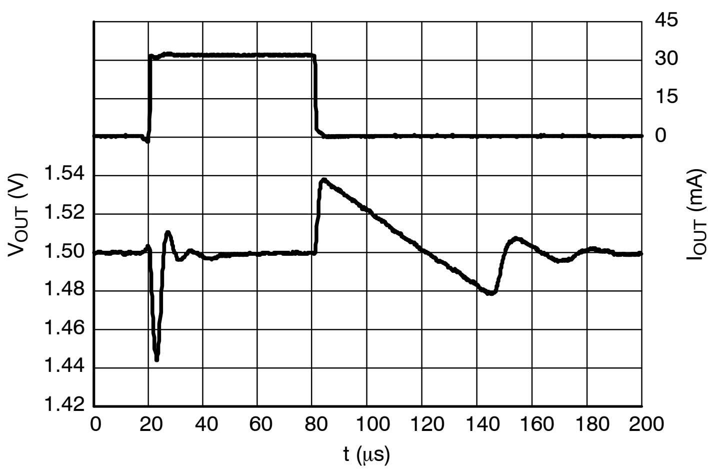


Figure 28. Load Transients, 1.5 V Version, I_{OUT} = 1 – 30 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.6 V

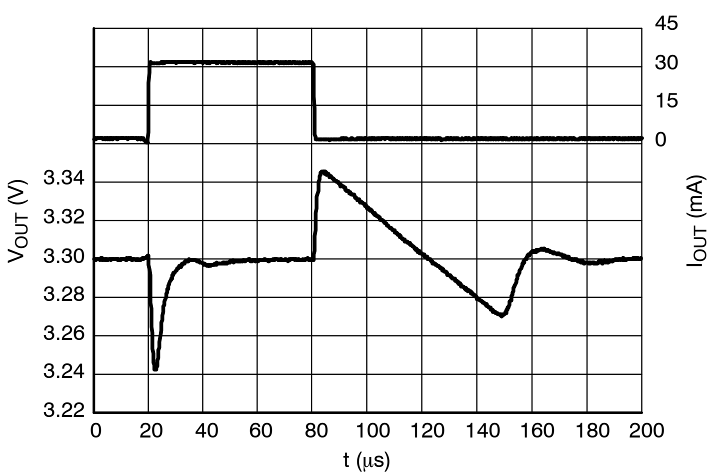


Figure 29. Load Transients, 3.3 V Version, I_{OUT} = 1 – 30 mA, t_R = t_F = 0.5 μs, V_{IN} = 4.3 V

TYPICAL CHARACTERISTICS

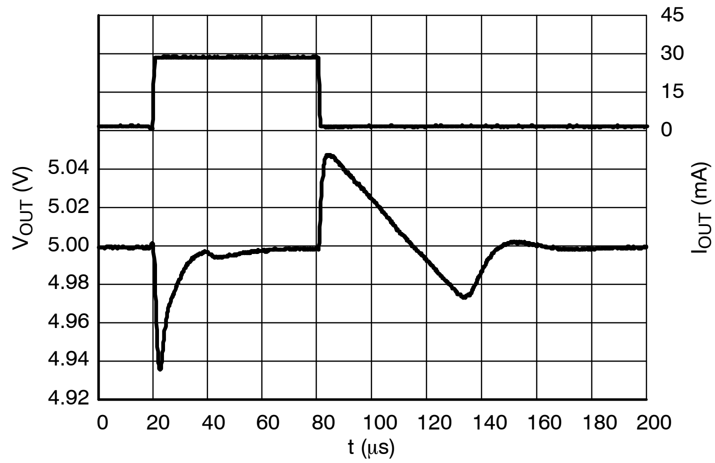


Figure 30. Load Transients, 5.0 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 6.0 V

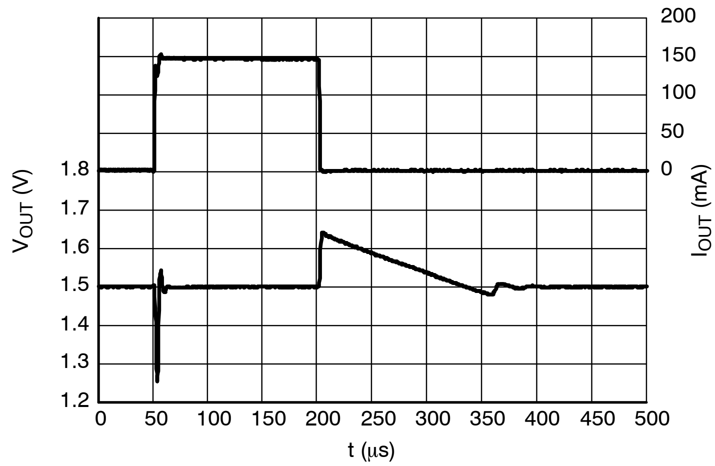


Figure 31. Load Transients, 1.5 V Version, I_{OUT} = 1 – 150 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.6 V

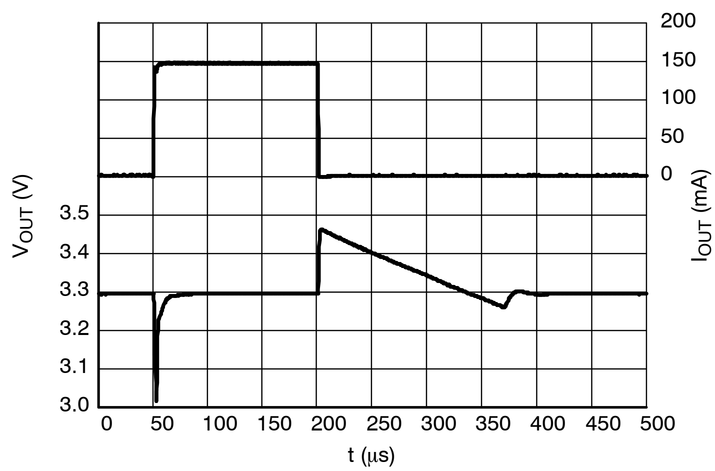


Figure 32. Load Transients, 3.3 V Version, I_{OUT} = 1 – 150 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

TYPICAL CHARACTERISTICS

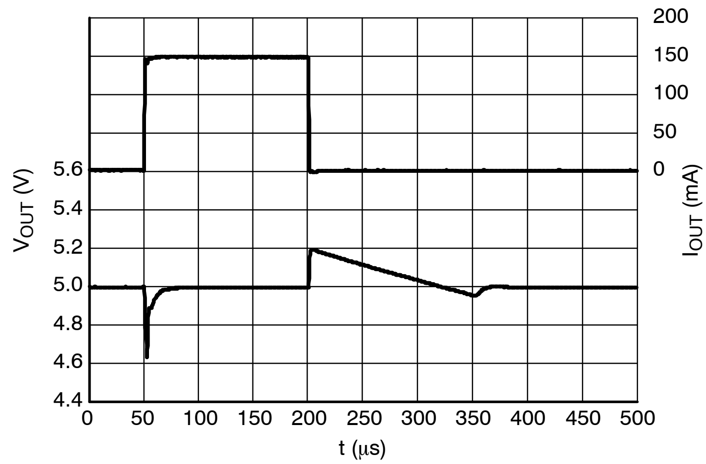


Figure 33. Load Transients, 5.0 V Version,
I_{OUT} = 1 – 150 mA, t_R = t_F = 0.5 μs, V_{IN} = 6.0 V

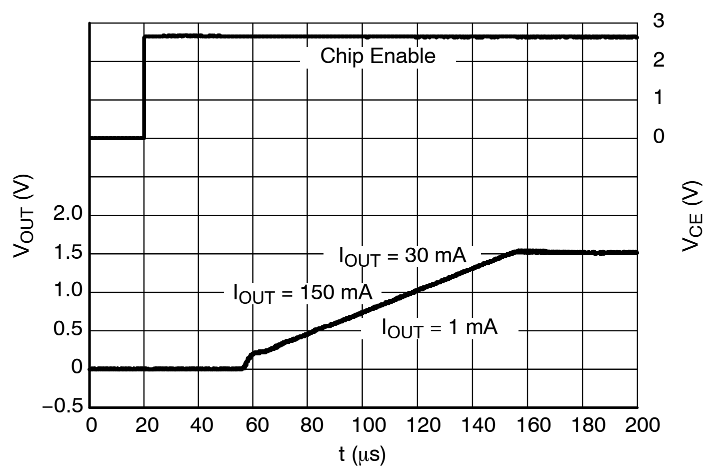


Figure 34. Start−up, 1.5 V Version, V_{IN} = 2.6 V

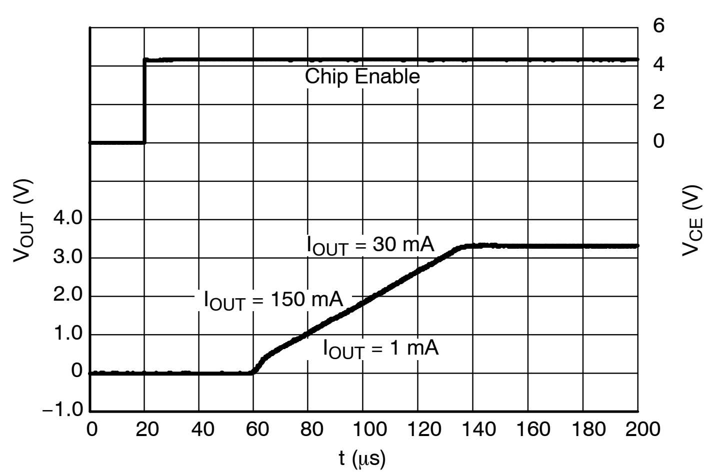


Figure 35. Start−up, 3.3 V Version, V_{IN} = 4.3 V

TYPICAL CHARACTERISTICS

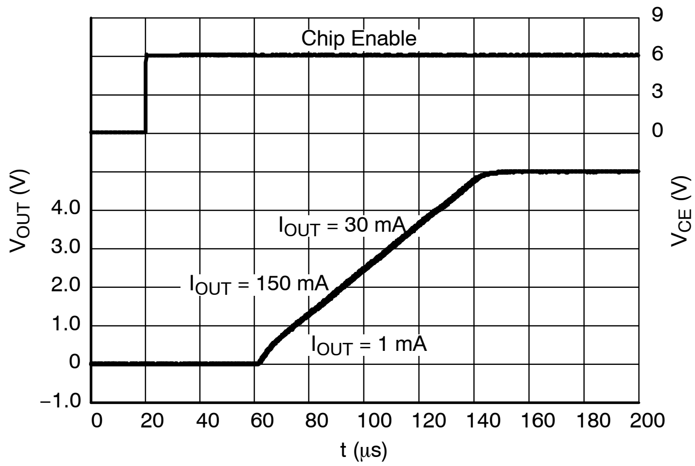


Figure 36. Start−up, 5.0 V Version, V_{IN} = 6.0 V

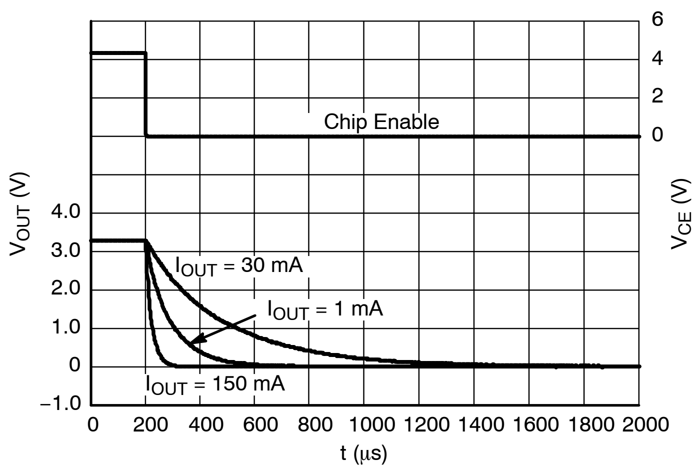


Figure 37. Shutdown, 3.3 V Version D,
V_{IN} = 4.3 V

APPLICATION INFORMATION

A typical application circuit for NCP4620 series is shown in Figure 38.

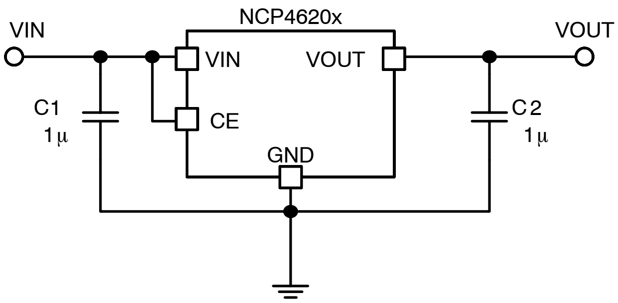


Figure 38. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4620. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Output Discharger

The D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

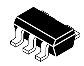
PCB layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4620DSN15T1G	1.5 V	Auto discharge	JBE	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620DSN30T1G	3.0 V	Auto discharge	JBX	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620DSN33T1G	3.3 V	Auto discharge	KBA	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620DSN50T1G	5.0 V	Auto discharge	KBT	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620HSN15T1G	1.5 V	Standard	JAE	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620HSN33T1G	3.3 V	Standard	KAA	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620HSN50T1G	5.0 V	Standard	KAT	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4620DSQ18T1G	1.8 V	Auto discharge	AD08	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4620HSQ12T1G	1.2 V	Standard	AC01	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4620HSQ15T1G	1.5 V	Standard	AC05	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4620HSQ18T1G	1.8 V	Standard	AC08	SC−70 (Pb−Free)	3000 / Tape & Reel
NCP4620HSQ25T1G	2.5 V	Standard	AC16	SC−70 (Pb−Free)	3000 / Tape & Reel

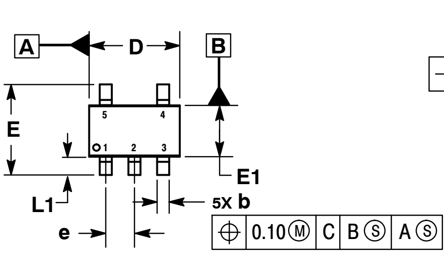
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*To order other package and voltage variants, please contact your ON Semiconductor sales representative.

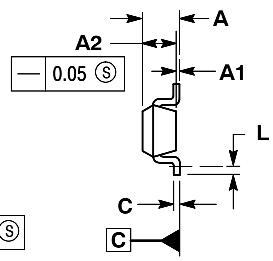


SCALE 2:1

SOT−23 5−LEAD
CASE 1212−01
ISSUE A

DATE 28 JAN 2011

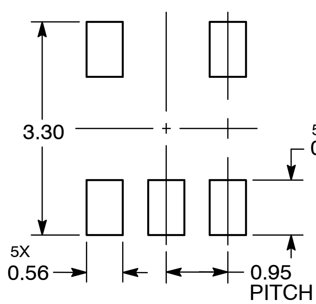




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

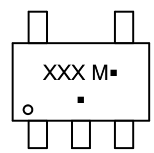
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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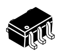
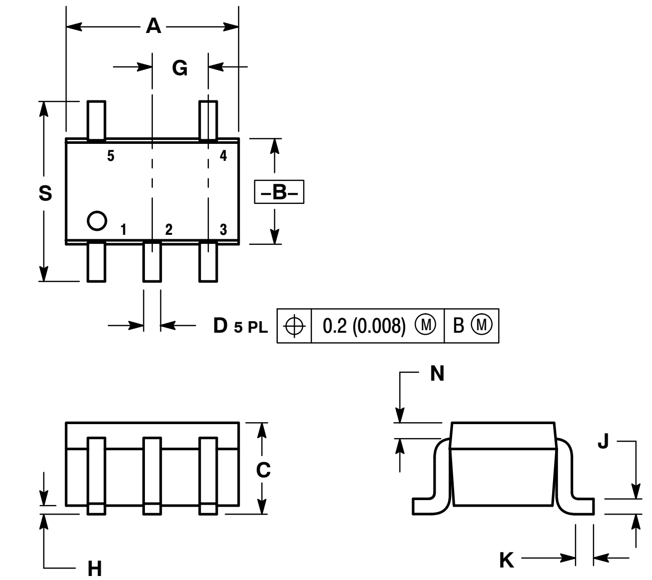
DESCRIPTION:	SOT−23 5−LEAD	PAGE 1 OF 1



SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

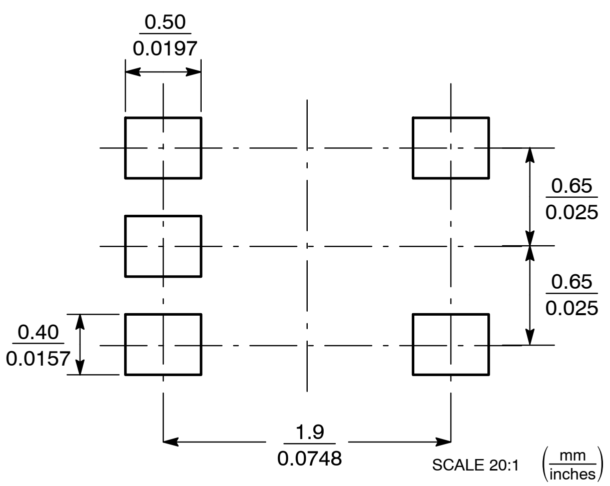
DATE 17 JAN 2013



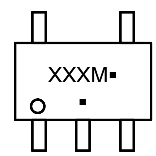
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

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