NCP5217A

Single Synchronous Step-Down Controller

The NCP5217A is a synchronous step−down controller for high performance systems battery−power systems. The NCP5217A includes a high efficiency PWM controller. A pin is provided to enable or disable forced PWM mode of operation. An internal power good voltage monitor tracks the SMPS output. NCP5217A also features soft−start sequence, UVLO for V_{CC} and switcher, overvoltage protection, overcurrent protection, undervoltage protection and thermal shutdown. The IC is packaged in QFN14.

Features

- 0.8% accuracy 0.8 V Reference
- 4.5 V to 27 V Battery/Adaptor Voltage Range
- Adjustable Output Voltage Range: 0.8 V to 3.3 V
- Selectable Power Saving Mode / Force PWM Mode
- Lossless Inductor Current Sensing
- Programmable Transient−Response−Enhancement (TRE) Control
- Programmable Adaptive Voltage Positioning (AVP)
- Input Supply Feedforward Control
- Internal Soft−Start
- Integrated Output Discharge (Soft−Stop)
- Build−in Adaptive Gate Drivers
- PGOOD Indication
- Overvoltage, Undervoltage and Overcurrent Protections
- Thermal Shutdown
- QFN14 Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Notebook Application
- System Power

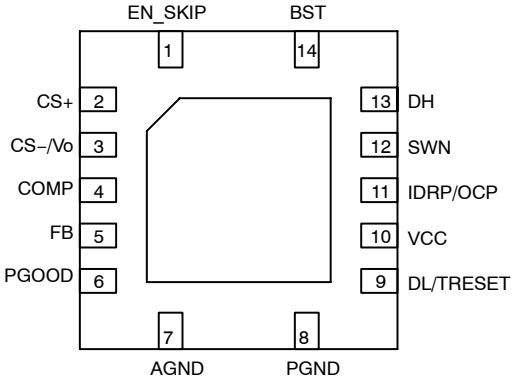
ON Semiconductor®

http://onsemi.com

QFN14
CASE 485AL

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)



QFN14
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5217AMNTXG	QFN14 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

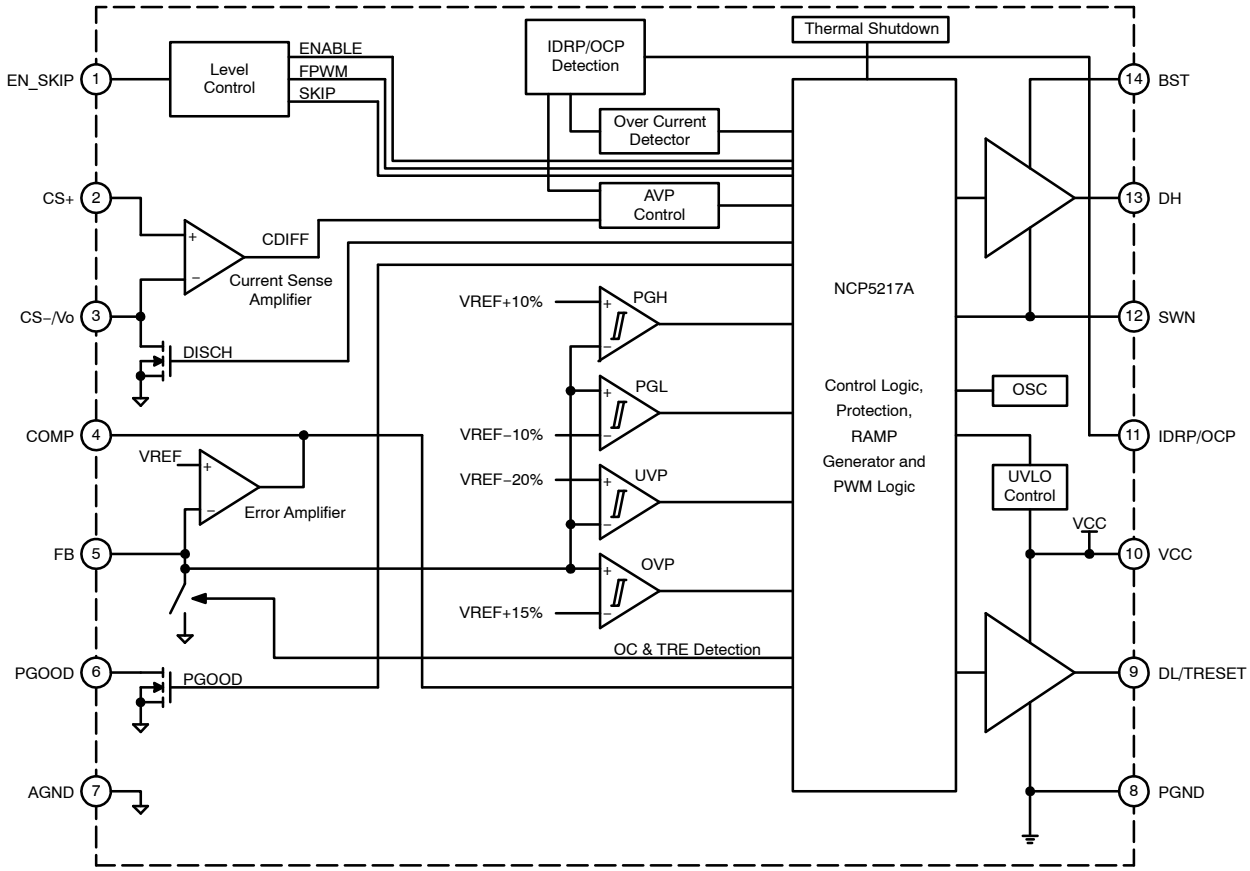


Figure 1. Block Diagram

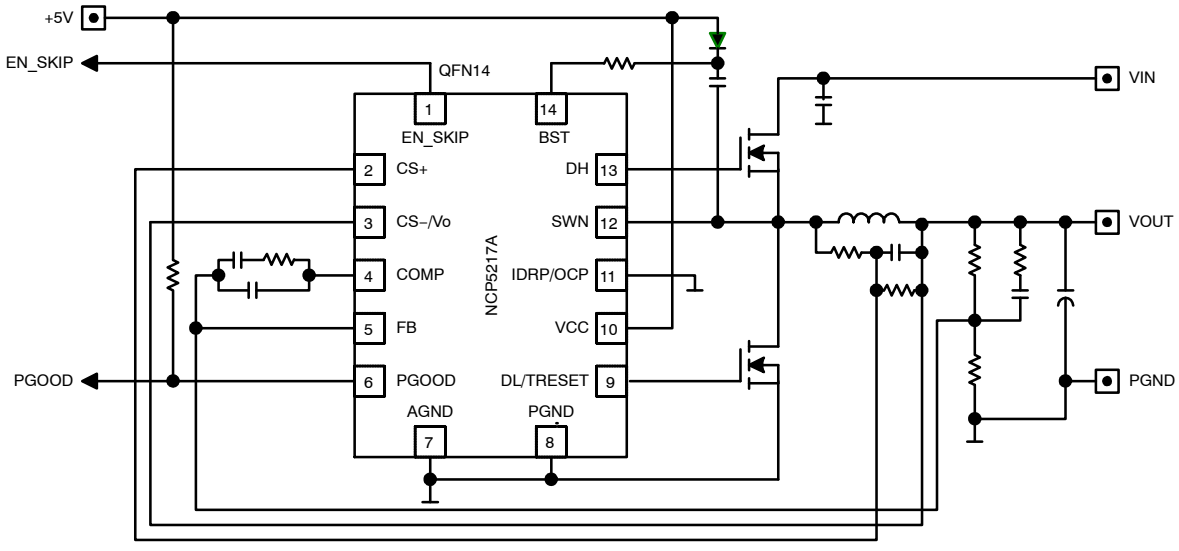


Figure 2. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	EN_SKIP	This pin serves as two functions. Enable: Logic control for enabling the switcher. SKIP: Power saving mode (Skip and Force PWM) programmable pin.
2	CS+	Inductor current differential sense non−inverting input.
3	CS−/Vo	Inductor current differential sense inverting input.
4	COMP	Output of the error amplifier.
5	FB	Output voltage feed back.
6	PGOOD	Power good indicator of the output voltage. High impendence (open drain) if power good (in regulation). Low impendence if power not good.
7	AGND	Analog ground.
8	PGND	Ground reference and high−current return path for the bottom gate driver.
9	DL/TRESET	Gate driver output of bottom N−channel MOSFET. It also has the function for TRESET.
10	VCC	Supply for analog circuit and bottom gate driver.
11	IDRP/OCP	Over current protection and Droop Voltage programmable pin.
12	SWN	Switch node between the top MOSFET and bottom MOSFET.
13	DH	Gate driver output of the top N−channel MOSFET.
14	BST	Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VCC Power Supply Voltage to AGND	VCC	−0.3, 6.0	V
High−side Gate Drive Supply: BST to SWN High−side Gate Drive Voltage: DH to SWN Low−side Gate Drive Supply: VCC to PGND Low−side Gate Drive Voltage: DL to PGND	$V_{BST}-V_{SWN}$, $V_{DH}-V_{SWN}$, $VCC-V_{PGND}$, $V_{DL}-V_{PGND}$,	−0.3, 6.0	V
Input / Output Pins to AGND	V_{IO}	−0.3, 6.0	V
Switch Node SWN	V_{SWN}	−5 V (< 100 ns) 30 V	V
High−Side Gate Drive/Low−Side Gate Drive Outputs	DH, DL	−3(DC)	V
PGND	V_{PGND}	−0.3, 0.3	V
Thermal Characteristics Thermal Resistance Junction−to−Ambient (QFN14 Package)	$R_{\theta JA\_QFN14}$	48	°C/W
Operating Junction Temperature Range (Note 1)	T_J	−40 to + 150	°C
Operating Ambient Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 55 to +150	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. Internally limited by thermal shutdown, 150°C min.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 5 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
Input Voltage	V_{IN}		4.5	–	27	V
V_{CC} Operating Voltage	V_{CC}		4.5	5.0	5.5	V
SUPPLY CURRENT						
V_{CC} Quiescent Supply Current in FPWM operation	IVCC_FPWM	EN_SKIP = 2.0 V, V_{FB} forced above regulation point. DH, DL are open		1.5	2.5	mA
V_{CC} Quiescent Supply Current in Power Saving Operation	IVCC_PS	EN_SKIP = 5 V, V_{FB} forced above regulation point, DH, DL are open		1.5	2.5	mA
V_{CC} Shutdown Current	IVCC_SD	EN_SKIP = L, V_{CC} = 5 V, true shutdown			1	uA
BST Quiescent Supply Current in FPWM operation	IBST_FPWM	EN_SKIP = 1.5 V, V_{FB} forced above regulation point, DH and DL are open, No boost trap diode			0.3	mA
BST Quiescent Supply Current in power−saving operation	IBST_PS	EN_SKIP = 5 V, V_{FB} forced above regulation point, DH and DL are open No boost trap diode			0.3	mA
BST Shutdown Current	IBST_SD	EN_SKIP = 0 V			1	μA
dV/dt on V_{CC}	dVCC/dt	(Note 2)	−10		10	V/μs
VOLTAGE−MONITOR						
Rising V_{CC} Threshold	VCCth+	Wake Up	4.05	4.25	4.48	V
V_{CC} UVLO Hysteresis	VCCHYS		200	275	400	mV
Power Good High Threshold	VPGH	PGOOD in from higher Vo (PGOOD goes high)	105	110	115	%
Power Good High Hysteresis	VPGH_HYS	PGOOD high hysteresis (PGOOD goes low)		5		%
Power Good Low Threshold	VPGL	PGOOD in from lower Vo (PGOOD goes high)	80	85	90	%
Power Good Low Hysteresis	VPGL_HYS	PGOOD low hysteresis (PGOOD goes low)		−5		%
Power Good High Delay	Td_PGH			150		us
Power Good Low Delay	Td_PGL			1.5		us
Output Overvoltage Rising Threshold	OVPth+	With respect to Error Comparator Threshold of 0.8 V	110	115	120	%
Overvoltage Fault Propagation Delay	OVPTblk	FB forced 2% above trip threshold		1.5		us
Output Undervoltage Trip Threshold	UVPth	With respect to Error Comparator Threshold of 0.8 V	75	80	85	%
Output Undervoltage Protection Blanking Time	UVPTblk		–	$8/f_{SW}$	–	s
REFERENCE OUTPUT						
Internal Reference Voltage	VREF		0.7936	0.8	0.8064	V
OSCILLATOR						
Operation Frequency	FSW		270	300	330	kHz
OVERCURRENT THRESHOLD DETECTION						
Total Detection Time	T_{DETECT}	A short period before SS	1.26	1.92	2.21	ms
OCSET Detection Time	T_OCDET	(Note 2)	1.09		1.47	ms

2. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 5 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
INTERNAL SOFT−START							
Soft−Start Time	T_{SS}			0.9	1.1	1.3	ms
VOLTAGE ERROR AMPLIFIER							
DC Gain	GAIN_VEA	(Note 2)			88		dB
Unity Gain Bandwidth	BW_VEA	(Note 2)			15		MHz
Slew Rate	SR_VEA	COMP PIN TO GND = 100 pF (Note 2)			2.5		V/μs
FB Bias Current	Ibias_FB					0.1	μA
Output Voltage Swing	Vmax_EA	Isource_EA = 2 mA		3.3	3.5		V
	Vmin_EA	Isink_EA = 2 mA			0.15	0.3	
DIFFERENTIAL CURRENT SENSE AMPLIFIER							
CS+ and CS− Common−mode Input Signal Range	VCSCOM_MAX	Refer to AGND				3.5	V
Input Bias Current	CS_IIB			−100		100	nA
Input Signal Range	CS_range			−70		70	mV
Offset Current at IDRP	IDRP_offset	(CS+) − (CS−) = 0 V		−1.0		1.0	μA
[(CS+) − (CS−)] to IDRP Gain	IDRP_GAIN (IDRP/((CS+) − (CS−)))	(CS+) − (CS−) = 10 mV, V(IDRP) = 0.8 V	T_A = 25°C	0.475	0.525	0.575	μA/mV
			T_A=−40°C to 85°C	0.425		0.625	
Current−Sense Bandwidth	BW_CS	At −3dB to DC Gain (Note 2)			20		MHz
Maximum IDRP Output Voltage	IDRP_Max	(CS+) − (CS−) = 70 mV, Isource drops to 95% of the value when $V_{(IDRP)}$ = 0.8 V		2.5			V
Minimum IDRP Output Voltage	IDRP_Min				0		V
IDRP Output current	I_IDRP			−1.0		35	μA
OVERCURRENT PROTECTION SETTING							
Overcurrent Threshold (OCTH) Detection Current	I_OCSET	Sourced from OCP before soft−start, Rocp = 16.7 kΩ is connected from OCP to AGND or FB		21.6	24	26.4	μA
Ratio of OC Threshold over OCSET Voltage	K_OCSET	V((CS+) − (CS−)) / V_OCSET (Note 2)			0.1		−
OCSET Voltage for Default Fixed OC Threshold	VOCSET_DFT	Rocp ≤ 2 kΩ is connected from OCP to AGND or FB				100	mV
OCSET Voltage for Adjustable OC Threshold	VOCSET_ADJ	Rocp = 8.3 ~ 25 kΩ is connected from OCP to AGND or FB		200		600	mV
OCSET Voltage for OC Disable	VOCSET_DIS	Rocp ≥ 35 kΩ is connected from OCP to AGND or FB		720			mV
Default Fixed OC Threshold	V_OCTH_DFT	(CS+) − (CS−), Pin IDRP/OCP is shorted to AGND or FB		35	40	45	mV
Adjustable OC Threshold	V_OCTH ((CS+) − (CS−))	(CS+) − (CS−), During OC threshold, set a voltage at pin OCP	VOCSET = 200 mV	15	20	25	mV
			VOCSET = 600 mV	52	60	68	
GATE DRIVERS							
DH Pull−HIGH Resistance	RH_DH	200 mA Source current			2.5		Ω
DH Pull−LOW Resistance	RL_DH	200 mA Sink current			1.5		Ω
DL Pull−HIGH Resistance	RH_DL	200 mA Source current			2		Ω
DL Pull−LOW Resistance	RL_DL	200 mA Sink current			0.75		Ω

2. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 5 V, T_A = −40°C to 85°C, unless other noted)

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
GATE DRIVERS							
DH Source Current	Isource_DH	(Note 2)			1		A
DH Sink Current	Isink_DH	(Note 2)			1.7		A
DL Source Current	Isource_DL	(Note 2)			1.3		A
DL Sink Current	Isink_DL	(Note 2)			3.3		A
Dead Time	TD_LH	DL−off to DH−on (Note 2)			20		ns
	TD_HL	DH−off to DL−on (Note 2)			20		
Negative Current Detection Threshold	NCD_TH	SWN−PGND, at EN_SKIP = 5 V			−1		mV
SWN source leakage	ISWN_SD	EN_SKIP = 0 V				1	uA
Internal Resistor from DH to SWN	R_DH_SWN	(Note 2)			100		kΩ
CONTROL SECTION							
EN_SKIP Logic Input Voltage for Disable	VEN_Disable	Set as Disable		0.7	1.0	1.3	V
		Hysteresis		150	200	250	mV
EN_SKIP Logic Input Voltage for FPWM	VEN_FPWM	Set as FCCM mode		1.7	1.95	2.25	V
EN_SKIP Logic Input Voltage for Skip Mode	VEN_SKIP	Set as SKIP Mode		2.35	2.6	2.85	V
		Hysteresis		100	175	250	mV
EN_SKIP Source Current	IEN_SOURCE	VEN_SKIP = 0 V				0.1	μA
EN_SKIP Sink Current	IEN_SINK	VEN_SKIP = 5 V				0.1	μA
PGOOD Pin ON Resistance	PGOOD_R	I_PGOOD = 5 mA			100		Ω
PGOOD Pin OFF Current	PGOOD_LK					1	μA
OUTPUT DISCHARGE MODE							
Output Discharge On−Resistance	Rdischarge	EN = 0 V			20	35	Ω
Threshold for Discharge Off	Vth_DisOff			0.2	0.3	0.4	V
TRE SETTING							
TRE Threshold Detection Current	I_TRESET	Source from DL in the short period before soft−start. (Rtre = 47 kΩ is connected from DL to GND		7.2	8	8.8	μA
Detection Voltage for TRE Threshold Selection	VDL_TRE_1 (Default)	Internal TRE_TH is set to 300 mV	Rtre ≥ 75 kΩ (Note 2)	500	600	700	mV
	VDL_TRE_2	Internal TRE_TH is set to 500 mV	Rtre = 44 ~ 50 kΩ (Note 2)	300		450	
	VDL_TRE_3	TRE is Disabled	Rtre ≤ 25 kΩ (Note 2)	0		250	
TRE Comparator Offset	TRE_OS	(Note 2)			10		mV
Propagation Delay of TRE Comparator	TD_PWM	(Note 2)			20		ns
THERMAL SHUTDOWN							
Thermal Shutdown	Tsd	(Note 2)			150		°C
Thermal Shutdown Hysteresis	Tsdhys	(Note 2)			25		°C

2. Guaranteed by design, not tested in production.

TYPICAL OPERATING CHARACTERISTICS

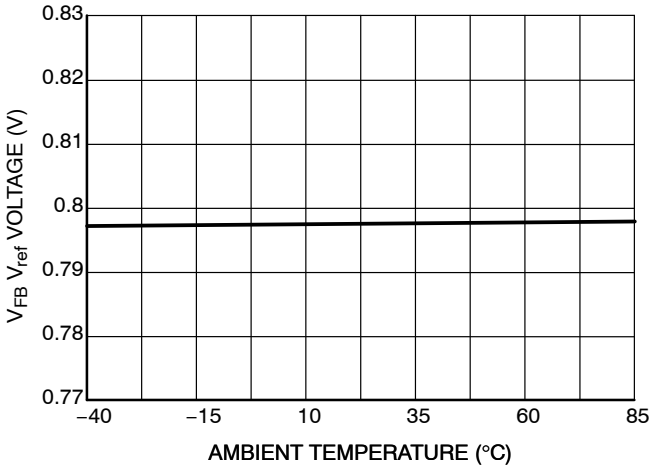


Figure 3. V_{ref} Voltage vs Ambient Temperature

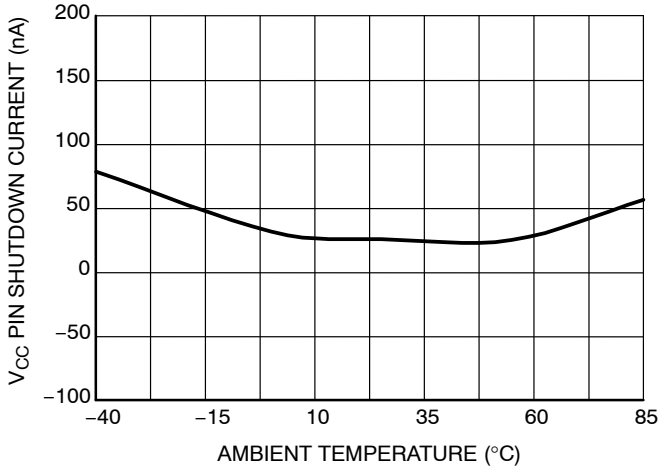


Figure 4. V_{CC} Shutdown Current vs Ambient Temperature

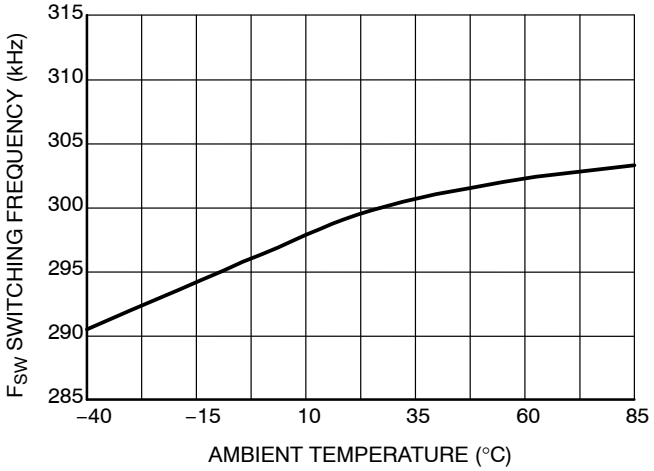


Figure 5. Switching Frequency vs Ambient Temperature

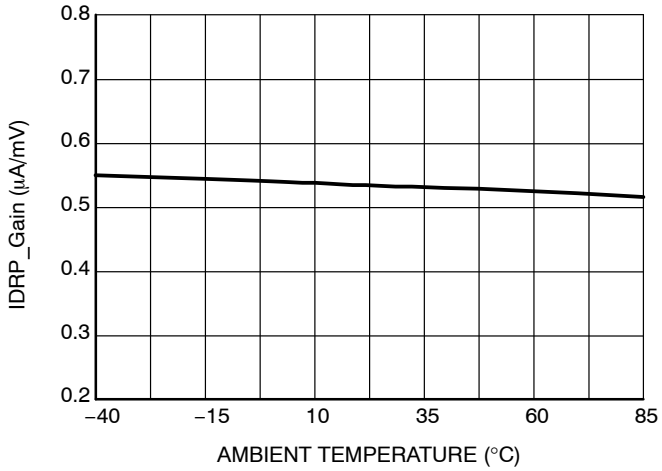


Figure 6. IDRP Gain vs Ambient Temperature

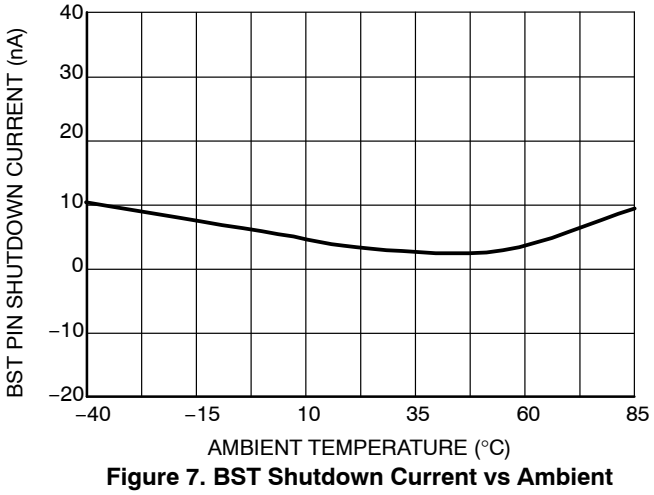


Figure 7. BST Shutdown Current vs Ambient Temperature

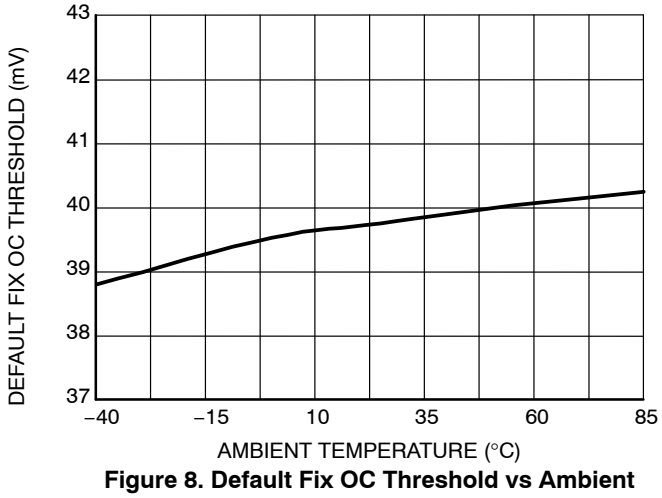
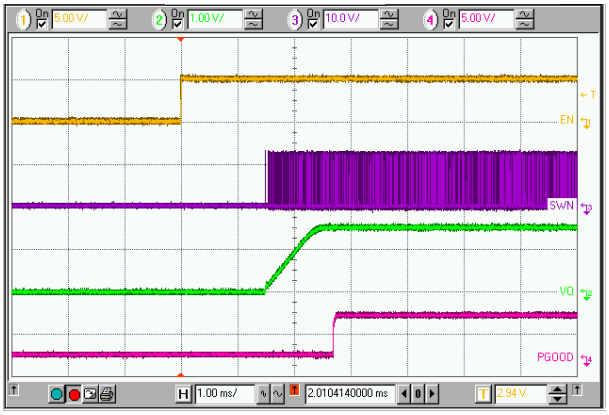


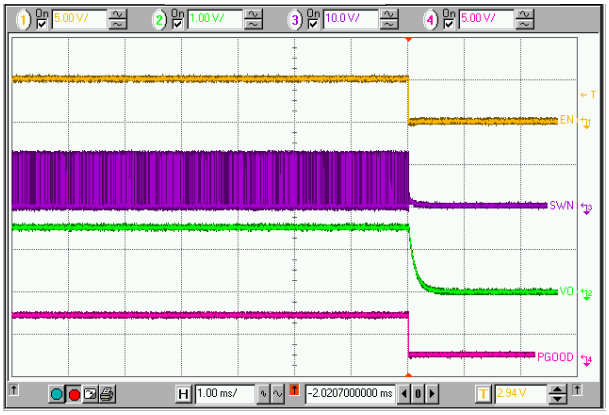
Figure 8. Default Fix OC Threshold vs Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS



Top to Bottom: EN, SWN, V_o, PGOOD

Figure 9. Powerup Sequence

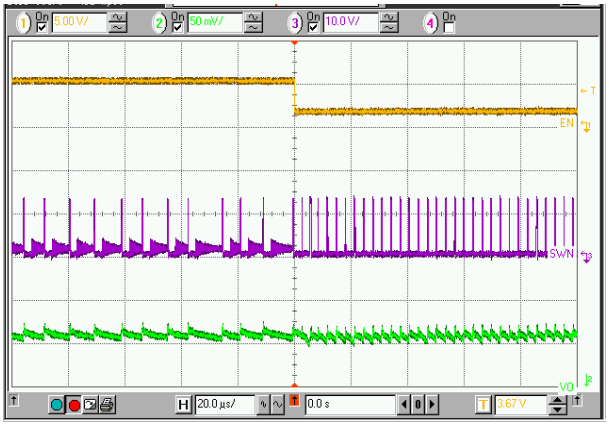


Top to Bottom: EN, SWN, V_o, PGOOD

Figure 10. Powerdown Sequence

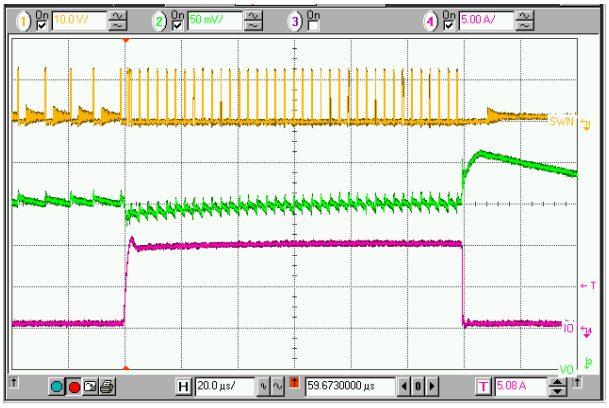
Top to Bottom: SWN_Slave, SWM, V_o

Figure 11. On Line Mode Change (CCM → DCM)



Top to Bottom: EN, SWM, V_o

Figure 12. On Line Mode Change (DCM → CCM)



Top to Bottom: SWN, Vo, Output Current

Figure 13. Typical Transient

DETAILED OPERATING DESCRIPTION

General

The NCP5217A synchronous step−down power controller contains a PWM controller for wide battery/adaptor voltage range applications

The NCP5217A includes power good voltage monitor, soft−start, over current protection, under−voltage protection, overvoltage protection and thermal shutdown. The NCP5217A features power saving function which can increase the efficiency at light load. It is ideal for battery operated systems. The IC is packaged in QFN14.

Control Logic

The internal control logic is powered by V_{CC}. The device is controlled by an EN_SKIP pin. The EN_SKIP serves two functions. When voltage of EN_SKIP is below VEN_Disable, it shuts down the device. When the voltage of EN_SKIP is between VEN_FPWM and VEN_SKIP, the device is operating as force PWM mode. When voltage level of EN_SKIP is above VEN_SKIP, the device is operating as power saving mode. When EN_SKIP is above VEN_Disable, the internal Vref is activated and power−on reset occurs which resets all the protection faults. Once Vref reaches its regulation voltage, an internal signal will wake up the supply under−voltage monitor which will assert a "GOOD" condition. In addition, the NCP5217A continuously monitors V_{CC} level with an undervoltage lockout (UVLO) function.

Forced PWM Operation (FPWM Mode)

The device is operating as force PWM mode if EN_SKIP voltage keeps at between VEN_FPWM and VEN_SKIP. Under this mode, the low−side gate driver signal is forced to be the complement of the high−side gate driver signal. This mode allows reverse inductor current, in such a way that it provides more accurate voltage regulation and better (fast) transient response. During the soft−start operation, the NCP5217A automatically runs as FPWM mode regardless of the EN_SKIP setting at either FPWM or SKIP mode to make sure to have smooth power up.

Pulse Skipping Operation (Skip Mode)

The device is operating as skip mode if EN_SKIP voltage keeps above VEN_SKIP. However, in medium and high load range, the controller still runs in continuous−conduction−mode (CCM) of which it behaves exactly same as FPWM mode. In light load range, the controller will go to skip mode which is similar to conventional constant on−time scheme.

Transient Response Enhancement (TRE)

For the conventional PWM controller in CCM, the fastest response time is one switching cycle in the worst case. To further improve transient response in CCM, a transient response enhancement circuitry is implemented inside the NCP5217A. In CCM operation, the controller is continuously monitoring the COMP pin output voltage of the error amplifier to detect the load transient events. The functional block diagram of TRE is shown below.

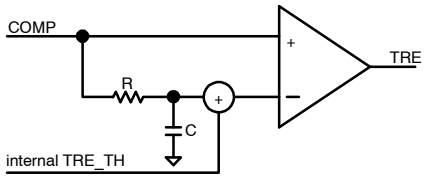
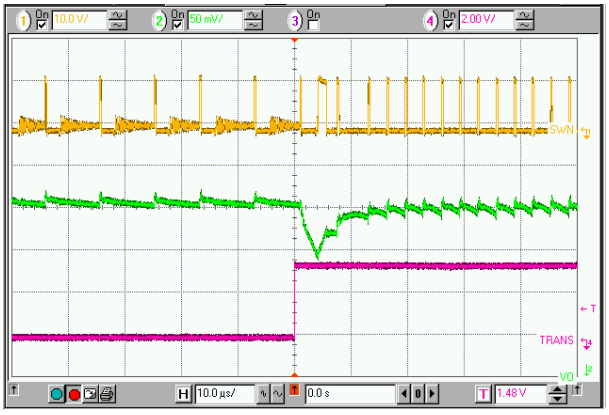


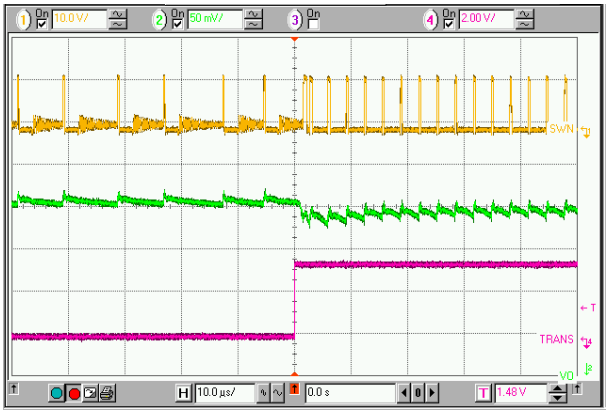
Figure 14. Block Diagram of TRE Circuit

Once the large transient occurs, the COMP signal may be large enough to exceed the threshold and then TRE "flag" signal will be asserted in a short period which is typically around one normal switching cycle. In this short period, the controller will be running at high frequency and hence has faster response. After that the controller comes back to normal switching frequency operation. We can program the internal TRE threshold (TRE_TH). For detail please see the electrical table of "TRE Setting" section. Basically, the recommend internal TRE threshold value is around 1.5 times of peak−to−peak value of the COMP signal at CCM operation. The higher the internal TRE_TH, the lower sensitivity to load transient. The TRE function can be disable by setting the Rtre which is connecting to DL/TRE pin to less than 25 kΩ. For system component saving, it is usually set as default value, that is, Rtre is open (≥ 75 kΩ) and internal TRE_TH is 300 mV typical.



Top to Bottom SWN, V_o, Transient Signal

Figure 15. Transient Response with TRE Disable



Top to Bottom SWN, V_o, Transient Signal

Figure 16. Transient Response with TRE Enable

Adaptive Voltage Positioning (AVP)

For applications with fast transient currents, adaptive voltage positioning can reduce peak−to−peak output voltage deviations due to load transients. With the use of AVP, the output voltage allows to have some controlled sag when load current is applied. Upon removal of the load, the output voltage returns no higher than the original level, just allowing one output transient peak to be cancelled over a load step up and release cycle. The amount of AVP is adjustable.

The behaviors of the V_o waveforms with or without AVP are depicted at Figure 17.

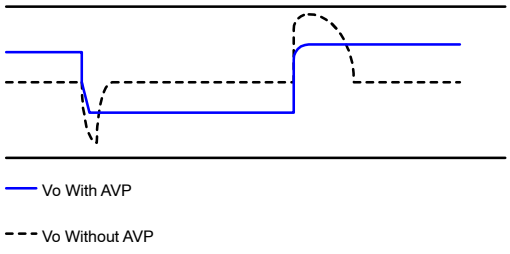


Figure 17. Adaptive Voltage Positioning

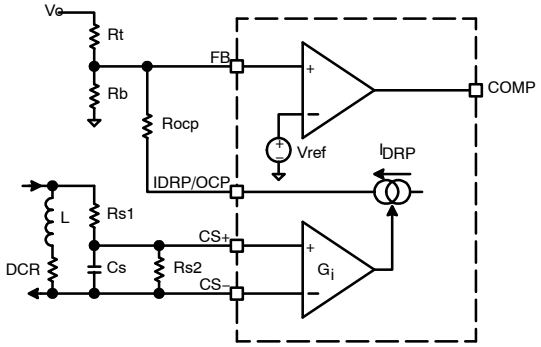


Figure 18. Configuration for AVP function

The Figure 18 shows how to realize the AVP function. A current path is connecting to the FB pin via R_{ocp} resistor. Rocp is not actually for AVP function, indeed, R_{ocp} is used for OCP threshold value programming. The IDRP/OCP pin has dual functions: OCP programming and AVP. At the IDRP/OCP pin, conceptually there is a current source which is modulated by current sensing amplifier.

The output voltage Vo with AVP is:

$$V_O = V_O0 - I_O * R_{LL} \quad \text{(eq. 1)}$$

Where I_o is the load current, no load output voltage Vo0 is set by the external divider that is

$$V_O0 = \left(1 + \frac{Rt}{Rb}\right) * V_{ref} \quad \text{(eq. 2)}$$

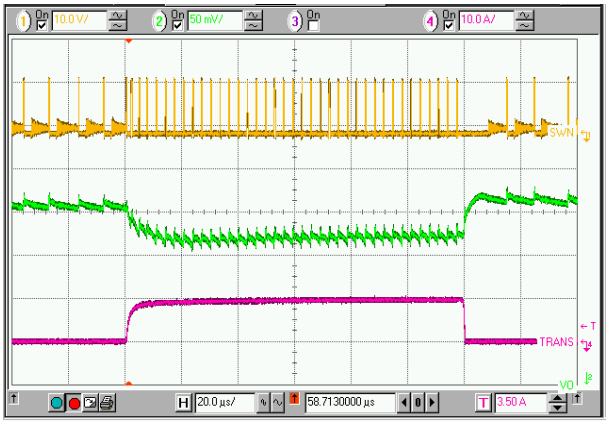
The load line impendence R_{LL} is given by:

$$R_{LL} = DCR * Gain\_CS * Rt * \frac{Rs2}{Rs1 + Rs2} \quad \text{(eq. 3)}$$

Where DCR is inductor DC resistance. Gain_CS is a gain from [(CS+) − (CS−)] to IDRP Gain (At electrical table, the symbol is IDRP_GAIN), the typical value is 0.525 μA/mV.

The AVP function can be easily disable by shorting the Rocp resistor into ground.

From the equation we can see that the value of “top” resistor Rt can affect the R_{LL}, so it is recommended to define the amount of R_{LL} FRIST before defining the compensation component value. And if the user wants to fine tune the compensation network for optimizing the transient performance, it is NOT recommend to adjust the value of Rt. Otherwise, both transient performance and AVP amount will be affected. The following diagram shows the typical waveform of AVP. Note that the Rt typical value should be above 1 kΩ.



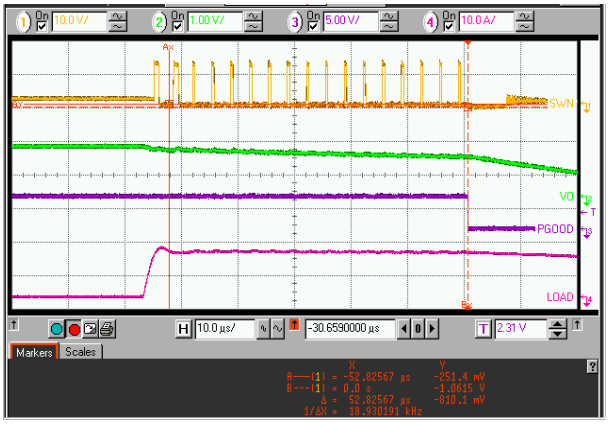
Top to Bottom: SWN, V_o, Transient Signal (0.5−10−0.5A)

Figure 19. Typical waveform of AVP

Overcurrent Protection (OCP)

The NCP5217A protects power system if over current event occurs. The current is continuously monitored by the differential current sensing circuit. The current limit threshold voltage VOCSET can be programmed by resistor Rocset connecting at the IDRP/OCP pin. However, fixed default VOCSET can be achieved if Rocset is less than 2 kΩ.

If the inductor current exceeds the current threshold continuously, the top gate driver will be turned off cycle by cycle. If it happens over consecutive 16 clock cycles time (16 x $1/f_{SW}$), the device is latched off such that top and bottom gate drivers are off. EN resets or power recycle the device can exit the fault. The following diagram shows the typical behavior of OCP.



Top to Bottom : SWN, V_o, PGOOD, I_o

Figure 20. Overcurrent Protection

The NCP5217A uses lossless inductor current sensing for acquiring current information. In addition, the threshold OCP voltage can be programmed to some desired value by setting the programming resistor Rocp.

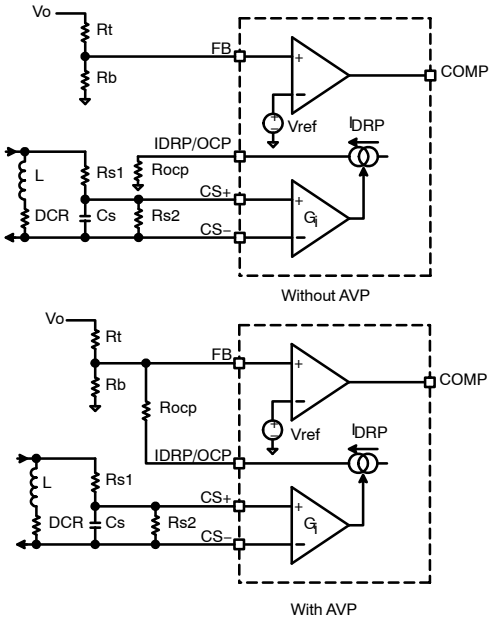


Figure 21. OCP Configurations

It should be noted that there are two configurations for Rocp resistor. If Adaptor Voltage Position (AVP) is used, the Rocp should be connected to FB pin. If AVP is not used, the Rocp should be connected to ground. At the IDRP/OCP pin, there is a constant current(24 μA typ.) flowing out during the programming stage at system start up. This is used to sense the voltage level which is developed by a resistor R_{ocp} so as to program the overcurrent detection threshold voltage. For typical application, the V_{octh} is set as default value (40 mV typ) by setting R_{ocp} = 0 Ω, or directly short the IDRP/OCP pin to ground. It has the benefit of saving one component at application board. For other programming values of V_{octh}, please refer to the electrical table of "Overcurrent Protection Setting" section.

Guidelines for selecting OCP Trip Component

1. Choose the value of R_{ocp} for V_{octh} selection. (typical is 0 Ω for V_{octh} = 40 mV typical)
2. Define the DC value of OCP trip point (I_{OCP_DC}) that you want. The typical value is 1.5 to 1.8 times of maximum loading current. For example, if maximum loading is 10 A, then set OCP trip point at 15 A to 18 A.
3. Calculate the inductor peak current (I_{pk})which is estimated by the equation:

$$I_{pk} = I_{OCP\_DC} + \frac{V_O * (V_{IN} - V_O)}{2 * V_{IN} * f_{SW} * L_O} \quad \text{(eq. 4)}$$

4. Check with inductor datasheet to find out the value of inductor DC resistance DCR, then calculate the RS1, RS2 dividing factor k based on the equation:

$$k = \frac{V_{OCth}}{I_{pk} * DCR} \quad \text{(eq. 5)}$$

5. Select Cs value between 100 nF to 200 nF. Typically, 100 nF will be used.
6. Calculate Rs1 value by the equation:

$$Rs1 = \frac{L}{k * DCR * Cs} \quad \text{(eq. 6)}$$

7. Calculate Rs2 value by the equation:

$$Rs2 = \frac{k * Rs1}{1 - k} \quad \text{(eq. 7)}$$

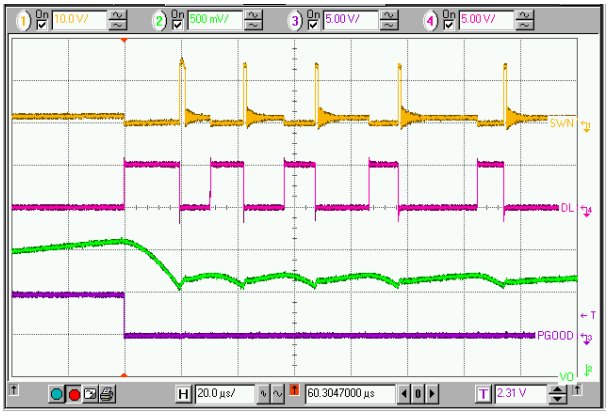
8. Hence, all the current sense components Rs1, Rs2, Cs have been found for target I_{OCP_DC}.
9. If Rs2 is not used (open), set k = 1, at that moment, the I_{pk} will be restricted by:

$$I_{pk} = \frac{V_{OCth}}{DCR} \quad \text{(eq. 8)}$$

Overvoltage Protection (OVP)

When V_{FB} voltage is above 115% (typical) of the nominal V_{FB} voltage for over 1.5 μs blanking time, an OV fault is set. At that moment, the top gate drive is turned off and the bottom gate drive is turned on until the V_{FB} below lower under voltage (UV) threshold and bottom gate drive is

turned on again whenever V_{FB} goes above upper UV threshold. EN resets or power recycle the device can exit the fault. The following diagram shows the typical waveform when OVP event occurs.

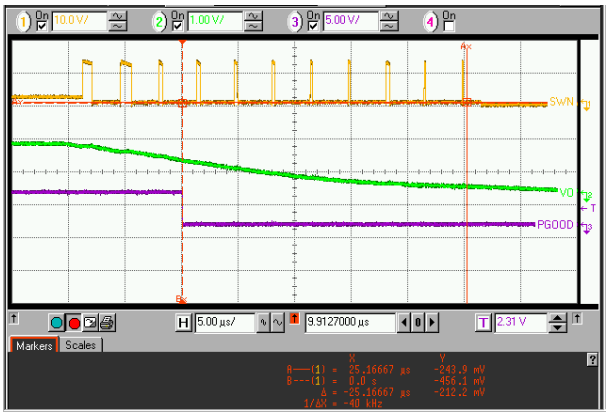


Top to Bottom : SWN, DL, V_o, PGOOD

Figure 22. Overvoltage Protection

Undervoltage Protection (UVP)

An UVP circuit monitors the V_{FB} voltage to detect under voltage event. The undervoltage limit is 80% of the nominal V_{FB} voltage. If the V_{FB} voltage is below this threshold over consecutive 8 clock cycles, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault.



Top to Bottom : SWN, V_o, PGOOD

Figure 23. Undervoltage Protection

Thermal Shutdown

The IC will shutdown if the die temperature exceeds 150°C. The IC restarts operation only after the junction temperature drops below 125°C.

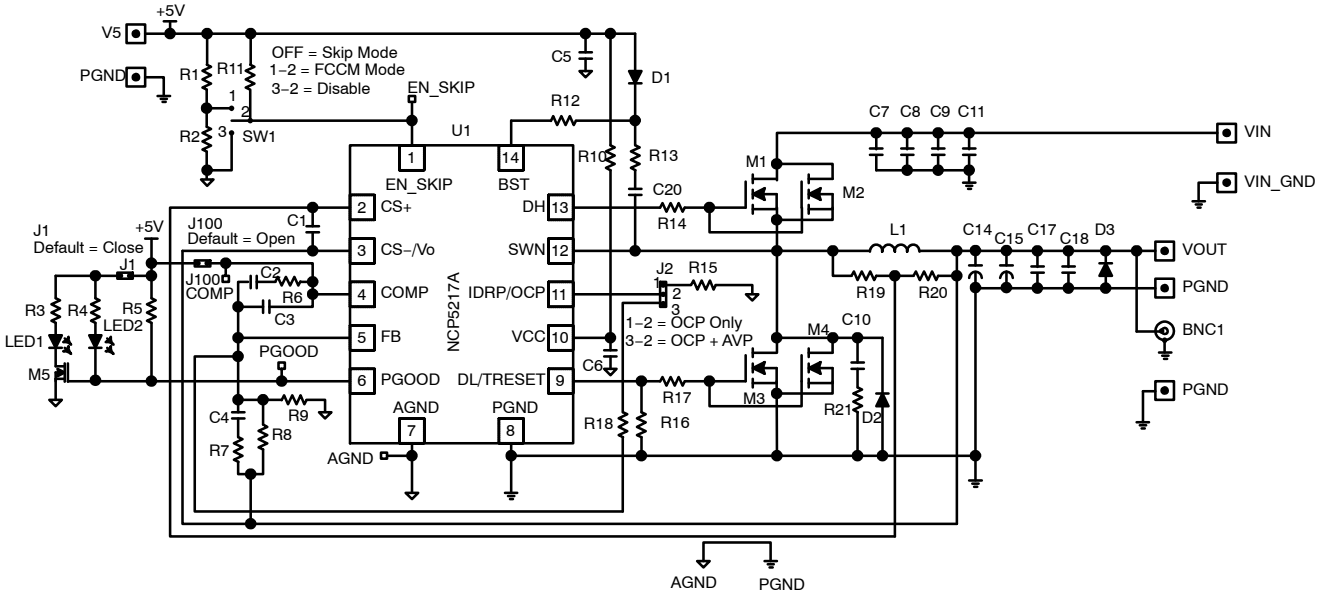


Figure 24. Demo Board Schematic

DEMO BOARD BILL OF MATERIAL BOM (See next tables for compensation network and power stage)

Designator	Qty	Description	Value	Footprint	Manufacturer	Manufacturer P/N
U1	1	Single Synchronous Stepdown Controller	–	QFN14 (Special)	ON Semiconductor	NCP5217MNR2G
R1	1	Chip Resistor, ±5%	75k	0603	Panasonic	ERJ3GEYJ753V
R2	1	Chip Resistor, ±5%	10k	0603	Panasonic	ERJ3GEYJ103V
R3, R4	2	Chip Resistor, ±5%	1k	0603	Panasonic	ERJ3GEYJ102V
R5	1	Chip Resistor, ±5%	100k	0603	Panasonic	ERJ3GEYJ104V
R10	1	Chip Resistor, ±5%	5.6	0603	Panasonic	ERJ3GEYJ5R6V
R11	1	Chip Resistor, ±5%	20k	0603	Panasonic	ERJ3GEYJ203V
R12	1	Chip Resistor, ±5%	5.6	0603	Panasonic	ERJ3GEYJ5R6V
R13, R14, R15, R17	4	Chip Resistor, ±5%	0	0603	Panasonic	ERJ3GEYJR00V
R16, R18, R21,	3	–	DNP	–	–	–
C1	1	MLCC Chip Capacitor, ±10% Temp Char: X7R, Rate V = 50 V	100 nF	0603	Panasonic	ECJ1VB1E104K
C5, C6	2	MLCC Chip Capacitor, ±20% Temp Char: X5R, Rate V=25V	1 μF	0805	Panasonic	ECJ2FB1E105M
C7,C8,C9, C11	4	MLCC Chip Capacitor, ±20% Temp Char: X5R, Rate V = 25 V	4.7 μF	0805	Panasonic	ECJ2FB1E475M
C10, C13, C17, C18	4	–	DNP	–	–	–
C20	1	MLCC Chip Capacitor, ±20% Temp Char: X7R, Rate V = 50 V	0.1 μF	0603	Panasonic	ECJ1VB1E104M
D1	1	30V Schottky Diode Vf=0.35V @ 10mA	–	SOT−23	ON Semiconductor	BAT54LT1
D2, D3	1	–	DNP	–	–	–
M5	1	Power MOSFET 50 V, 200 mA Single N−Channel	–	SOT−23	ON Semiconductor	BSS138L
LED1	1	Surface Mount LED (Green)	–	0805	LUMEX	SML−LX0805GC−TR
LED2	1	Surface Mount LED (Red)	–	0805	LUMEX	SML−LX0805IC−TR
J1, J100, COMP, EN_SKIP, PGOOD, AGND	6	Pin Header Single Row	–	Pitch=2.54 mm	Betamax	2211S−40G−F1
V5, VIN, VIN_GND, PGND, PGND, PGND, VOUT	7	Terminal Pin	–	f = 1.74 mm	HARWIN	H2121−01
BNC1	1	SMB SMT Straight Socket	–	5.1 x 5.1 mm	Tyco Electronics	RS Stock# 420−5401
SW1	1	2P ON−OFF−ON toggle switch	–	3 pins, 2.54 mm pitch	C & K	RS Stock# 249−2984 Manufacturer # 7203SYCQE

DEMO BOARD BILL OF MATERIAL (V_o = 1.1 V, I_o = 15 A)

Item	Component	Value	Tol	Footprint	Manufacturer	Manufacturer P/N
Compensation Network	R6	100k	1%	0603	Panasonic	ERJ3EKF1003V
	R7	560	1%	0603	Panasonic	ERJ3EKF5600V
	R8	3k	1%	0603	Panasonic	ERJ3EKF3001V
	R9	8k	1%	0603	Panasonic	ERJ3EKF8001V
	C2	470 pF	10%	0603	Panasonic	ECJ1VC1H471K
	C3	15 pF	10%	0603	Panasonic	ECJ1VC1H150K
	C4	1.2 nF	10%	0603	Panasonic	ECJ1VB1H122K
Power Stage & Current Sense	M1, M2	–	–	SOIC8−FL	ON Semiconductor	NTMFS4821N
	M3, M4	–	–	SOIC8−FL	ON Semiconductor	NTMFS4847N
	L1	1 μH	20%	10x11.5mm	Cyntec	PCMC104T−1R0MN
	R19	6.2k	1%	0603	Panasonic	ERJ3EKF6201V
	R20	9.1k	1%	0603	Panasonic	ERJ3EKF9101V
	C14, C15	330 μF 6 mΩ	20%	7343	Panasonic	EEFSX0D331XR
					Sanyo	2TPLF330M6

DEMO BOARD BILL OF MATERIAL (V_o = 1.5 V, I_o = 8 A)

Item	Component	Value	Tol	Footprint	Manufacturer	Manufacturer P/N
Compensation Network	R6	82k	1%	0603	Panasonic	ERJ3EKF8202V
	R7	1k	1%	0603	Panasonic	ERJ3EKF1001V
	R8	5k	1%	0603	Panasonic	ERJ3EKF5001V
	R9	5.71k	1%	0603	Panasonic	ERJ3EKF5711V
	C2	270 pF	10%	0603	Panasonic	ECJ1VC1H271K
	C3	15 pF	10%	0603	Panasonic	ECJ1VC1H150K
	C4	560 pF	10%	0603	Panasonic	ECJ1VB1H561K
Power Stage & Current Sense	M1, M3	–	–	SO8	ON Semiconductor	NTMS4705N
	M2, M4	DNP	–	–	–	–
	L1	1 μH	20%	10x11.5mm	Cyntec	PCMC104T−1R0MN
				13x14x4.9mm	WE	744315120
Power Stage & Current Sense	R19	4.3k	1%	0603	Panasonic	ERJ3EKF4301V
	R20	DNP	–	–	–	–
	C14, C15	220 μF 12 mΩ	20%	7343	Panasonic	EEFUD0D221XR
					Sanyo	2R5TPL220MC

DEMO BOARD BILL OF MATERIAL (V_o = 1.8 V, I_o = 8 A)

Item	Component	Value	Tol	Footprint	Manufacturer	Manufacturer P/N
Compensation Network	R6	150k	1%	0603	Panasonic	ERJ3EKF1503V
	R7	1k	1%	0603	Panasonic	ERJ3EKF1001V
	R8	5k	1%	0603	Panasonic	ERJ3EKF5001V
	R9	4K	1%	0603	Panasonic	ERJ3EKF4001V
	C2	220pF	10%	0603	Panasonic	ECJ1VC1H221K
	C3	18pF	10%	0603	Panasonic	ECJ1VC1H180K
	C4	560pF	10%	0603	Panasonic	ECJ1VB1H561K
Power Stage & Current Sense	M1, M3	–	–	SO8	ON Semi	NTMS4705N
	M2, M4	DNP	–	–	–	–
	L1	1.2uH	20%	10x11.5mm	TOKO	FDA1254−1R2M=P3
	R19	4.3K	1%	0603	Panasonic	ERJ3EKF4301V
	R20	DNP	–	–	–	–
	C14, C15	220uF 12mΩ	20%	7343	Panasonic	EEFUD0D221XR
					Sanyo	2R5TPL220MC

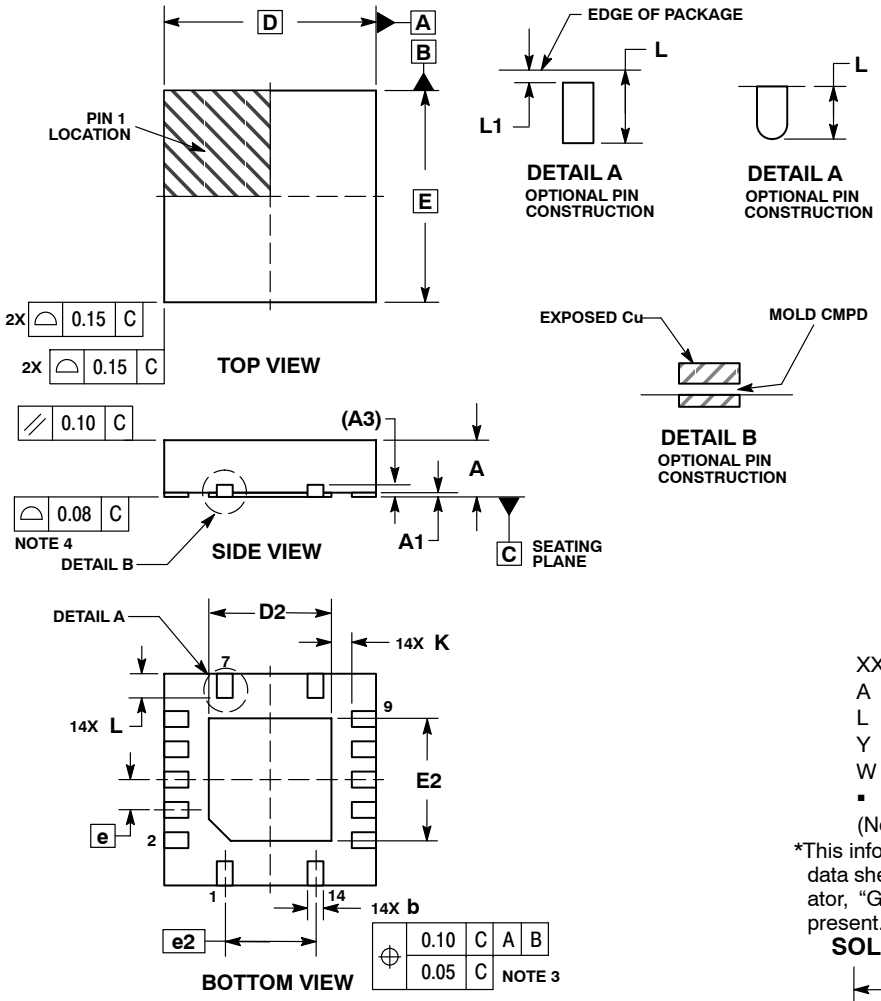
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

QFN14 3.5x3.5, 0.5P
CASE 485AL−01
ISSUE O

DATE 03 OCT 2007

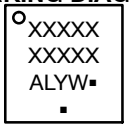
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.50 BSC	
D2	1.90	2.15
E	3.50 BSC	
E2	1.90	2.15
e	0.50 BSC	
e2	1.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.03

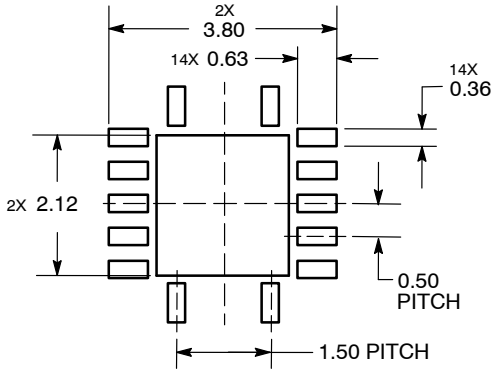
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON25416D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN14 3.5 X 3.5, 0.5P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Switching Controllers ***category:***

Click to view products by ON Semiconductor ***manufacturer:***

Other Similar products are found below :

AZ7500EP-E1 NCP1218AD65R2G NCP1234AD100R2G NCP1244BD065R2G NCP1336ADR2G NCP6153MNTWG NCP81101BMNTXG NCP81205MNTXG SJE6600 SMBV1061LT1G SG3845DM NCP4204MNTXG NCP6132AMNR2G NCP81102MNTXG NCP81203MNTXG NCP81206MNTXG NX2155HCUPTR UBA2051C MAX8778ETJ+ NTBV30N20T4G NCP1240AD065R2G NCP1240FD065R2G NCP1361BABAYSNT1G NTC6600NF NCP1230P100G NCP1612BDR2G NX2124CSTR SG2845M NCP81101MNTXG TEA19362T/1J IFX81481ELV NCP81174NMNTXG NCP4308DMTTWG NCP4308DMNTWG NCP4308AMTTWG NCP1251FSN65T1G NCP1246BLD065R2G NTE7154 NTE7242 LTC7852IUFD-1#PBF LTC7852EUFD-1#PBF MB39A136PFT-G-BND-ERE1 NCP1256BSN100T1G LV5768V-A-TLM-E NCP1365BABCYDR2G NCP1365AABCYDR2G MCP1633T-E/MG NCV1397ADR2G NCP1246ALD065R2G AZ494AP-E1