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# Synchronous Buck Controller with 2-Bit VID Inputs

# NCP5269B

NCP5269B is a synchronous buck controller that is optimized for converting the battery voltage or adaptor voltage into power supply rails required in notebook and desktop system. NCP5269B is designed for applications requiring dynamically selected slew−rate controlled output voltages. The soft−start is programmed by a single capacitor. Voltage identification logic−inputs select four resistor programmed set−point reference voltages that directly set the output voltage of the converter between 0.65 V to 1.5 V. NCP5269B supports high efficiency, fast transient response and provides power good signal. Forced CCM operation provides DDR termination voltage with source/sink capability. The part operates with input voltage ranging from 3.3 V to 28 V. NCP5269B is available in a 20−pin 3 mm x 3 mm QFN package.

### Features

- Wide Input Voltage Range: from 3.3 V to 28 V
- Three Selectable Fixed Frequency 300 kHz, 400 kHz or 600 kHz
- 2−Bit VID Selects Four Independent Voltages from 0.65 V to 1.5 V
- ±1.0% System Accuracy
- Differential Remote Output Voltage Sensing
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Build−in Power−Good Masking Supports Voltage Identification (VID) On−The−Fly Transients
- Simple Resistor Programming Voltage Levels
- Programmable Soft−Start through a Single Capacitor
- Forced CCM Operation
- Input Supply Voltage Feed Forward Control
- Resistive or Lossless Inductor's DCR Current Sensing
- Over−Temperature Protection
- Built−in Adaptive Gate Drivers
- Output Discharge Operation
- Built−in Over−Voltage, Under−Voltage and Over−Current Protection and Power Good Output
- This is a Pb−Free Device

### Applications

- Notebooks, Desktops & Servers
- DDR Termination Voltage
- I/O Supplies
- System Power Supplies
- Graphic Cards

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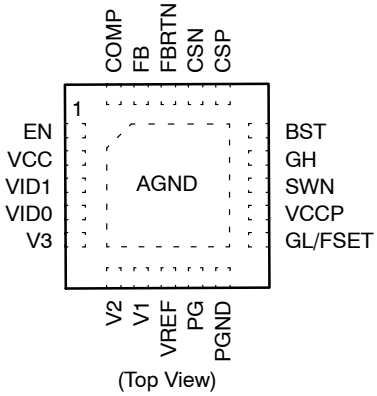
**20 PIN QFN, 3x3**
**MN SUFFIX**
**CASE 485BC**

**MARKING DIAGRAM**


| | |
|---|---|
| 5269B | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP5269BMNTWG | QFN20 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

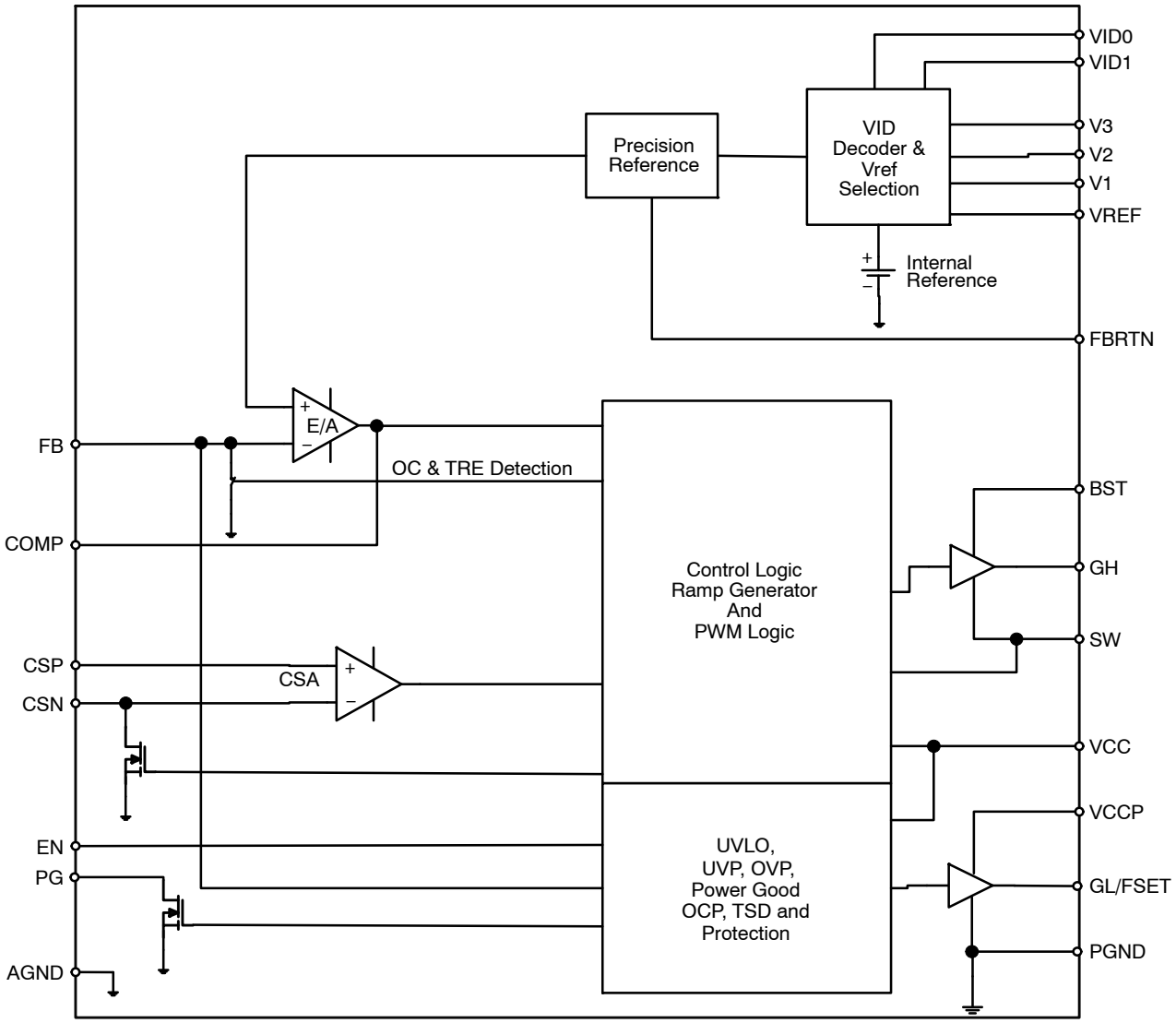



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTIONS**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | EN | Logic control for enabling the switcher. Applying greater than 1.4 V will turn on the part. Connect to GND to disable. |
| 2 | VCC | Supply for analog circuit. |
| 3 | VID1 | Logic input for reference voltage selector. Use in conjunction with the VID0 pin to select among four set−point reference voltages. |
| 4 | VID0 | Logic input for reference voltage selector. Use in conjunction with the VID1 pin to select among four set−point reference voltages. |
| 5 | V3 | Voltage set−point programming resistor input. |
| 6 | V2 | Voltage set−point programming resistor input. |
| 7 | V1 | Voltage set−point programming resistor input. External reference input when enabled by connecting the V3 pin to the VCC pin. |
| 8 | VREF | Soft−start programming capacitor input. Set-point reference voltage programming resistor input. Connects internally to the inverting input of the VSET voltage set-point amplifier. |
| 9 | PG | Power good indicator of the output voltage. Open−drain output. |
| 10 | PGND | Ground reference and high−current return path for the bottom gate driver. |
| 11 | GL/FSET | Gate driver output of bottom N−channel MOSFET. And it is also used to set up switching frequency by connecting a resistor from this pin to ground. |
| 12 | VCCP | Power supply for MOSFET gate drive |
| 13 | SWN | Switch node between the top MOSFET and bottom MOSFET. |
| 14 | GH | Gate driver output of the top N−channel MOSFET. |
| 15 | BST | Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin. |
| 16 | CSP | Inductor current differential sense non−inverting input. |
| 17 | CSN | Inductor current differential sense inverting input. |
| 18 | FBRTN | Feedback Return Input/Output. This pin remotely senses the output voltage. It is also used as the ground return for the VID reference voltage and the voltage error amplifier blocks. |
| 19 | FB | Output voltage feed back. |
| 20 | COMP | Output of the error amplifier. |
|  | AGND | Analog ground. Bottom thermal pad. |

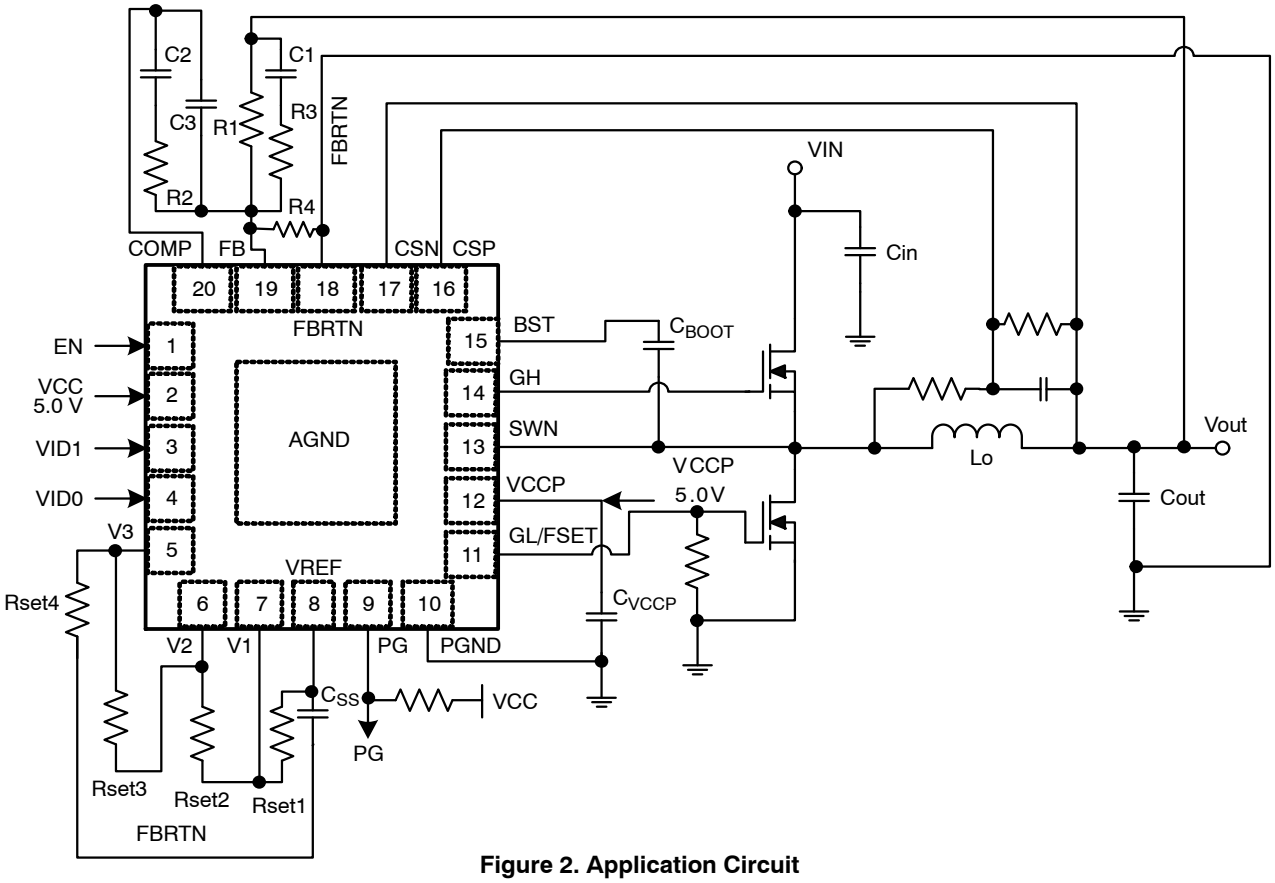



**Figure 2. Application Circuit**

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating | Value |
|---|---|
| VCC to AGND | −0.3 V (DC) to 6.5 V |
| FBRTN, PGND | −0.3 V to +0.3 V |
| SWN to PGND | −5.0 V to 28 V, −10.0 V for T < 100 ns |
| BST, GH to GND | −0.3 V to 34 V |
| BST to SWN, GH to SWN, VCC to PGND, DL to PGND | −0.3 V to 6.5 V |
| All other pins | −0.3 V to 6.5 V |
| Operating Temperature Range, $T_A$ | −40°C to +100°C |
| Junction Temperature, $T_J$ | −40°C to +100°C |
| Storage Temperature Range, $T_S$ | −55°C to +150°C |
| Package Characteristic<br>Thermal Resistance from Junction−to−Ambient ($T_A$ = +25°C), $R_{thja}$ | 35 °C/W (Note 1) |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This data is for solder on 4−layer board with 2 oz. copper.

**Table 3. ELECTRICAL CHARACTERISTICS**
($V_{CC}$ = $V_{CCP}$ = 5.0 V, $V_{out}$ = 1.0 V, $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| VCC Operation Voltage | $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| VCCP Operation Voltage | $V_{CCP}$ | | 4.5 | 5 | 5.5 | V |
| **VOLTAGE MONITORING & PROTECTION** | | | | | | |
| VCC Start Threshold | | | 3.9 | 4.2 | 4.45 | V |
| VCC UVLO Hysteresis | | | 300 | 350 | 400 | mV |
| Power Good Low Voltage | | $I_{PG(sink)}$ = 4 mA | | 230 | 300 | mV |
| Power Good High Leakage Current | | | | | 1.0 | μA |
| Power Good Startup Delay (Note 2) | | Measure from SSEND to PG pos edge | | 3.3 | | ms |
| Power Good Propagation Delay | | Delay for power good in | | 3.3 | | ms |
| | | Delay for power good out | | 1.5 | | μs |
| Power Good Threshold | | Power Good in from high | 101.5 | 105 | 107.5 | % |
| | | Power Good in from low | 92.5 | 95 | 98.5 | % |
| | | PG hysteresis | | 5 | | % |
| Power Good Masking Time | | Triggered by any VID Change | | 425 | | μs |
| FB Overvoltage Threshold | $V_{OVFB}$–VID | Relative to nominal VID Voltage | 150 | 200 | 250 | mV |
| Overvoltage Propagation Delay | | | | 1.5 | | μs |
| FB Over Voltage Threshold During Soft–Start | | | | 2.0 | | V |
| FB Under–Voltage Trip Threshold | $V_{UVFB}$–VID | Relative to nominal VID Voltage | −360 | −300 | −240 | mV |
| Undervoltage Protection Blanking Time | | | | 3.3 | | μs |
| **SUPPLY CURRENT** | | | | | | |
| VCC Quiescent Current | $I_{VCC}$ | $V_{skip}$ = 0 V, $V_{FB}$ = 1.5 V, EN = 5.0 (No Switching), GH and GL are open | | 3.9 | 5 | mA |
| VCC Shutdown Supply Current | $I_{VCC\_SD}$ | EN = 0 V | | | 3 | μA |
| VCCP Quiescent Current | $I_{VCCP}$ | $V_{skip}$ = 0 V, $V_{FB}$ = 1.5 V, EN = 5.0 (No Switching), GH and GL are open | | | 0.3 | mA |
| VCCP Shutdown Supply Current | $I_{VCCP\_SD}$ | EN = 0 V | | | 1 | μA |
| BST Quiescent Current | $I_{BST}$ | $V_{skip}$ = 0 V, $V_{FB}$ = 1.5 V, EN = 5.0 (No Switching), GH and GL are open | | | 0.33 | mA |
| BST Shutdown Supply Current | $I_{BST\_SD}$ | EN = 0, BST = 5 V, SWN = 0 | | | 1 | μA |
| **FEEDBACK VOLTAGE** | | | | | | |
| Reference Voltage | $V_{REF}$ | | | 0.65 | | V |
| System Accuracy | | VID0 = VID1 = High, PWM in CCM mode, −40°C < $T_A$ < 100°C | −1.0 | | +1.0 | % |
| | | $T_A$ = 25°C | −0.35 | | +0.35 | % |
| Feedback Voltage Line Regulation | | Vcc = 4.5 V ~ 5.5 V | | | 0.75 | %/V |

2. Guaranteed by characterization or correlation, not production tested

**Table 3. ELECTRICAL CHARACTERISTICS**
($V_{CC}$ = $V_{CCP}$ = 5.0 V, $V_{out}$ = 1.0 V, $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VOLTAGE ERROR AMPLIFIER** | | | | | | |
| Open Loop DC Gain (Note 2) | | | 80 | | | dB |
| Open Loop Unity Gain Bandwidth (Note 2) | $F_{0dB,EA}$ | | | 20 | | MHz |
| FB Input Voltage Range (Note 2) | | | 0 | | 2.0 | V |
| FB Bias Current (Note 2) | | Relative to CSN = VID | −1 | | 1 | μA |
| Slew Rate | | COMP pin to GND = 10 pF | | 10 | | V/μs |
| Maximum Output Voltage | | 10 mV of overdrive, $I_{SOURCE}$ = 2.0 mA | 3.3 | 3.5 | | V |
| Minimum Output Voltage | | 10 mV of overdrive, $I_{SINK}$ = 2.0 mA | | 0.2 | 0.3 | V |
| Output Source Current | | 10 mV of overdrive, $V_{out}$ = 3.5 V | 2 | | | mA |
| Output Sink Current | | 10 mV of overdrive, $V_{out}$ = 1.0 V | 2 | | | mA |
| **DIFFERENTIAL CURRENT SENSE AMPLIFIER** | | | | | | |
| CSP and CSN Common−mode Input Voltage Range | | Refer to AGND | −0.2 | | 2.0 | V |
| Differential Input Voltage Range | | | −30 | | 30 | mV |
| **OVER CURRENT PROTECTION** | | | | | | |
| OCP Threshold | | V(CSP)−V(CSN),<br>Vo = 1 V<br>Vo = 0.5 V ~ 1.5 V | <br>27<br>26 | <br>30<br>30 | <br>33<br>34 | mV |
| **2_BITS VID** | | | | | | |
| VID0, VID1 High Threshold Voltage | | | 0.65 | | | V |
| VID0, VID1 Low Threshold Voltage | | | | | 0.4 | V |
| VID0, VID1 Input Bias Current | | VID = 0 V | | 1 | | nA |
| VID0, VID1 Pull Down Current | | | | 2.5 | | μA |
| Charging current during VID up (Note 2) | | | | 73 | | μA |
| Discharging current during VID down (Note 2) | | | | 90 | | μA |
| VID Delay time | | Any VID edge to 10% of FB change | 200 | | | ns |
| **EN** | | | | | | |
| EN High Threshold Voltage | | | 1.4 | | | V |
| EN Low Threshold Voltage | | | | | 0.4 | V |
| EN Input Bias Current | $I_{EN}$ | EN = 5 V | | | 10 | μA |
| EN Input Voltage | | | | | 5.5 | V |
| **PWM** | | | | | | |
| Minimum Controllable ON Time (Note 2) | | | | 30 | | ns |
| Minimum OFF Time (Note 2) | | | 300 | 400 | 500 | ns |
| PWM Ramp Amplitude (Note 2) | | $V_{IN}$ = 5 V | | 1.25 | | V |
| | | $V_{IN}$ = 12 V | | 3 | | V |

2. Guaranteed by characterization or correlation, not production tested

**Table 3. ELECTRICAL CHARACTERISTICS**
($V_{CC}$ = $V_{CCP}$ = 5.0 V, $V_{out}$ = 1.0 V, $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **INTERNAL BST DIODE** | | | | | | |
| Forward Voltage Drop | | $I_F$ = 10 mA, $T_A$ = 25°C | | 0.3 | | V |
| Reverse−bias Leakage Current | | $V_{BST}$ = 34 V, $V_{SW}$ = 28 V, $T_A$ = 25°C | | 0.1 | 1 | μA |
| **SOFT STOP** | | | | | | |
| Output Discharge On−Resistance | | EN = 0, $V_{out}$ = 0.65 V | | 14 | 30 | Ω |
| Discharge Threshold in Vcc | | | | 0.6 | | V |
| **SOFT START** | | | | | | |
| Soft Start Current | Iss | | | 20 | | μA |
| **OSCILLATOR** | | | | | | |
| Oscillator Frequency | Fsw | $R_{set}$ = 2K | 270 | 300 | 330 | KHz |
| Oscillator Frequency Accuracy | | | | | ±10 | % |
| **GATE DRIVER** | | | | | | |
| GH Pull−High Resistance (Note 2) | RH_GH | Source, V(BST−GH) = 0.1 | | 1.3 | 1.8 | Ω |
| GH Pull−Low Resistance (Note 2) | RL_GH | Sink, V(GH−SWN) = 0.1 V | | 1.1 | 1.6 | Ω |
| GL Pull−High Resistance (Note 2) | RH_GL | Source, V(VCC−GL) = 0.1 V | | 1.0 | 1.8 | Ω |
| GL Pull−Low Resistance (Note 2) | RL_GL | Sink, V(GL−PGND) = 0.1 V | | 0.5 | 0.9 | Ω |
| GH Source Current | | | | 2 | | A |
| GH Sink Current | | | | 2 | | A |
| GL Source Current | | | | 2 | | A |
| GL Sink Current | | | | 4 | | A |
| Dead Time | | GL off to GH on | 10 | 20 | 30 | ns |
| | | GH off to GL on | 10 | 20 | 30 | |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Threshold (Note 2) | | | | 150 | | °C |
| Thermal Shutdown Hysteresis (Note 2) | | | | 25 | | °C |

2. Guaranteed by characterization or correlation, not production tested

## DETAILED DESCRIPTION

### Overview

NCP5269B is designed for applications requiring dynamically selected slew−rate controlled output voltages. It provides a synchronous PWM controller that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. Forced CCM operation provides DDR termination voltage with source/sink capability It also provides fast transient response and excellent stability. The features of the NCP5269B include a 2 bits VID selectable and external programmable reference, fixed three preset switching frequency, an error amplifier, adaptive gate driver, programmable soft−start, and very low shutdown current. The protection features of the NCP5269B include over−current protection, power good monitor, over voltage and under voltage protection, built in output discharge and thermal shutdown.

### Reference Voltage Programming

The NCP5269B incorporates 2−bits VID, which selects four user−programmed reference voltages that reflect on Vref pin. NCP5269B measures VFB and VREF pin voltage relative to FBRTN pin. An internal reference that allows output voltages as low as 0.65 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents. The VID truth tables for each part are listed below.

**Table 4. NCP5269B VID TRUTH TABLE**

| VID STATE | | RESULTS | | |
|---|---|---|---|---|
| VID0 | VID1 | CLOSE | $V_{REF}$ | $V_{OUT}$ |
| 0 | 0 | SW3 | Vset3 | $V_{OUT4}$ |
| 0 | 1 | SW2 | Vset2 | $V_{OUT3}$ |
| 1 | 0 | SW1 | Vset1 | $V_{OUT2}$ |
| 1 | 1 | SW0 | Vset0 | $V_{OUT1}$ |

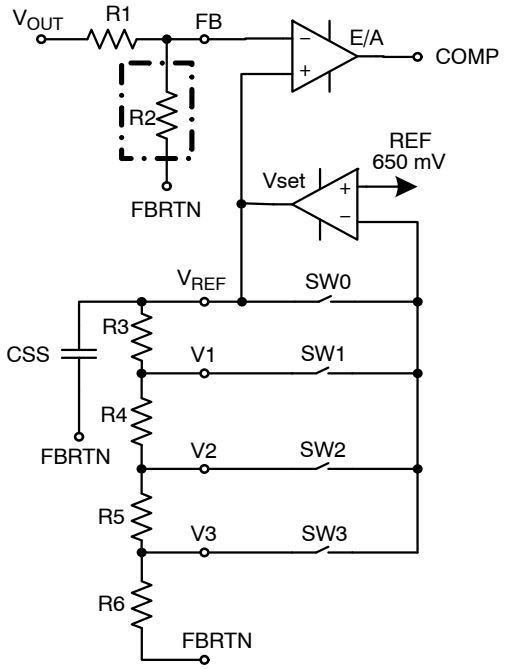



**Figure 3.**

### External Reference Voltage and Output Voltage Setting

Vset0, Vset1, Vset2 and Vset3 can be calculated based on the following equations:

$$V_{set0} = V_{INREF}$$

$$V_{set1} = V_{INREF} \cdot \left(1 + \frac{R_3}{R_4 + R_5 + R_6}\right)$$

$$V_{set2} = V_{INREF} \cdot \left(1 + \frac{R_3 + R_4}{R_5 + R_6}\right)$$

$$V_{set3} = V_{INREF} \cdot \left(1 + \frac{R_3 + R_4 + R_5}{R_6}\right)$$

And $V_{set3} > V_{set2} > V_{set1} > V_{set0}$

Vset0, Vset1, Vset2 and Vset3 are in the range of 0.65 V~1.5 V. If the required output voltage is higher than 0.65 V~1.5 V, a feedback voltage divider (a resistor R2 is added from FB pin to FBRTN) can be used to boost the output voltage up. So the output voltage can be calculated based on the following equations:

$$V_{OUT1} = V_{set0} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT2} = V_{set1} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT3} = V_{set2} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT4} = V_{set3} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

And $V_{OUT4} > V_{OUT3} > V_{OUT2} > V_{OUT1}$

### External Reference Voltage

NCP5269B accepts external reference voltage. To enable this feature, tie V3 to VCC and feed V1 from external reference. Then internal 650 mV reference is replaced by the voltage on V1 pin. The output voltage is programmed by resistor hooked from FB to FBRTN. VID0 and VID1 are disabled with this function. Please ground both VID0 and VID1 pins. All the resistors on Vref, V1, V2 and V3 are removed. The soft−start cap $C_{SS}$ remains on the Vref pin. The V2 pin can be left open.

The reference voltage on V1 pin can be from 0.5 V to 2.0 V. However, the NCP5269B does not provide soft−transient feature and PG blanking for any reference voltage jump on V1. Therefore, external slewrate control or R/C is recommended to soften the reference voltage change on V1 pin input. The initial reference voltage on V1 pin should be established prior to EN assertion.

### Differential Sensing of Output Voltage

The NCP5269B combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to provide accurate output voltage. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point. FBRTN should be connected directly to the negative remote sensing point.

### External Soft−Start and VID Change Slew Rate

To limit the start−up inrush current, a capacitor can be connected from Vref pin to ground to ramp up reference voltage slowly. During this period, the set amplifier output 20 μA current to charge capacitor $C_{SS}$. The soft start period can be calculated by the following equation:

$$t_{SS} = -R_A \cdot C_{SS} \cdot LN\left(1 - \frac{V_O}{I_{SA1} \cdot R_A}\right)$$

Where:

- RA is the sum of the series resistors from VREF to ground. $R_A = R_3 + R_4 + R_5 + R_6$
- $I_{SA1}$ is soft start current 20 μA.
- Vo is the initial output voltage set by VID

The output current of the set amplifier will change to +73 μA /− 90 μA after soft start period. So during voltage steps due to VID bit change, the slew rate of output voltage can be calculated as follows:

$$t_{SL} = -R_A \cdot C_{SS} \cdot LN\left(1 - \frac{V_{O2} - V_{O1}}{I_{SA2} \cdot R_A}\right)$$

Where:

- $I_{SA2}$ is the source/sink current limit of set amplifier during VID changing, which is 73/90 μA.
- VO1 and VO2 are the voltages selected by VID inputs

### Oscillator Frequency

A fixed precision oscillator is provided. The actual switching frequency is set at 300 KHz, 400 KHz or 600 KHz by the resistor on GL/FSET pin. The resistor and frequency can be referred to the table below.

| GL/FSET Resistor | 2K | 6K | 15K |
|---|---|---|---|
| Switching Frequency | 300 KHz | 400 KHz | 600 KHz |

### Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 15 MHz, with open loop gain of at least 80 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large−scale transient response.

### Soft Stop

Soft−Stop or discharge mode is always on during faults or disable. In this mode, a fault (UVP, OVP, OCP, TSD) or disable (EN) causes the output to be discharged through an internal 20−ohm transistor inside of VO terminal. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

### Adaptive Non−Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET free-wheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP5269B implements adaptive dead time control to minimize the dead time, as well as preventing shoot through from happening.

## PROTECTIONS

### Under Voltage Lockout (UVLO)

There is under-voltage lock out protections (UVLO) for VCC in NCP5269B, which has a typical trip threshold voltage 4.2 V and trip hysteresis 300 mV. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

### Over Voltage Protection (OVP)

When VFB voltage is 200 mV (typical) above $V_{REF}$ voltage for over 1.5 μs blanking time, an OV fault is set. At that moment, the top gate driver is turned off and the bottom gate driver is turned on trying to discharge the output. The bottom gate driver will be turned off when VFB drops below under voltage threshold. EN resets or power recycle the device can exit the fault. OVP is disabled during VID changes.

### Under Voltage Protection (UVP)

An UVP circuit monitors the VFB voltage to detect under voltage event. The under voltage limit is 300 mV (typical) below $V_{REF}$ voltage. If the VFB voltage is below this threshold over 3.3 μs, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault. UVP is delayed for soft start after EN goes high. UVP is disabled during VID changes.

### Power Good Monitor (PG)

NCP5269B provides window comparator to monitor the FB voltage. The target voltage window and transition delay times of the PGOOD comparator are ±5% (typ.) and 3.3−ms delay for assertion (low to high), and ±10% (typ) and 1.5−μs delay for de−assertion (high to low) during running. The PG pin is open drain 5−mA pull down output. During startup, PG stays low until the feedback voltage is within the specified range for about 3.3 ms. To prevent a false alarm; the power−good circuit is masked during any VID change. The duration of the PG mask is set to approximately 425 μs by an internal timer.

### Over Current Protection (OCP)

The NCP5269B protects converter if over−current occurs. The current through inductor is continuously monitored with differential current sense. Current limit threshold Vth_OC between CS+ and CS− is internally fixed to 30 mV. The current limit can be programmed by inductor's DCR and current sensing resistor divider with Rs1 and Rs2.

The Rs1, Rs2 and C can be calculated as:

$$C \cdot \left(R_{S1} // R_{S2}\right) = \frac{L}{DCR}$$

The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{th\_DC}}{k \cdot DCR}, \text{where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} - \frac{V_O \cdot \left(V_{in} - V_O\right)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$

where Vin is the input supply voltage of the power stage, and fsw is normal switching frequency.

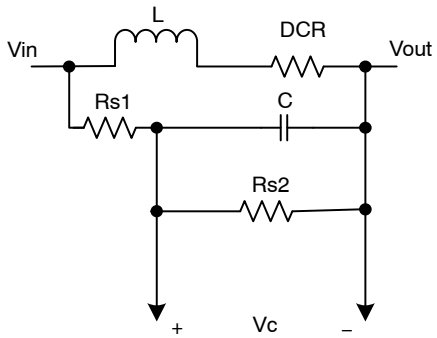



**Figure 4. Inductor DCR Current Sensing Circuit**

Figure 5 shows NTC resistor network to compensate the temperature drift of DCR.

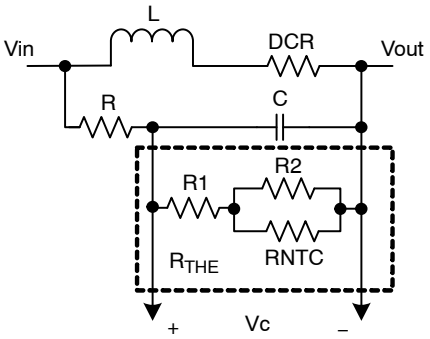



**Figure 5. Inductor DCR Current Sensing Circuit with Temperature Compensation Network**

If inductor current exceeds the current threshold, the high−side gate driver will be turned off cycle−by−cycle. In the mean time, an internal OC fault timer will be triggered. If the fault still exists after about 8 clock cycles, the part latches off, both the high−side MOSFET and the low−side MOSFET are turned off. The fault remains set until the system has shutdown and re−applied VCC and/or the enable signal EN is toggled.

### Pre−Bias Startup

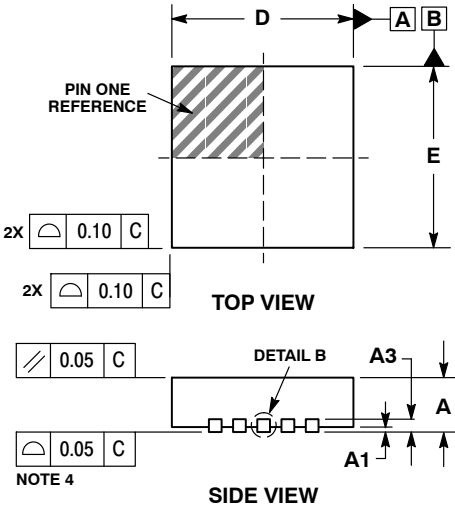
In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP5269B supports pre−bias start up by holding Low side FETs off till soft start ramp reaches the FB pin voltage.

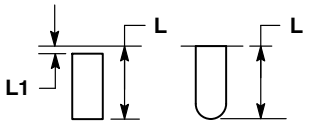
### Thermal Shutdown

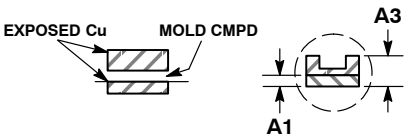
The NCP5269B protects itself from over heating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold, an internal resistor will discharge Vref and the voltage at the COMP pin will be pulled to GND, and both the upper and lower MOSFETs will be shut OFF. When temperature drops below threshold, the part will auto restart with soft− start feature.

## PACKAGE DIMENSIONS

**QFN20 3x3, 0.4P**
CASE 485BC
ISSUE O

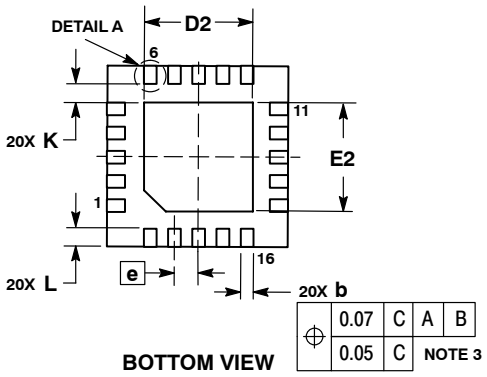


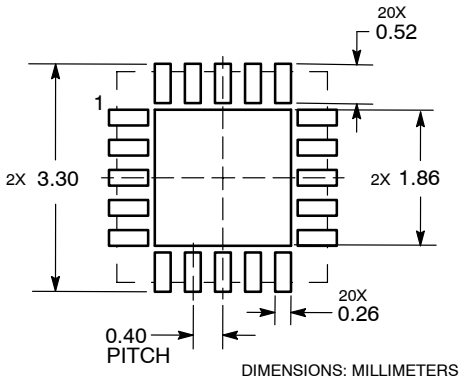




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 3.00 BSC | |
| D2 | 1.70 | 1.90 |
| E | 3.00 BSC | |
| E2 | 1.70 | 1.90 |
| e | 0.40 BSC | |
| K | 0.30 REF | |
| L | 0.20 | 0.40 |
| L1 | 0.00 | 0.15 |




**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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