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NCP58300

3.0A, Very Low-Dropout (VLDO) Fast Transient Response Regulator series

The NCP58300 series are high precision, very low dropout (VLDO), low ground current positive voltage regulators that are capable of providing an output current in excess of 3.0 A with a typical dropout voltage lower than 370 mV at 3.0 A load current. The devices are stable with tantalum output capacitors. This series consists initially of an Adjustable output voltage version, with fixed voltage versions planned in the future.

The NCP58300 series can withstand up to 18 V max input voltage. Internal protection features consist of output current limiting, built−in thermal shutdown and reverse output current protection. Logic level enable and error flag pins are available on the 5−pin version.

The NCP58302 is an Adjustable voltage Device and is offered in D2PAK−5 package.

Features

- Output Current in Excess of 3.0 A
- 370 mV Typical Dropout Voltage at 3.0 A
- Adjustable and Fixed Output Voltage Options
- Low Ground Current
- Fast Transient Response
- Stable with Tantalum Output Capacitor
- Logic Compatible Enable and Error Flag Pins
- Current Limit, Reverse Current and Thermal Shutdown Protection
- Operation up to 13.5 V Input Voltage
- Adjustable Device Output Voltage Range from 1.24 V to 12.9 V
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Consumer and Industrial Equipment Point of Regulation
- Servers and Networking Equipment
- FPGA, DSP and Logic Power supplies
- Switching Power Supply Post Regulation
- Battery Chargers
- Functional Replacement for Industry Standard MIC29300, MIC39300, MIC37300

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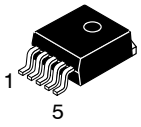
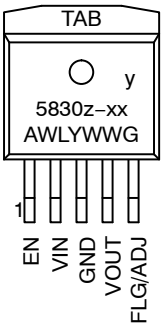
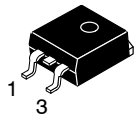
MARKING DIAGRAMS

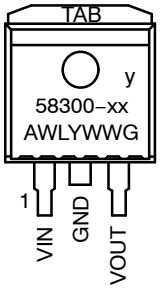


D²PAK
CASE 936A





D²PAK3
CASE 936



xx	= Voltage Version
y	= P (NCP), V (NCV)
z	= 1 (Fix Voltage), 2 (Adj)
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

TYPICAL APPLICATIONS

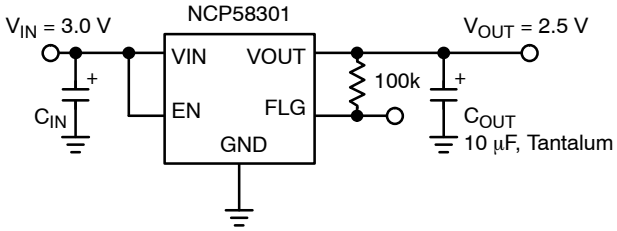


Figure 1. Fixed 2.5 Regulator with Error Flag

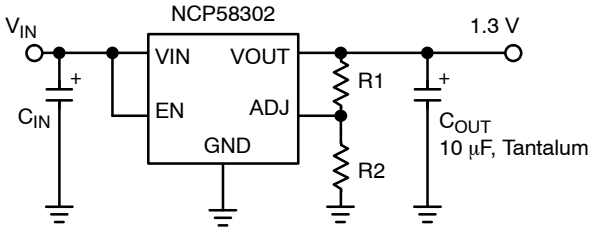


Figure 2. Adjustable Regulator

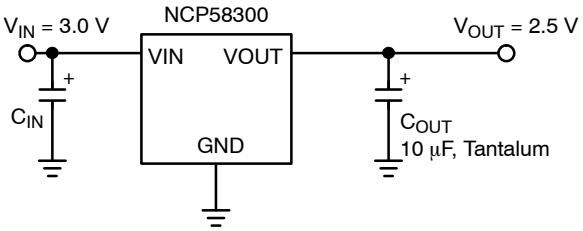


Figure 3. Fixed 2.5 Regulator in D^2PAK−3 Package

PIN FUNCTION DESCRIPTION

Pin Number D2PAK−5	Pin Number D2PAK−3	Pin Name	Pin Function
1	−	EN	Enable Input: CMOS and TTL logic compatible. Logic high = enable; Logic low = shutdown.
2	1	VIN	Input voltage which supplies both the internal circuitry and the current to the output load
3	2	GND	Ground
TAB	TAB	TAB	TAB is connected to ground.
4	3	VOUT	Linear Regulator Output.
5 (Fixed)	−	FLG	Error Flag Open collector output. Active−low indicates an output fault condition.
5 (Adj)	−	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{IN}	Supply Voltage	0 to 18	V
V_{EN}	Enable Input Voltage	0 to 18	V
V_{FLG}	Error Flag open collector output Max. voltage	0 to 18	V
$V_{OUT} - V_{IN}$	Reverse $V_{OUT} - V_{IN}$ Voltage (EN = Shutdown or V_{IN} = 0 V) (Note 1)	0 to 6.5	V
P_D	Power Dissipation (Notes 2 and 5)	Internally Limited	
T_J	Junction Temperature	$-40 \le T_J \le +125$	°C
T_S	Storage Temperature	$-65 \le T_J \le +150$	°C
	ESD Rating (Notes 3 and 4) Human Body Model Machine Model	2000 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: All voltages are referenced to GND pin unless otherwise noted.

1. The ENABLE pin input voltage must be ≤ 0.8 V or V_{IN} must be connected to ground potential.
2. $P_{D(max)} = (T_{J(max)} - T_A) / R_{\theta JA}$, where $R_{\theta JA}$ depends upon the printed circuit board layout.
3. Devices are ESD sensitive. Handling precautions recommended..
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model (HBM) tested per AEC – Q100 – 002 (EIA/JESD22 – A114C)
   ESD Machine Model (MM) tested per AEC – Q100 – 003 (EIA/JESD22 – A115C)
   This device contains latch – up protection and exceeds 100 mA per JEDEC Standard JESD78.
5. This protection is not guaranteed outside the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Rating	Value	Unit
V_{IN}	Maximum Supply Voltage	13.5	V
V_{EN}	Enable Input Voltage	0 to 13.5	V
V_{FLG}	Error Flag Open Collector Voltage	0 to 13.5	V
T_J	Junction Temperature	$-40 \le T_J \le +125$	°C

6. The device is not guaranteed to function outside it's Recommended operating conditions.

ELECTRICAL CHARACTERISTICS

T_J = 25°C with V_{IN} = $V_{OUT\ nominal}$ + 1 V; V_{EN} = V_{IN}; I_L = 10 mA; **bold** values indicate −40°C < T_J < +125°C, unless noted.

Parameter	Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy	I_L = 10 mA	−1		+1	%
	10 mA < I_{OUT} < 3.0 A , $V_{OUT\ nominal}$ + 1 ≤ V_{IN} ≤ 13.5 V	**−2**		**+2**	%
Output Voltage Line Regulation	V_{IN} = $V_{OUT\ nominal}$ + 1.0 V to 13.5 V; I_L = 10 mA		0.06	0.5	%
Output Voltage Load Regulation	I_L = 10 mA to 3.0 A , V_{IN} = $V_{OUT\ nominal}$ + 5.0 V		0.2	1	%
ΔVo / ΔT	Output Voltage Temperature Coefficient (Note 9)		**20**	**100**	ppm/°C
V_{IN} − V_{OUT} Dropout Voltage (Note 7)	I_L = 100 mA		80	**175**	mV
	I_L = 1.5 A		250		mV
	I_L = 3.0 A		370	**600**	mV
Ground Pin Current (Note 8)	I_L = 1.5 A, V_{IN} = $V_{OUT\ nominal}$ + 1.0 V		25	**50**	mA
	I_L = 3.0 A		50		mA
Ground Pin Current at Dropout	V_{IN} = V_{OUT} − 0.5V , I_L = 10 mA		1.7		mA
Ground Pin Current in Shutdown	V_{EN} ≤ 0.4 V		2.0	10 **30**	μA
Overload Protection Current Limit	V_{OUT} = 0 V, V_{IN} = $V_{OUT\ nominal}$ + 1.0 V		4.5		A
Output Noise Voltage (10 Hz to 100 kHz), I_L = 100 mA	C_{OUT} = 10 μF C_{OUT} = 33 μF		400 260		μV (rms)
FLAG OUTPUT					
Output Leakage Current $I_{flg(leak)}$	V_{oh} = 13.5 V		0.01	1 **2**	μA
Output Low Voltage $V_{FLG(LO)}$	Device set for 5 V, V_{IN} = 4.5 V, I_{FLG} = 250 μA		220	300 **400**	mV
Upper Threshold Voltage	Device set for 5 V (Note 11)	40 **25**	60		mV
Upper Threshold Voltage	Device set for 5 V (Note 11)		75	95 **140**	mV
Hysteresis	Device set for 5 V (Note 11)		15		mV
ENABLE INPUT					
Enable Input Signal Levels	Regulator enable	**2.4**			V
	Regulator shutdown			**0.8**	V
Enable pin Input Current	V_{EN} = 0.8 V			2 **4**	μA
	V_{EN} = 13.5 V		100	600 **750**	μA
Regulator Output Current in Shutdown	V_{EN} ≤ 0.8 V and V_{IN} ≤ 13.5 V, V_{OUT} = 0 V		10	**500**	μA

ELECTRICAL CHARACTERISTICS

T_J = 25°C with V_{IN} = $V_{OUT\ nominal}$ + 1 V; V_{EN} = V_{IN}; I_L = 10 mA; **bold** values indicate −40°C < T_J < +125°C, unless noted.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE NCP58302 ONLY					
Reference Voltage		1.228 **1.215**	1.240	1.252 **1.265**	V
Adjust Pin Bias Current			50	 **120**	nA
Reference Voltage Temperature Coefficient	(Note 10)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C

7. V_{DO} = V_{IN} − V_{OUT} when V_{OUT} decreases to 99% of its nominal output voltage with V_{IN} = V_{OUT} + 1 V.
8. I_{IN} = I_{GND} + I_{OUT}.
9. Output Voltage Temperature Coefficient is defined as worst case voltage change divided by the total temperature range. Guaranteed by design.
10. Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 4 W pulse for T = 10 ms.
11. Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5 V, the Error output is guaranteed to go low when the output drops by 95 mV x 5 V/1.240 V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.7% guaranteed.

Package	Conditions / PCB Footprint	Thermal Resistance
D2PAK−3, Junction−to−Case		$R_{\theta JC}$ = 2.0°C/W
D2PAK−5, Junction−to−Case		$R_{\theta JC}$ = 2.0°C/W

TYPICAL CHARACTERISTICS

T_J = 25°C if not otherwise noted

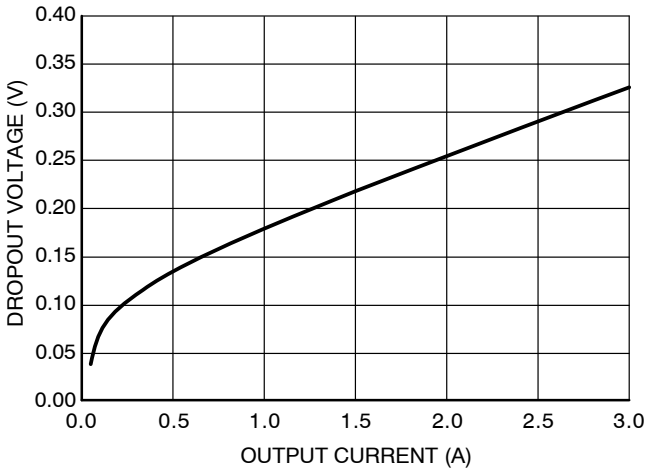


Figure 4. Dropout Voltage vs. Output Current

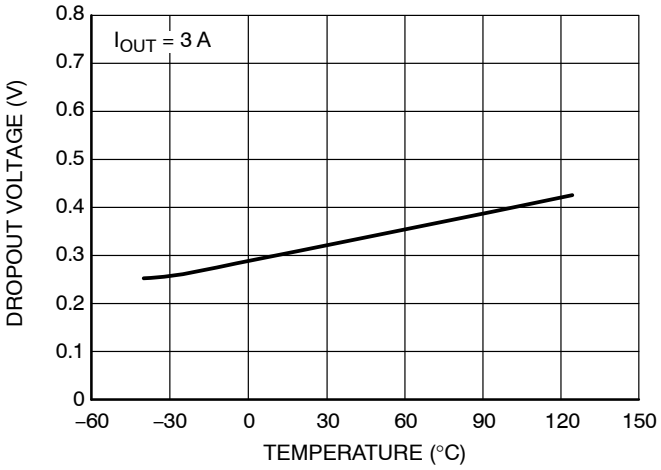


Figure 5. Dropout Voltage vs. Temperature

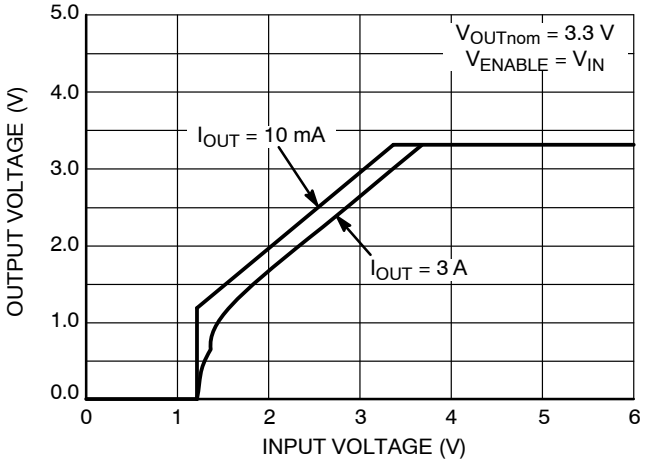


Figure 6. Dropout Characteristics

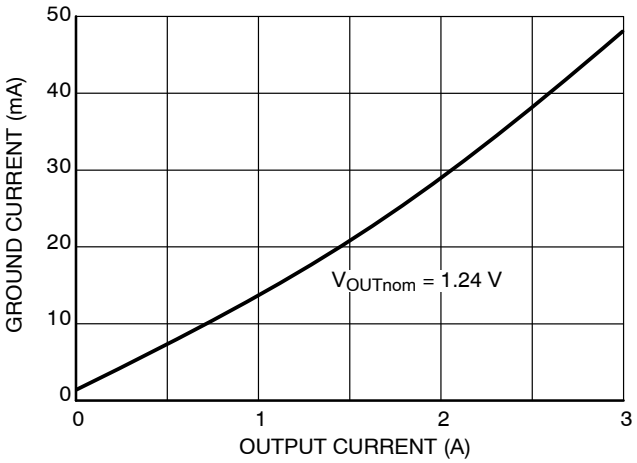


Figure 7. Ground Current vs. Output Current

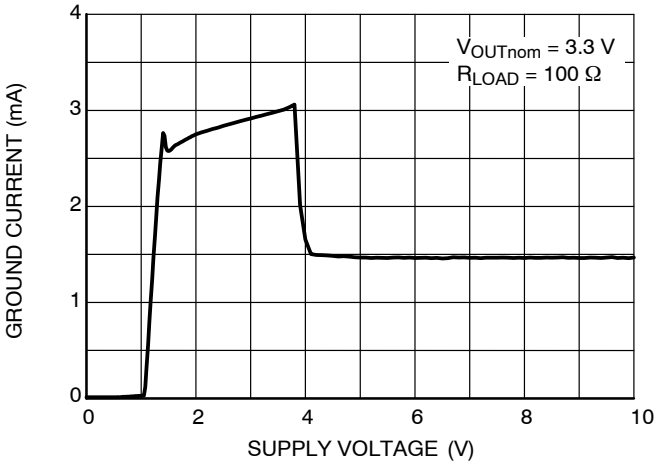


Figure 8. Ground Current vs. Supply Voltage

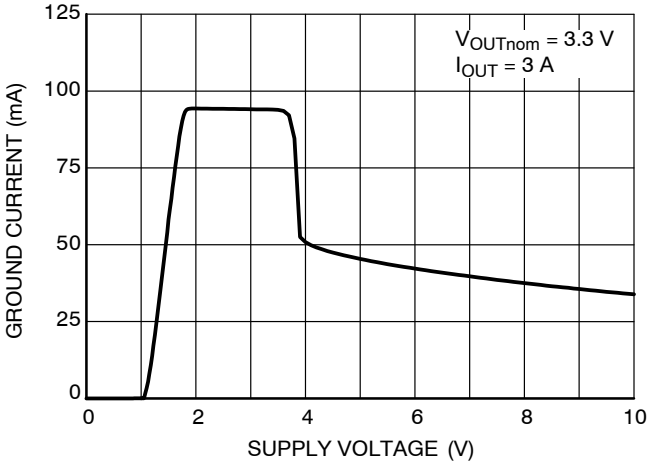


Figure 9. Ground Current vs. Supply Voltage

TYPICAL CHARACTERISTICS

T_J = 25°C if not otherwise noted

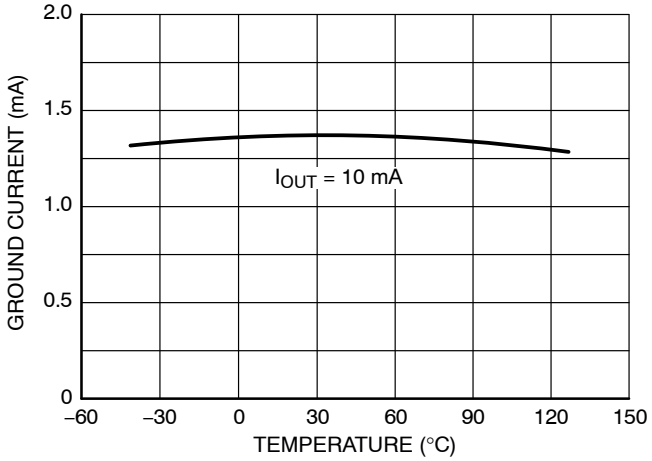


Figure 10. Ground Current vs. Temperature

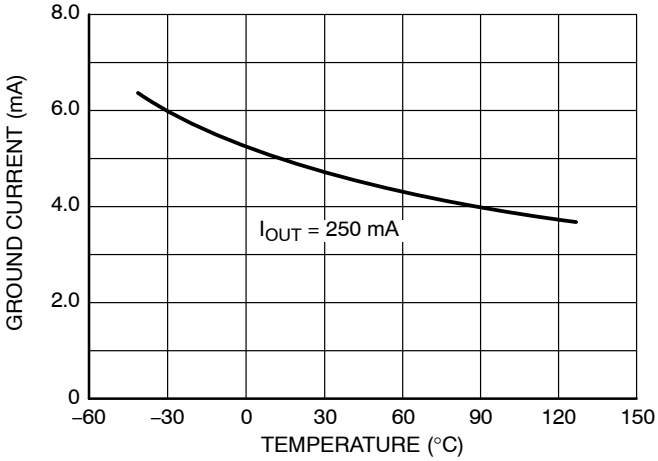


Figure 11. Ground Current vs. Temperature

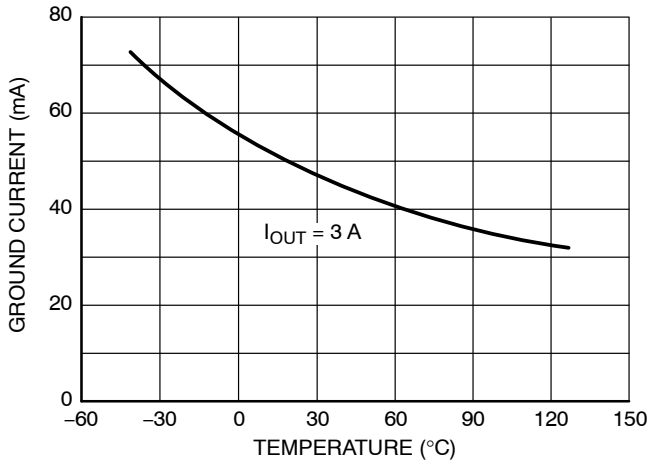


Figure 12. Ground Current vs. Temperature

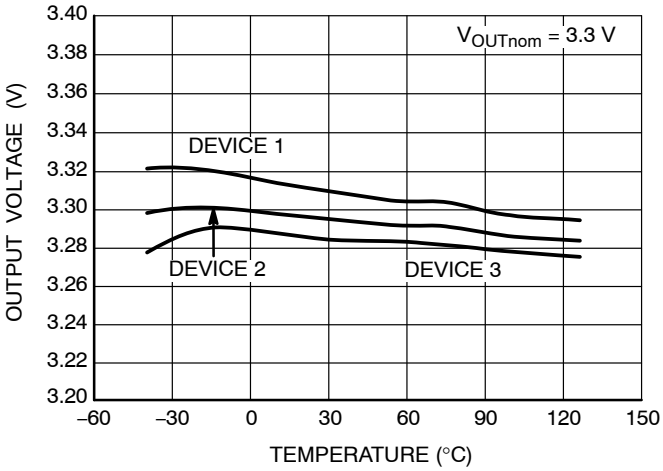


Figure 13. Output Voltage vs. Temperature

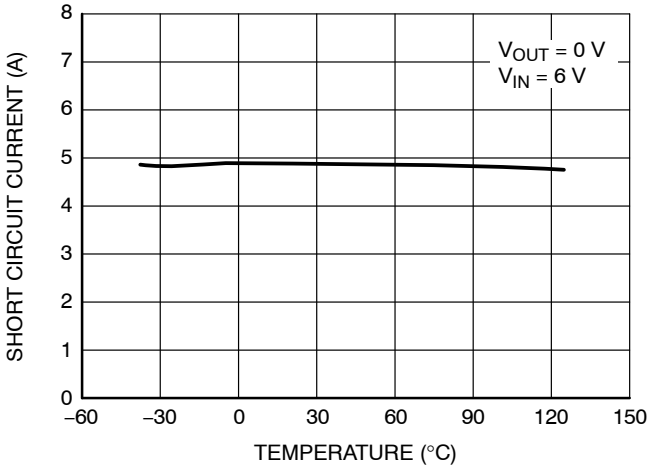


Figure 14. Short Circuit Current vs. Temperature

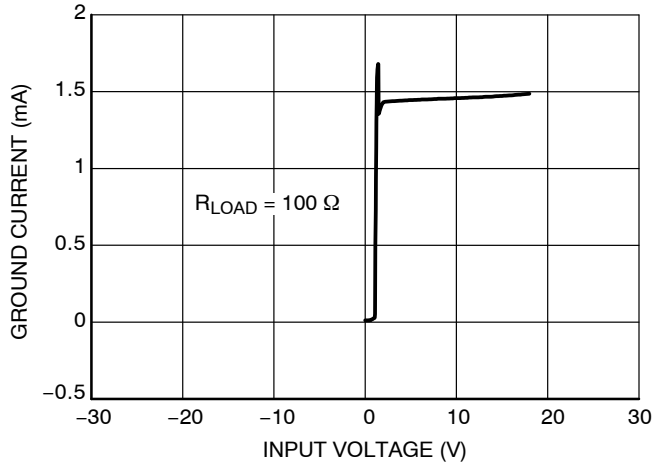


Figure 15. Ground Current vs. Input Voltage

TYPICAL CHARACTERISTICS

T_J = 25°C if not otherwise noted

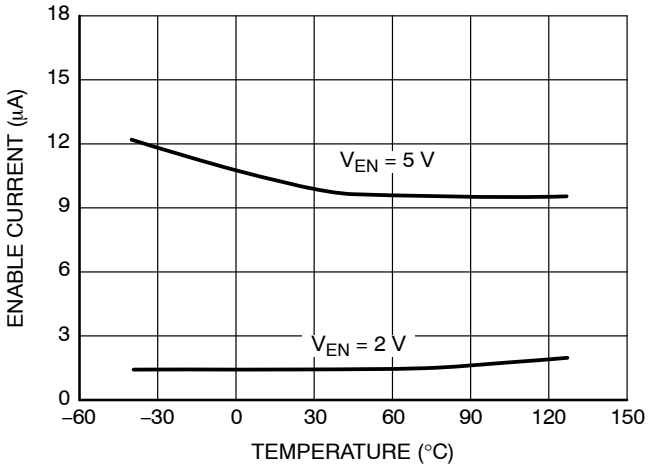


Figure 16. Enable Current vs. Temperature

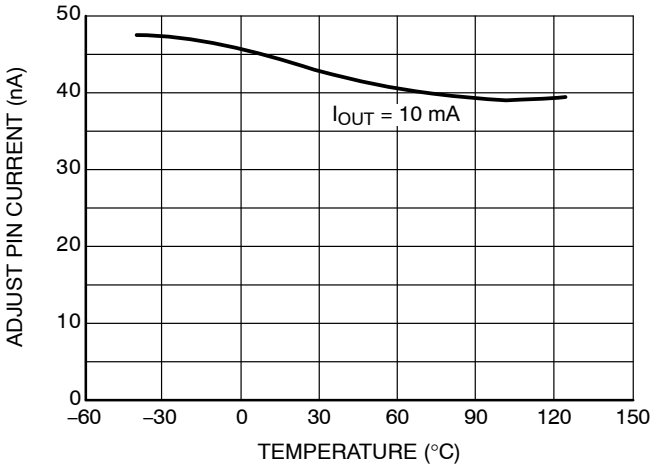


Figure 17. Adjust Pin Current vs. Temperature

APPLICATIONS INFORMATION

Output Capacitor and Stability

The NCP58300 series requires an output capacitor for stable operation. The NCP58300 series is designed to operate with tantalum output capacitors. The recommended output capacitance value is 10 μF or greater. Higher value helps to improve transient response and noise reduction. The value of output capacitor is dependent upon the output current; lower currents allow smaller capacitors.

Input Capacitor

An input capacitor of 0.1 μF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface−mount chip capacitors can be used for the bypassing. The capacitor should be place within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input of the regulator, further improving the integrity of the output voltage.

Minimum Load Current

The NCP58300 regulator is specified between finite loads. A 7 mA minimum load current is necessary for proper operation.

Error Flag

Some NCP58300 series members feature an error flag circuit that monitors the output voltage and signals an error condition when the voltage is 5% below the nominal output voltage. The error flag is an open−collector output that can sink up to 10 mA during a V_{OUT} fault condition. The FLG output is overload protected when a short circuit of the pullup load resistor occurs in the application. This is guaranteed in the full range of FLG output voltage Max ratings (see Max Ratings table).

Enable Input

Some NCP58300 series members also feature an enable input for on/off control of the device. It's shutdown state draws "zero" current from input voltage supply (only microamperes of leakage). The enable input is TTL/CMOS compatible for simple logic interface, but can be connected up to V_{IN}.

Overcurrent and Reverse Output Current Protection

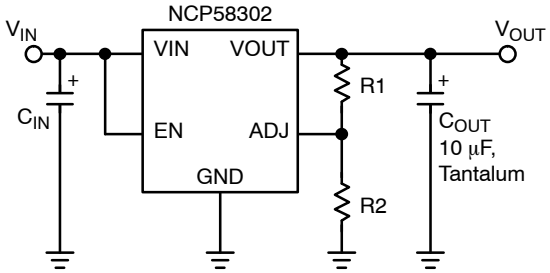
The NCP58300 regulator is fully protected from damage due to output current overload conditions. When NCP58300 output is overloaded, Output Current limiting is provided. This limiting is linear; output current during overload conditions is constant. The device is also capable to withstand power−on or enable start−up with output shorted to ground for the full Recommended Operating Conditions range. These features are advantageous for powering FPGAs and other ICs having current consumption higher than nominal during their startup.

Thermal shutdown disables the NCP58300 device when the die temperature exceeds the maximum safe operating temperature.

When NCP58300 is disabled and (V_{OUT} – V_{IN}) voltage difference is less than 6.5 V in the application, the output structure of these regulators is able to withstand output voltage (backup battery as example) to be applied without reverse current flow. Of course the additional current flowing through the internal Feedback resistor divider at the NCP58300 Fix voltage versions needs to be included in the backup battery discharging calculations.

Adjustable Voltage Design

The NCP/NCV58302 Adjustable voltage Device Output voltage is set by the ratio of two external resistors as shown in Figure 18.The device maintains the voltage at the ADJ pin at 1.24 V referenced to ground. The current in R2 is then equal to1.24 V / R2, and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current flows from VOUT through R1 into the ADJ pin.



$$V_{OUT} = 1.24\ V \cdot \left(1 + \frac{R1}{R2}\right) + I_{ADJ} \cdot R1$$

Figure 18. Adjustable Voltage Operation

For the R2 resistor value up to 15 kΩ the I_{ADJ} current impact can be neglected and the R1 resistor value can be calculated y:

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.24} - 1\right) \quad \text{(eq. 1)}$$

Where V_{OUT} is the desired nominal output voltage.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The P_D total power dissipated by the device has two components, Input to output voltage differential multiplied by Output current and Input voltage multiplied by GND pin current.

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} + V_{IN} \cdot I_{GND} \quad \text{(eq. 2)}$$

The GND pin current value can be found in Electrical Characteristics table and in Typical Characteristics graphs.

The Junction temperature T_J is

$$T_J = T_A + P_D \cdot R_{\theta JA} \quad \text{(eq. 3)}$$

where T_A is ambient temperature and $R_{\theta JA}$ is the Junction to Ambient Thermal Resistance of the NCP/NCV58300 device mounted on the specific PCB.

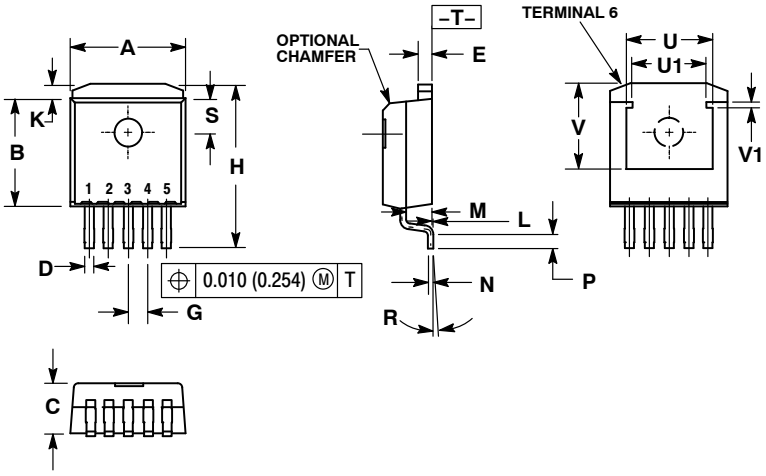
ORDERING INFORMATION

Device	Output Current	Output Voltage	Junction Temp. Range	Package	Shipping†
NCP58302DSADJR4G	3.0 A	ADJ	−40°C to +125°C	D^2PAK−5 (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

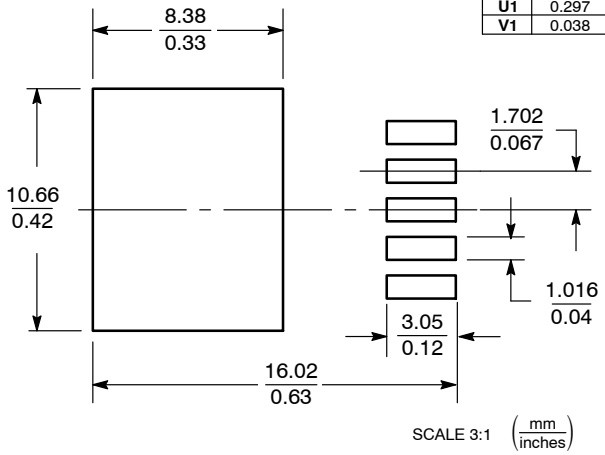
D²PAK 5
CASE 936A−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5 ° REF		5 ° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	
U1	0.297	0.305	7.544	7.747
V1	0.038	0.046	0.965	1.168

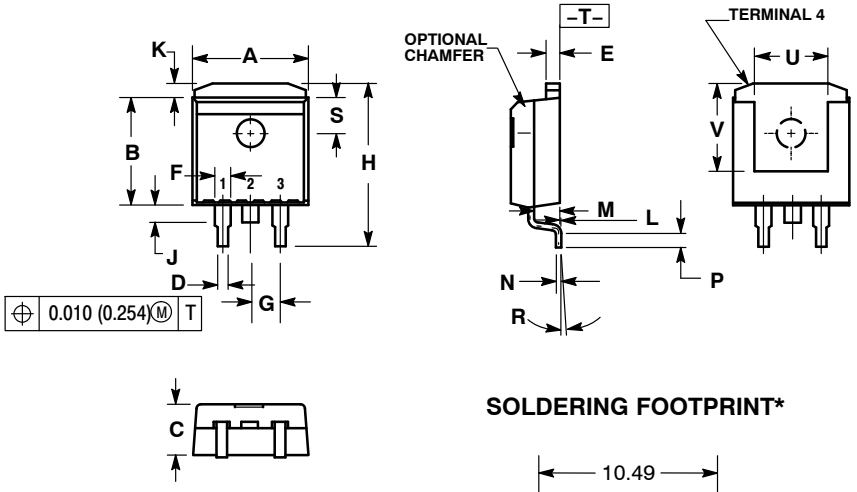
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

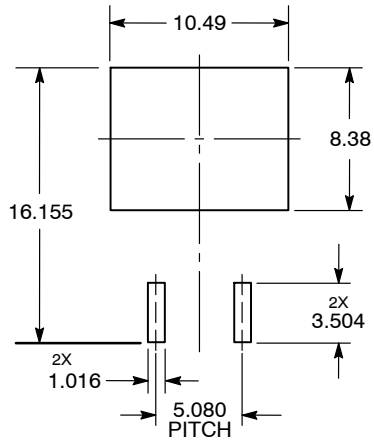
D²PAK
CASE 936−03
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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