# Ultra-Low Iq 150 mA CMOS LDO Regulator with Enable

The NCP583 series of low dropout regulators are designed for portable battery powered applications which require precise output voltage accuracy and low quiescent current. These devices feature an enable function which lowers current consumption significantly and are offered in two small packages; SC–82AB and the SOT–563.

A 1.0  $\mu$ F ceramic capacitor is the recommended value to be used with these devices on the output pin.

# Features

- Ultra-Low Dropout Voltage of 250 mV at 150 mA
- Excellent Line Regulation of 0.05%/V
- Excellent Load Regulation of 20 mV
- High Output Voltage Accuracy of  $\pm 2\%$
- Ultra–Low Iq Current of 1.0 µA
- Very Low Shutdown Current of 0.1 µA
- Wide Output Voltage Range of 1.5 V to 3.3 V
- Low Temperature Drift Coefficient on the Output Voltage of  $\pm 100 \text{ ppm/}^{\circ}\text{C}$
- Fold Back Protection Circuit
- Input Voltage up to 6.5 V
- These are Pb–Free Devices

# **Typical Applications**

- Portable Equipment
- Hand-Held Instrumentation
- Camcorders and Cameras



Figure 1. Simplified Block Diagram



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## MARKING DIAGRAMS





X = Device Code

T = Traceability Information

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Semiconductor Components Industries, LLC, 2016 January, 2016 – Rev. 15 1

# PIN FUNCTION DESCRIPTION

SOT-563 Pin	SC-82AB Pin	Symbol	Description
1	4	V <sub>in</sub>	Power supply input voltage.
2	2	GND	Power supply ground.
3	3	Vout	Regulated output voltage.
4	-	NC	No connect.
5	-	GND	Power supply ground.
6	1	CE	Chip enable pin.

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V <sub>in</sub>	6.5	V
Input Voltage (CE Pin)	V <sub>CE</sub>	6.5	V
Output Voltage	V <sub>out</sub>	–0.3 to V <sub>in</sub> +0.3	V
Output Current	l <sub>out</sub>	180	mA
Thermal Junction Resistance SC–82AB SOT–563	R <sub>θJA</sub>	263 200	°C/W
ESD Capability, Human Body Model, C = 100 pF, R = 1.5 k $\Omega$	ESD <sub>HBM</sub>	2000	V
ESD Capability, Machine Model, C = 200 pF, R = 0 $\Omega$	ESD <sub>MM</sub>	200	V
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to +85	°C
Maximum Junction Temperature	T <sub>J(max)</sub>	125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **ELECTRICAL CHARACTERISTICS** ( $V_{in} = V_{out} + 1.0 V$ , $T_A = -40^{\circ}C$ to +85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Input Voltage	V <sub>in</sub>	1.7	-	6.0	V
Output Voltage (1.0 $\mu$ A $\leq$ I <sub>out</sub> $\leq$ 30 mA)	Vout	V <sub>out</sub> x 0.98	_	V <sub>out</sub> x 1.02	V
Line Regulation ( $I_{out}$ = 30 mA) ( $V_{out}$ + 0.5 V $\leq$ Vin $\leq$ 6.0 V)	Reg <sub>line</sub>	_	0.05	0.20	%/V
Load Regulation (1.0 $\mu$ A $\leq$ I <sub>out</sub> $\leq$ 150 mA)	Reg <sub>load</sub>	-	20	40	mV
$ \begin{array}{l} \text{Dropout Voltage (I_{out} = 150 \text{ mA})} \\ \text{V}_{out} = 1.5 \text{ V} \\ 1.7 \text{ V} \leq \text{V}_{out} \leq 1.9 \text{ V} \\ 2.1 \text{ V} \leq \text{V}_{out} \leq 2.7 \text{ V} \\ 2.8 \text{ V} \leq \text{V}_{out} \leq 3.3 \text{ V} \end{array} $	V <sub>DO</sub>	- - - -	0.60 0.50 0.35 0.25	0.90 0.75 0.55 0.40	V
Quiescent Current (I <sub>out</sub> = 0 mA)	lq	-	1.0	1.5	μΑ
Output Current	I <sub>out</sub>	150	-	-	mA
Shutdown Current (V <sub>CE</sub> = Gnd)	I <sub>SD</sub>	-	0.1	1.0	μΑ
Output Short Circuit Current (V <sub>out</sub> = 0)	l <sub>lim</sub>	-	40	-	mA
Enable Input Threshold Voltage – High – Low	Vth <sub>enh</sub> Vth <sub>enl</sub>	1.2 0	-	6.0 0.3	V
Output Voltage Temperature Coefficient ( $I_{out} = 30 \text{ mA}, -40^{\circ}\text{C} \le T_A \le 85^{\circ}\text{C}$ )	$\Delta V_{out}/\Delta T$	-	±100	-	ppm/°C

# TYPICAL CHARACTERISTICS



# **TYPICAL CHARACTERISTICS**



Figure 8. Dropout Voltage vs. Output Current







Figure 10. Dropout Voltage vs. Output Current



Figure 11. Ripple Rejection vs. Frequency











# **TYPICAL CHARACTERISTICS**



 $(V_{out} = 2.8 \text{ V}, \text{ tr} = \text{tf} = 5.0 \ \mu\text{s}, V_{in} = 3.8 \text{ V})$ 





# **APPLICATION INFORMATION**

## Input Decoupling

A 1.0  $\mu F$  ceramic capacitor is the recommended value to be connected between  $V_{in}$  and GND. For PCB layout considerations, the traces of  $V_{in}$  and GND should be sufficiently wide in order to minimize noise and prevent unstable operation.

## **Output Decoupling** It is recommended to use a 0.1 $\mu$ F ceramic capacitor on the V<sub>out</sub> pin. For better performance, select a capacitor with low Equivalent Series Resistance (ESR). For PCB layout considerations, place the output capacitor close to the output pin and keep the leads short as possible.

#### **ORDERING INFORMATION**

Device	Output Type / Features	Nominal Output Voltage	Marking	Package	Shipping <del> </del>
NCP583SQ15T1G	Active High w/Enable	1.5	A5	SC-82AB (Pb-Free)	3000 / Tape & Reel
NCP583SQ18T1G	Active High w/Enable	1.8	A8	SC-82AB (Pb-Free)	3000 / Tape & Reel
NCP583SQ25T1G	Active High w/Enable	2.5	B5	SC-82AB (Pb-Free)	3000 / Tape & Reel
NCP583SQ27T1G	Active High w/Enable	2.7	B7	SC–82AB (Pb–Free)	3000 / Tape & Reel
NCP583SQ28T1G	Active High w/Enable	2.8	B8	SC–82AB (Pb–Free)	3000 / Tape & Reel
NCP583SQ30T1G	Active High w/Enable	3.0	C0	SC–82AB (Pb–Free)	3000 / Tape & Reel
NCP583SQ33T1G	Active High w/Enable	3.3	C3	SC–82AB (Pb–Free)	3000 / Tape & Reel
NCP583XV15T2G	Active High w/Enable	1.5	G15B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV18T2G	Active High w/Enable	1.8	G18B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV25T2G	Active High w/Enable	2.5	G25B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV26T2G	Active High w/Enable	2.6	G26B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV28T2G	Active High w/Enable	2.8	G28B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV29T2G	Active High w/Enable	2.9	G29B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV30T2G	Active High w/Enable	3.0	G30B	SOT–563 (Pb–Free)	4000 / Tape & Reel
NCP583XV31T2G	Active High w/Enable	3.1	G31B	SOT-563 (Pb-Free)	4000 / Tape & Reel
NCP583XV33T2G	Active High w/Enable	3.3	G33B	SOT–563 (Pb–Free)	4000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Other voltages are available. Consult your ON Semiconductor representative.

DATE 22 JUN 2012





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SC-82AB CASE 419C-02 **ISSUE F** 

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- NOTES:
  DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  CONTROLLING DIMENSION: MILLIMETER.
  419C-01 OBSOLETE. NEW STANDARD IS 419C-02.
  DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURDS BURRS.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	1.80	2.20	0.071	0.087	
В	1.15	1.35	0.045	0.053	
С	0.80	1.10	0.031	0.043	
D	0.20	0.40	0.008	0.016	
F	0.30	0.50	0.012	0.020	
G	1.10	1.50	0.043	0.059	
н	0.00	0.10	0.000	0.004	
J	0.10	0.26	0.004	0.010	
K	0.10		0.004		
L	0.05	BSC	0.002	BSC	
N	0.20	REF	0.008	B REF	
S	1.80	2.40	0.07	0.09	

#### GENERIC **MARKING DIAGRAM\***



XXX = Specific Device Code Μ = Month Code

= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ", may or may not be present.

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MILLIMETERS

NDM.

0.55

0.22

0.13

1.60

1.20

0.50 BSC

0.20

1.60

MAX.

0.60

0.27

0.18

1.70

1.30

0.30

1.70

SIDE VIEW

MIN.

0.50

0.17

0.08

1.50

1.10

0.10

1.50





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DATE 26 JAN 2021

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NDTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.

А

DIM

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- 1. DIMENSIONING AND TOLERANCING PER A 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS DF BASE MATERIAL.



RECOMMENDED MOUNTING FOOTPRINT\* \* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

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STYL PIN	E 4: 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 5: PIN 1. CATHIDE 2. CATHIDE 3. ANIDE 4. ANIDE 5. CATHIDE 6. CATHIDE	STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYL PIN	E 7: 1. CATHEDE 2. ANEDE 3. CATHEDE 4. CATHEDE 5. ANEDE 6. CATHEDE	STYLE 8: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SDURCE 5. DRAIN 6. DRAIN	STYLE 9: PIN 1. SDURCE 1 2. GATE 1 3. DRAIN 2 4. SDURCE 2 5. GATE 2 6. DRAIN 1
STYL PIN	E 10: 1. CATHEDE 1 2. N/C 3. CATHEDE 2 4. ANEDE 2 5. N/C	STYLE 11: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1	

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## GENERIC **MARKING DIAGRAM\***

XX M=

XX = Specific Device Code

M = Month Code

. = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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