

NCP583

Ultra-Low Iq 150 mA CMOS LDO Regulator with Enable

The NCP583 series of low dropout regulators are designed for portable battery powered applications which require precise output voltage accuracy and low quiescent current. These devices feature an enable function which lowers current consumption significantly and are offered in two small packages; SC-82AB and the SOT-563.

A 1.0 μ F ceramic capacitor is the recommended value to be used with these devices on the output pin.

Features

- Ultra-Low Dropout Voltage of 250 mV at 150 mA
- Excellent Line Regulation of 0.05%/V
- Excellent Load Regulation of 20 mV
- High Output Voltage Accuracy of $\pm 2\%$
- Ultra-Low Iq Current of 1.0 μ A
- Very Low Shutdown Current of 0.1 μ A
- Wide Output Voltage Range of 1.5 V to 3.3 V
- Low Temperature Drift Coefficient on the Output Voltage of ± 100 ppm/ $^{\circ}$ C
- Fold Back Protection Circuit
- Input Voltage up to 6.5 V
- These are Pb-Free Devices

Typical Applications

- Portable Equipment
- Hand-Held Instrumentation
- Camcorders and Cameras

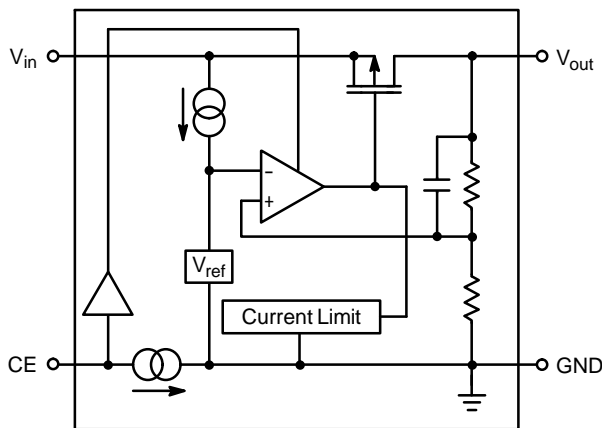


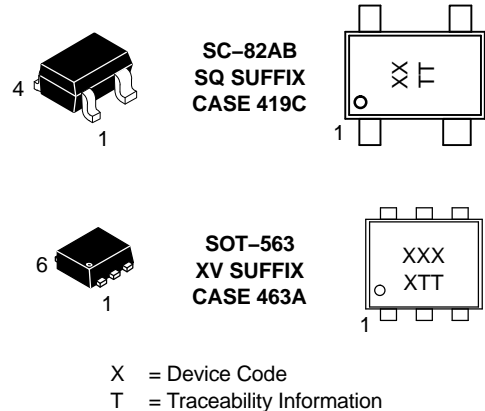
Figure 1. Simplified Block Diagram



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MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NCP583

PIN FUNCTION DESCRIPTION

| SOT-563 Pin | SC-82AB Pin | Symbol | Description |
|-------------|-------------|-----------|-----------------------------|
| 1 | 4 | V_{in} | Power supply input voltage. |
| 2 | 2 | GND | Power supply ground. |
| 3 | 3 | V_{out} | Regulated output voltage. |
| 4 | – | NC | No connect. |
| 5 | – | GND | Power supply ground. |
| 6 | 1 | CE | Chip enable pin. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------------|------------------------|------|
| Input Voltage | V_{in} | 6.5 | V |
| Input Voltage (CE Pin) | V_{CE} | 6.5 | V |
| Output Voltage | V_{out} | -0.3 to $V_{in} + 0.3$ | V |
| Output Current | I_{out} | 180 | mA |
| Thermal Junction Resistance SC-82AB SOT-563 | $R_{\theta JA}$ | 263 200 | °C/W |
| ESD Capability, Human Body Model, C = 100 pF, R = 1.5 k Ω | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model, C = 200 pF, R = 0 Ω | ESD_{MM} | 200 | V |
| Operating Ambient Temperature Range | T_A | -40 to +85 | °C |
| Maximum Junction Temperature | $T_{J(max)}$ | 125 | °C |
| Storage Temperature Range | T_{stg} | -55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS ($V_{in} = V_{out} + 1.0$ V, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------------|-----------------------|------------------------------|------------------------------|---------------|
| Input Voltage | V_{in} | 1.7 | – | 6.0 | V |
| Output Voltage ($1.0 \mu\text{A} \leq I_{out} \leq 30$ mA) | V_{out} | $V_{out} \times 0.98$ | – | $V_{out} \times 1.02$ | V |
| Line Regulation ($I_{out} = 30$ mA) ($V_{out} + 0.5$ V $\leq V_{in} \leq 6.0$ V) | Reg_{line} | – | 0.05 | 0.20 | %/V |
| Load Regulation ($1.0 \mu\text{A} \leq I_{out} \leq 150$ mA) | Reg_{load} | – | 20 | 40 | mV |
| Dropout Voltage ($I_{out} = 150$ mA) $V_{out} = 1.5$ V 1.7 V $\leq V_{out} \leq 1.9$ V 2.1 V $\leq V_{out} \leq 2.7$ V 2.8 V $\leq V_{out} \leq 3.3$ V | V_{DO} | – | 0.60 0.50 0.35 0.25 | 0.90 0.75 0.55 0.40 | V |
| Quiescent Current ($I_{out} = 0$ mA) | I_q | – | 1.0 | 1.5 | μA |
| Output Current | I_{out} | 150 | – | – | mA |
| Shutdown Current ($V_{CE} = \text{Gnd}$) | I_{SD} | – | 0.1 | 1.0 | μA |
| Output Short Circuit Current ($V_{out} = 0$) | I_{lim} | – | 40 | – | mA |
| Enable Input Threshold Voltage – High – Low | $V_{th_{enh}}$ $V_{th_{enl}}$ | 1.2 0 | – – | 6.0 0.3 | V |
| Output Voltage Temperature Coefficient ($I_{out} = 30$ mA, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$) | $\Delta V_{out}/\Delta T$ | – | ± 100 | – | ppm/°C |

TYPICAL CHARACTERISTICS

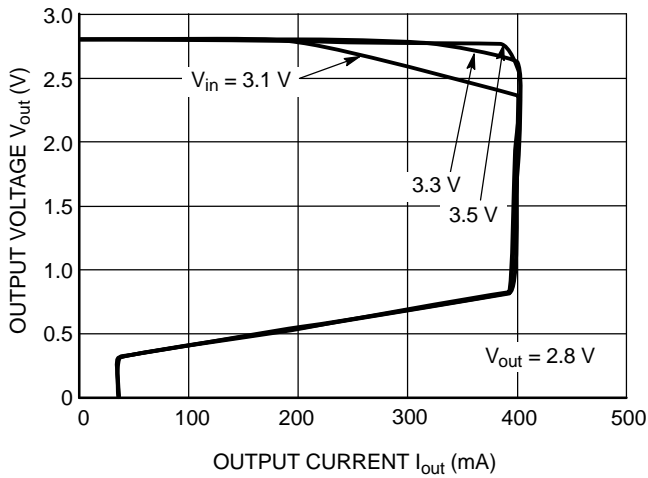


Figure 2. Output Voltage vs. Output Current

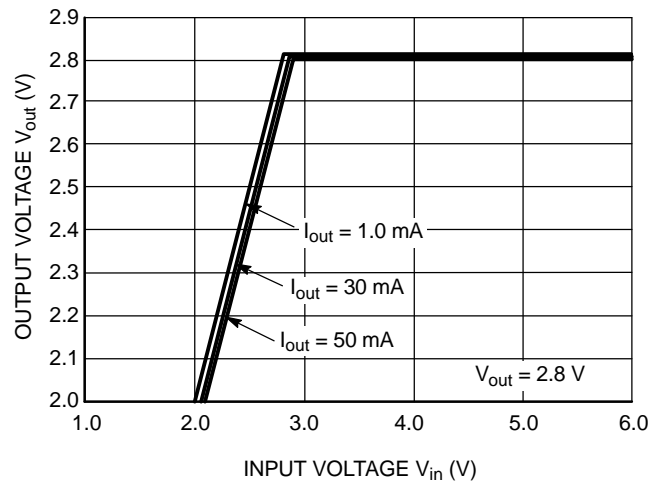


Figure 3. Output Voltage vs. Input Voltage

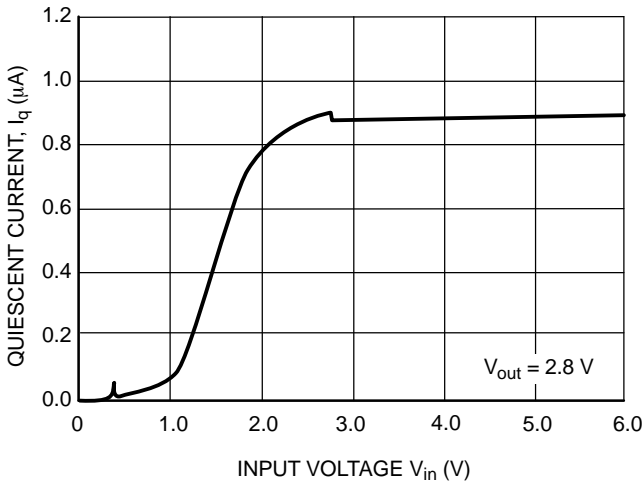


Figure 4. Quiescent Current vs. Input Voltage

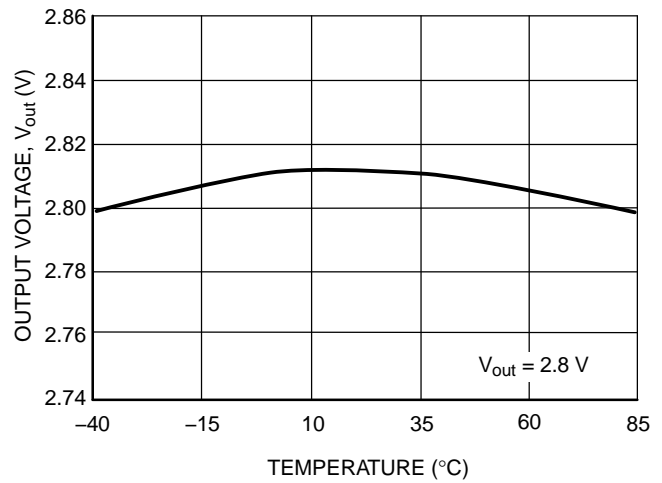


Figure 5. Output Voltage vs. Temperature

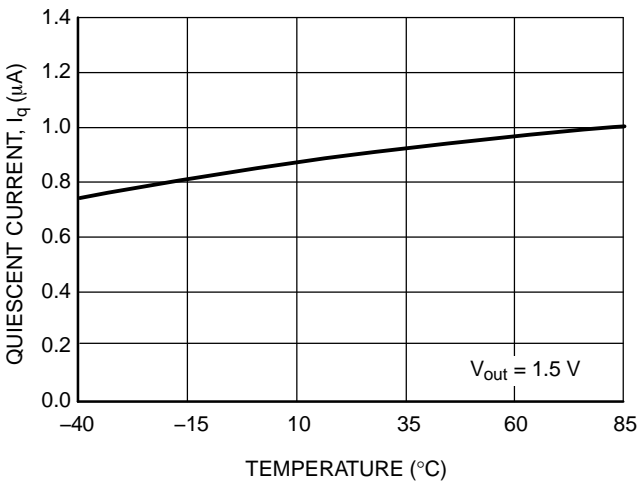


Figure 6. Quiescent Current vs. Temperature

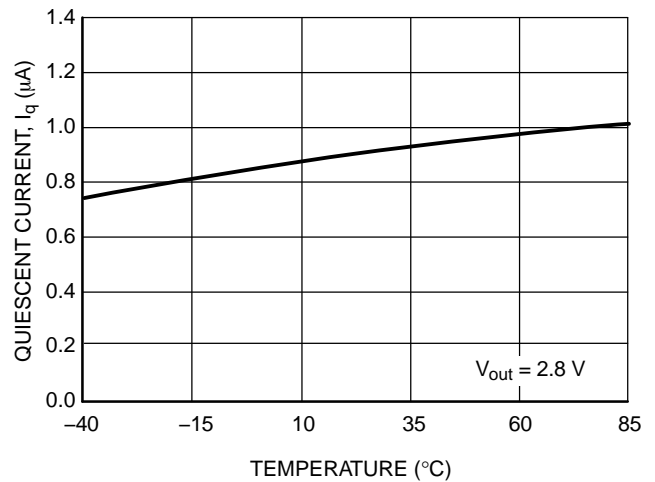


Figure 7. Quiescent Current vs. Temperature

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TYPICAL CHARACTERISTICS

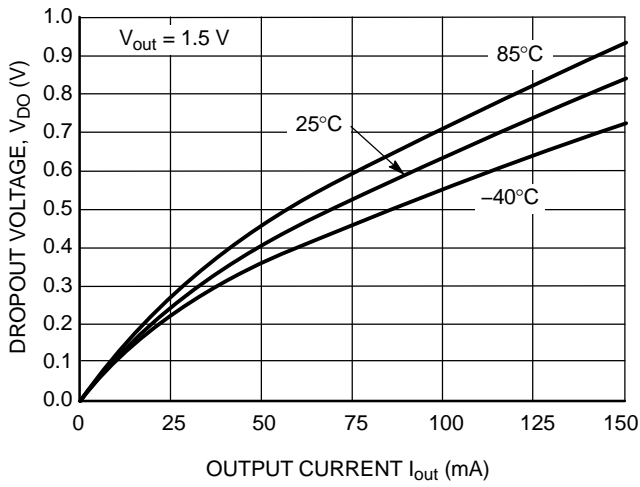


Figure 8. Dropout Voltage vs. Output Current

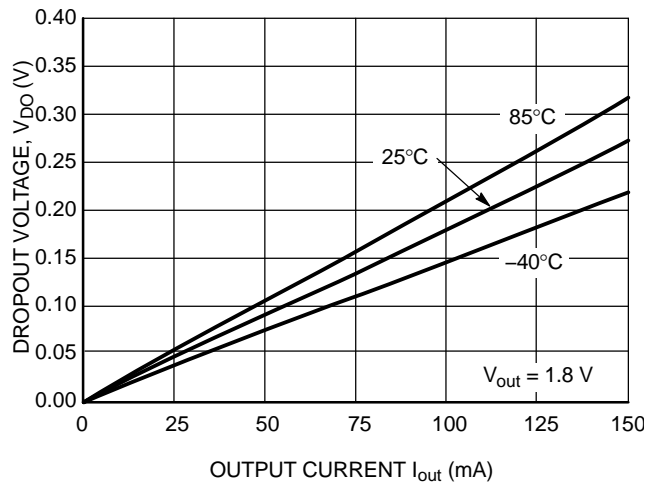


Figure 9. Dropout Voltage vs. Output Current

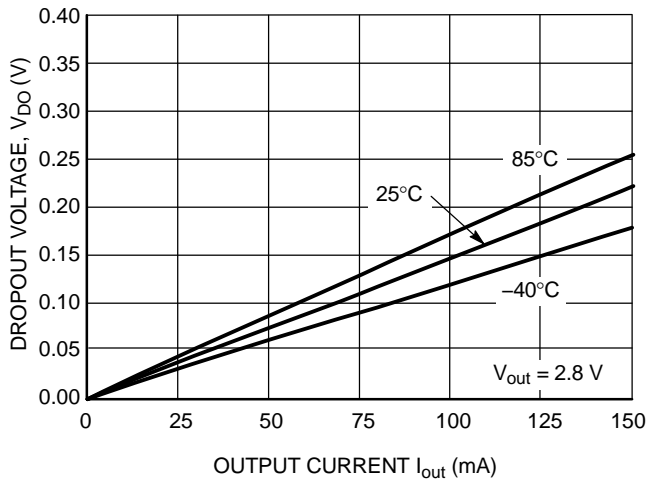


Figure 10. Dropout Voltage vs. Output Current

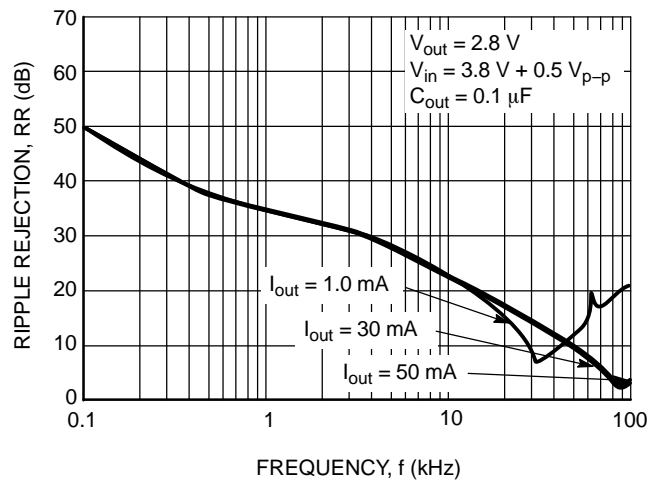


Figure 11. Ripple Rejection vs. Frequency

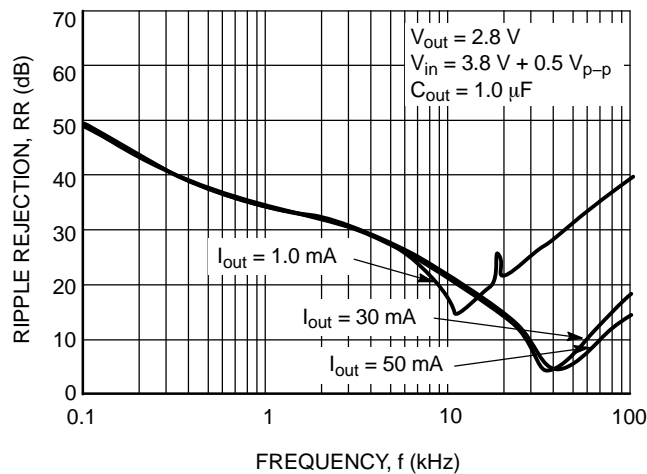


Figure 12. Ripple Rejection vs. Frequency

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TYPICAL CHARACTERISTICS

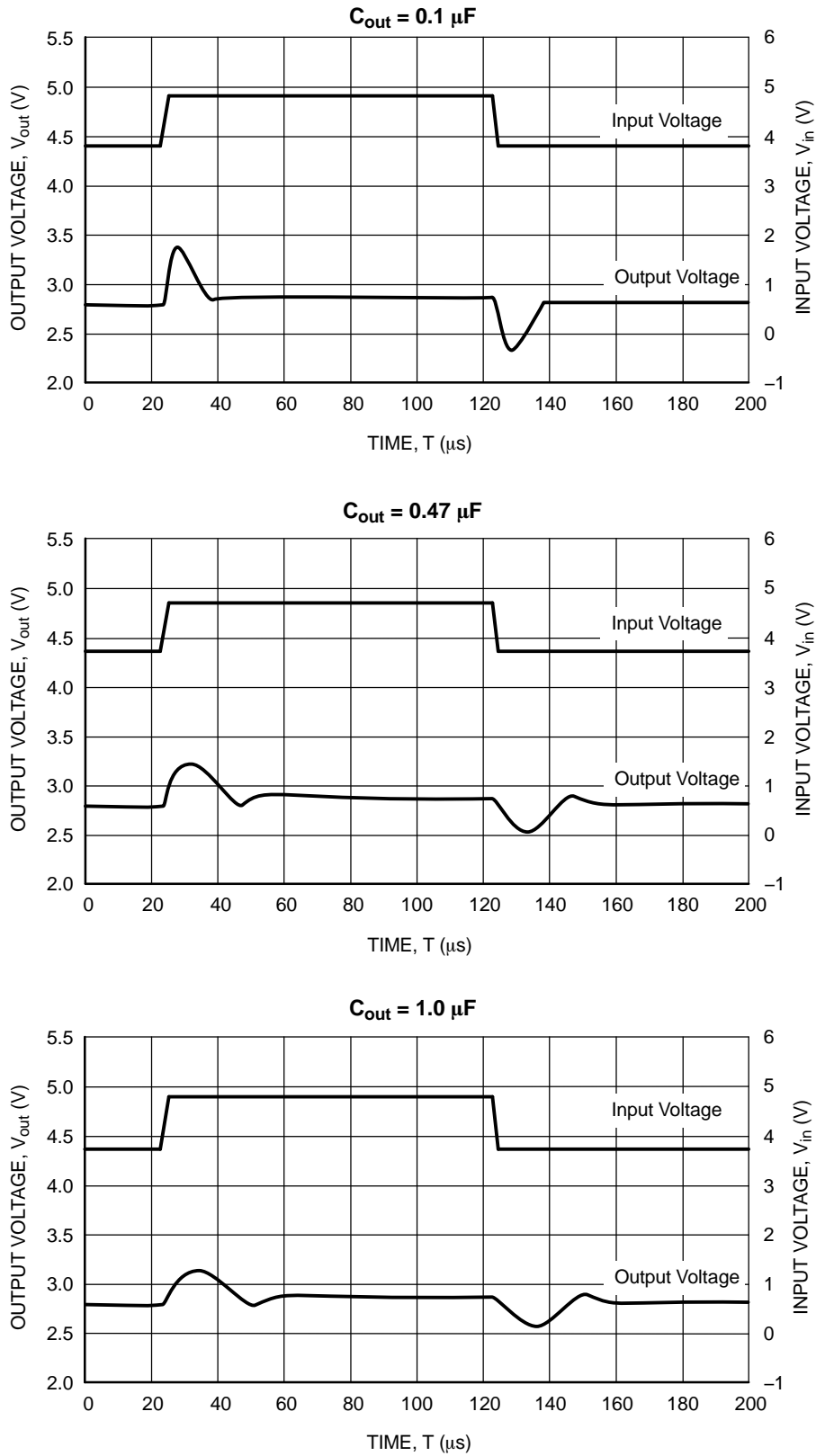


Figure 13. Input Transient Response
($V_{out} = 2.8 V$, $I_{out} = 30 mA$, $t_r = t_f = 5.0 \mu s$, $C_{in} = 0$)

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TYPICAL CHARACTERISTICS

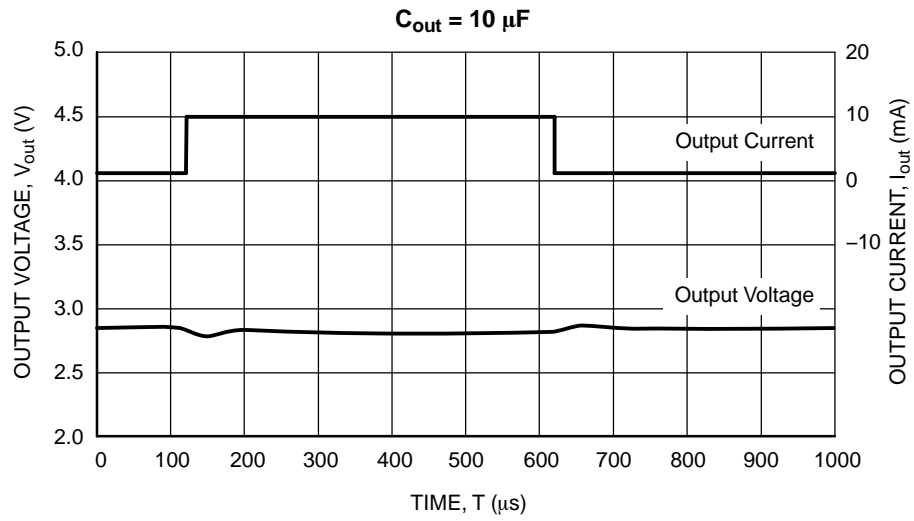
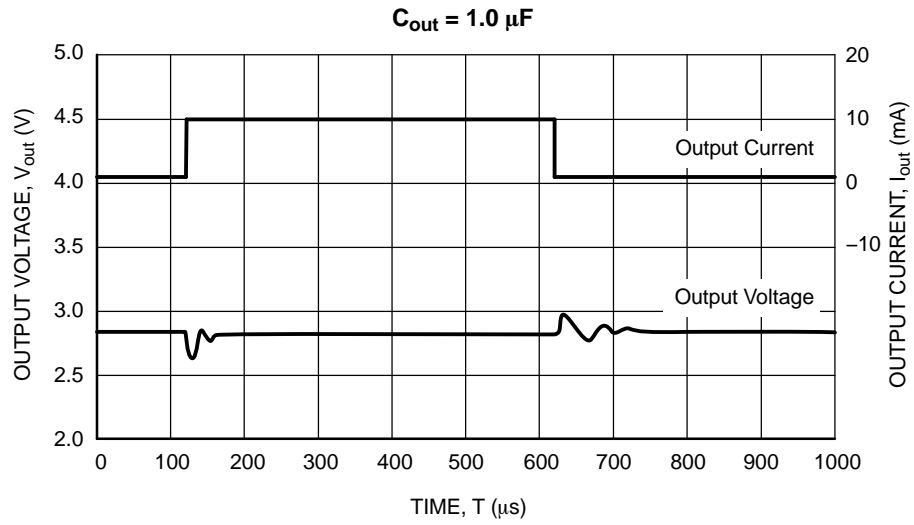


Figure 14. Load Transient Response
($V_{out} = 2.8$ V, $t_r = t_f = 5.0 \mu s$, $V_{in} = 3.8$ V)

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TYPICAL CHARACTERISTICS

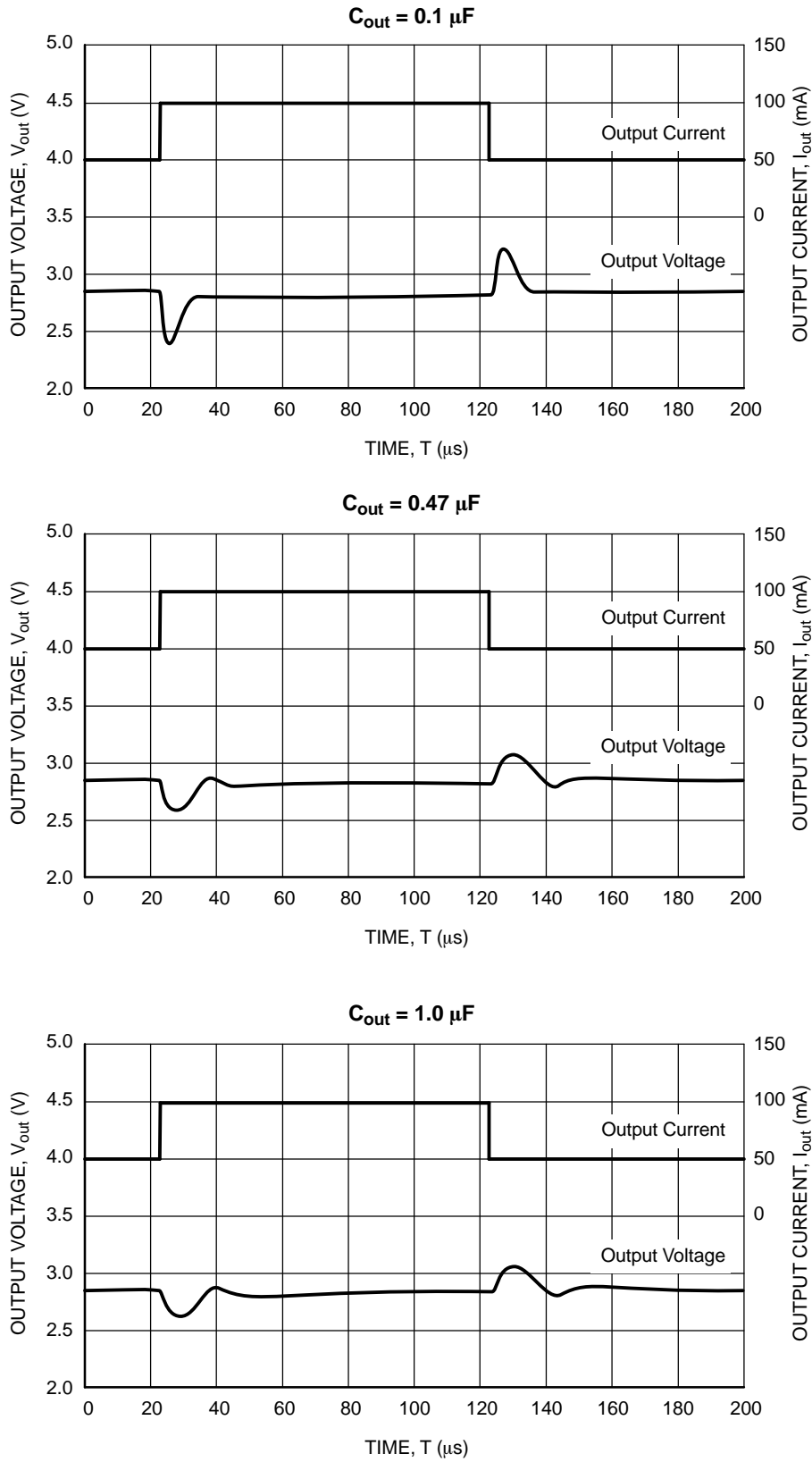


Figure 15. Load Transient Response
(V_{out} = 2.8 V, tr = tf = 5.0 μs, V_{in} = 3.8 V)

NCP583

APPLICATION INFORMATION

Input Decoupling

A 1.0 μF ceramic capacitor is the recommended value to be connected between V_{in} and GND. For PCB layout considerations, the traces of V_{in} and GND should be sufficiently wide in order to minimize noise and prevent unstable operation.

Output Decoupling

It is recommended to use a 0.1 μF ceramic capacitor on the V_{out} pin. For better performance, select a capacitor with low Equivalent Series Resistance (ESR). For PCB layout considerations, place the output capacitor close to the output pin and keep the leads short as possible.

ORDERING INFORMATION

| Device | Output Type / Features | Nominal Output Voltage | Marking | Package | Shipping† |
|---------------|------------------------|------------------------|---------|-------------------|--------------------|
| NCP583SQ15T1G | Active High w/Enable | 1.5 | A5 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ18T1G | Active High w/Enable | 1.8 | A8 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ25T1G | Active High w/Enable | 2.5 | B5 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ27T1G | Active High w/Enable | 2.7 | B7 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ28T1G | Active High w/Enable | 2.8 | B8 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ30T1G | Active High w/Enable | 3.0 | C0 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583SQ33T1G | Active High w/Enable | 3.3 | C3 | SC-82AB (Pb-Free) | 3000 / Tape & Reel |
| NCP583XV15T2G | Active High w/Enable | 1.5 | G15B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV18T2G | Active High w/Enable | 1.8 | G18B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV25T2G | Active High w/Enable | 2.5 | G25B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV26T2G | Active High w/Enable | 2.6 | G26B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV28T2G | Active High w/Enable | 2.8 | G28B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV29T2G | Active High w/Enable | 2.9 | G29B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV30T2G | Active High w/Enable | 3.0 | G30B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV31T2G | Active High w/Enable | 3.1 | G31B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |
| NCP583XV33T2G | Active High w/Enable | 3.3 | G33B | SOT-563 (Pb-Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Other voltages are available. Consult your ON Semiconductor representative.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

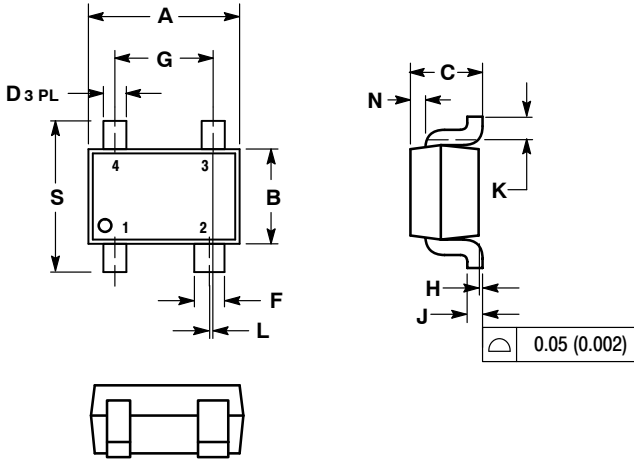
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SC-82AB
CASE 419C-02
ISSUE F

DATE 22 JUN 2012

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 419C-01 OBSOLETE. NEW STANDARD IS 419C-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.80 | 2.20 | 0.071 | 0.087 |
| B | 1.15 | 1.35 | 0.045 | 0.053 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| F | 0.30 | 0.50 | 0.012 | 0.020 |
| G | 1.10 | 1.50 | 0.043 | 0.059 |
| H | 0.00 | 0.10 | 0.000 | 0.004 |
| J | 0.10 | 0.26 | 0.004 | 0.010 |
| K | 0.10 | --- | 0.004 | --- |
| L | 0.05 BSC | | 0.002 BSC | |
| N | 0.20 REF | | 0.008 REF | |
| S | 1.80 | 2.40 | 0.07 | 0.09 |

SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Month Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

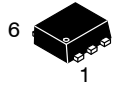
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

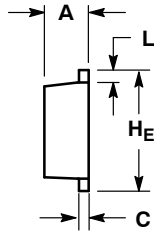
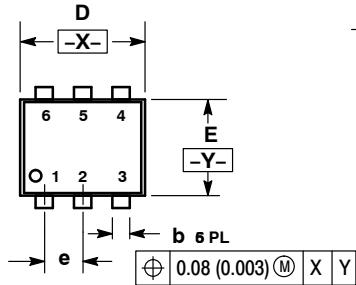
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SOT-563, 6 LEAD CASE 463A ISSUE G

DATE 23 SEP 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|----------------|-------------|------|------|----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.021 | 0.023 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| C | 0.08 | 0.12 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 1.50 | 1.60 | 1.70 | 0.059 | 0.062 | 0.066 |
| E | 1.10 | 1.20 | 1.30 | 0.043 | 0.047 | 0.051 |
| e | 0.5 BSC | | | 0.02 BSC | | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| H _E | 1.50 | 1.60 | 1.70 | 0.059 | 0.062 | 0.066 |

STYLE 1:

- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

STYLE 2:

- PIN 1. EMITTER 1
- 2. EMITTER 2
- 3. BASE 2
- 4. COLLECTOR 2
- 5. BASE 1
- 6. COLLECTOR 1

STYLE 3:

- PIN 1. CATHODE 1
- 2. CATHODE 1
- 3. ANODE/ANODE 2
- 4. CATHODE 2
- 5. CATHODE 2
- 6. ANODE/ANODE 1

STYLE 4:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 5:

- PIN 1. CATHODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. CATHODE
- 6. CATHODE

STYLE 6:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. ANODE
- 6. CATHODE

STYLE 8:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

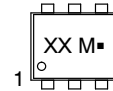
STYLE 9:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 2
- 6. DRAIN 1

STYLE 10:

- PIN 1. CATHODE 1
- 2. N/C
- 3. CATHODE 2
- 4. ANODE 2
- 5. N/C
- 6. ANODE 1

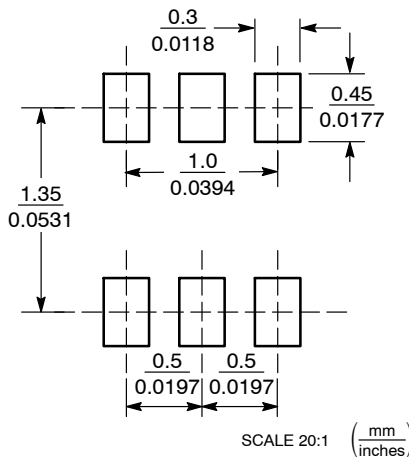
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Month Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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