

# NCP81061

## VR12 Compatible Synchronous Buck Dual MOSFET Driver

The NCP81061 is a high performance dual MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. It can drive a 3 nF load with a 30 ns propagation delay and a 30 ns transition time.

Adaptive anti-cross-conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook and desktop systems. The Bidirectional EN pins can provide a fault signal to the controller when the gate driver detects an OVP or UVLO fault. Also, an under-voltage lockout function guarantees the outputs are low when supply voltage is low.

### Features

- Adaptive Anti-Cross-Conduction Circuit
- Integrated Bootstrap Diode
- Pre OV Function
- ZCD Detect
- Floating Top Driver Accommodates Boost Voltages of up to 35 V
- Output Disable Control Turns Off Both MOSFETs
- Under-voltage Lockout
- Power Saving Operation Under Light Load Conditions
- Direct Interface to NCP6151 and Other Compatible PWM Controllers
- Thermally Enhanced Package
- This is a Pb-Free Device

### Typical Applications

- Power Management solutions for Desktop and Server Systems



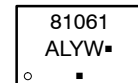
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM

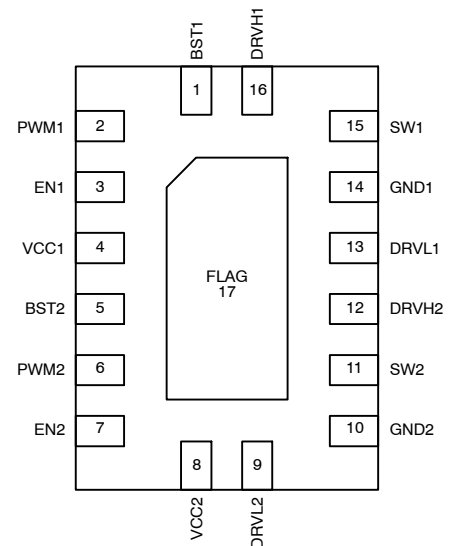


QFN16  
CASE 485AW



81061 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)



Pin Connections (Top View)

### ORDERING INFORMATION

| Device        | Package            | Shipping†             |
|---------------|--------------------|-----------------------|
| NCP81061MNTWG | QFN16<br>(Pb-Free) | 3000 / Tape &<br>Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NCP81061

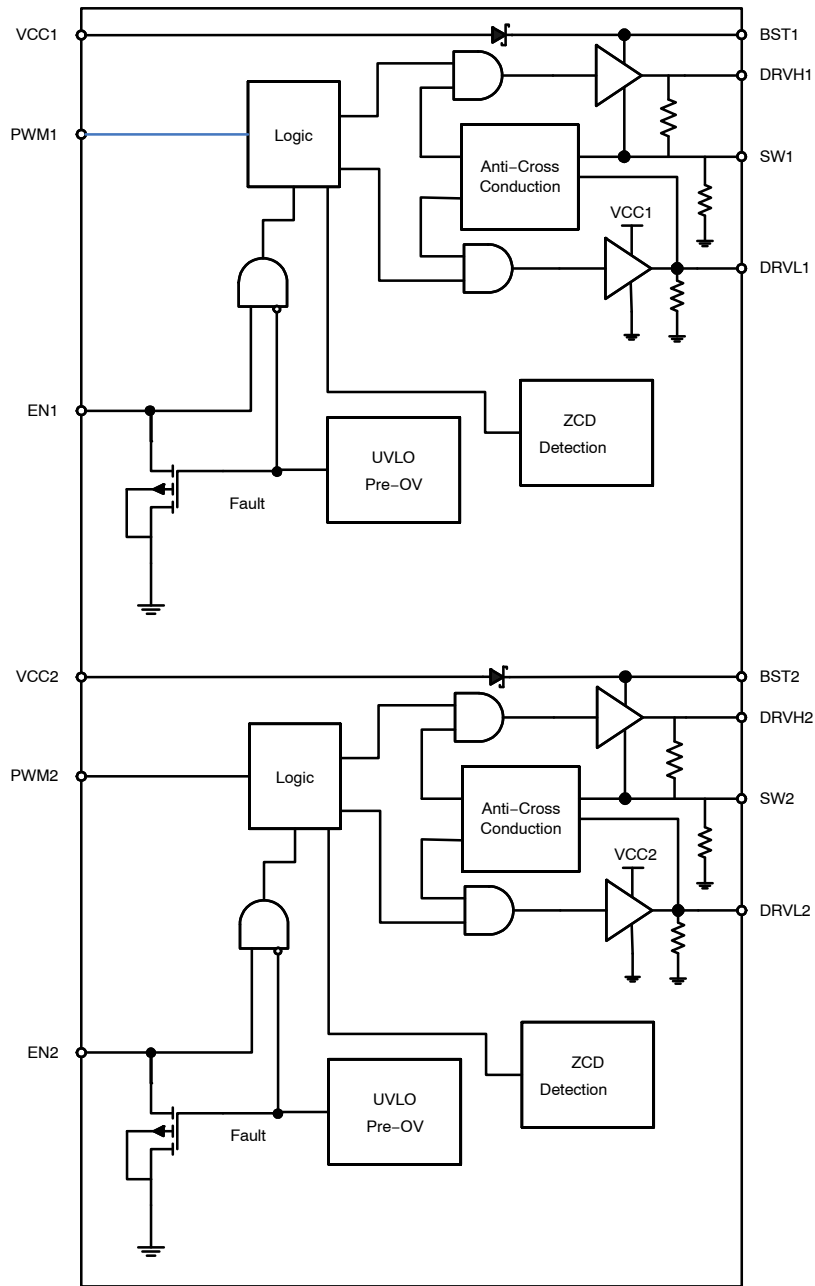


Figure 1. Block Diagram

# NCP81061

## PIN DESCRIPTIONS

| Pin No. | Symbol       | Description   |
|---------|--------------|---|
| 1, 5    | BST1, BST2   | Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.                           |
| 2, 6    | PWM1, PWM2   | Control input. The PWM signal has four distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled. |
| 3, 7    | EN1, EN2     | Logic input. A logic high to enable the part and a logic low to disable the part.   |
| 4, 8    | VCC1, VCC2   | Power supply input. Connect a bypass capacitor (0.1 $\mu$ F) from this pin to ground.   |
| 9, 13   | DRVL1, DRVL2 | Low side gate drive output. Connect to the gate of low side MOSFET.   |
| 10, 14  | GND1, GND2   | Bias and reference ground. All signals are referenced to this node.   |
| 11, 15  | SW1, SW2     | Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.   |
| 12, 16  | DRVH1, DRVH2 | High side gate drive output. Connect to the gate of high side MOSFET.   |
| 17      | FLAG         | Thermal flag. There is no electrical connection to the IC. Connect to ground plane.   |

## APPLICATION CIRCUIT

## ABSOLUTE MAXIMUM RATINGS

### ELECTRICAL INFORMATION

| Pin Symbol   | Pin Name                                 | V <sub>MAX</sub>  | V <sub>MIN</sub>                       |
|--------------|--|---|--|
| VCC1, VCC2   | Main Supply Voltage Input                | 15 V  | -0.3 V                                 |
| BST1, BST2   | Bootstrap Supply Voltage                 | 35 V wrt/ GND<br>40 V $\leq$ 50 ns wrt/ GND<br>15 V wrt/ SW | -0.3 V wrt/SW                          |
| SW1, SW2     | Switching Node (Bootstrap Supply Return) | 35 V<br>40 V $\leq$ 50 ns                                   | -5 V<br>-10 V (200ns)                  |
| DRVH1, DRVH2 | High Side Driver Output                  | BST + 0.3 V   | -0.3 V wrt/SW<br>-2 V (<200 ns) wrt/SW |
| DRVL1, DRVL2 | Low Side Driver Output                   | VCC + 0.3 V   | -0.3 V DC<br>-5 V (< 200 ns)           |
| PWM1, PWM2   | DRVH and DRVL Control Input              | 6.5 V   | -0.3 V                                 |
| EN1, EN2     | Enable Pin                               | 6.5 V   | -0.3 V                                 |
| GND1, GND2   | Ground                                   | 0 V   | 0 V                                    |

### THERMAL INFORMATION

| Pin Symbol                                | Pin Name         | Typ         | Unit |
|---|------------------|-------------|------|
| Thermal Characteristic (Note 1)           | R <sub>θJA</sub> | 29          | °C/W |
| Operating Junction Temperature Range      | T <sub>J</sub>   | -10 to 150  | °C   |
| Operating Ambient Temperature Range       |                  | -10 to +125 | °C   |
| Maximum Storage Temperature Range         | T <sub>STG</sub> | -55 to +150 | °C   |
| Moisture Sensitivity Level<br>QFN Package | MSL              | 1           |      |

\*The maximum package power dissipation must be observed.  
1. 5776 mm<sup>2</sup> Cu., 1 oz. thickness.

# NCP81061

**NCP81061 DRIVER ELECTRICAL CHARACTERISTICS Unless otherwise stated**  $-10^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ ;  $V_{CC1}/V_{CC2} = 4.5\text{ V} \sim 13.2\text{ V}$

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------|-----------------|-----|-----|-----|------|
|-----------|-----------------|-----|-----|-----|------|

## SUPPLY VOLTAGE

|                          |  |     |      |      |   |
|--------------------------|--|-----|------|------|---|
| VCC Operation Voltage    |  | 4.5 |      | 13.2 | V |
| Power ON Reset threshold |  |     | 2.75 | 3.2  | V |

## UNDERVOLTAGE LOCKOUT

|  |   |     |      |     |    |
|--|---|-----|------|-----|----|
| VCC Start Threshold                          |   | 3.8 | 4.35 | 4.5 | V  |
| VCC UVLO Hysteresis                          |   | 150 | 200  | 250 | mV |
| Output Overvoltage Trip Threshold at Startup | Power Startup time, $V_{CC} > \text{POR}$ | 2.1 | 2.25 | 2.4 | V  |

## SUPPLY CURRENT

|                 |  |  |      |     |    |
|-----------------|--|--|------|-----|----|
| Normal mode     | $I_{CC} + I_{BST}$ , $EN = 5\text{ V}$ , $PWM = \text{OSC}$ , $F_{sw} = 100\text{ kHz}$ , $C_{LOAD} = 3\text{ nF}$ |  | 24.4 |     | mA |
| Standby Current | $I_{CC} + I_{BST}$ , $EN = \text{GND}$   |  | 1.0  | 3.8 | mA |
| Standby Current | $I_{CC} + I_{BST}$ , $EN = \text{HIGH}$ , $PWM = \text{LOW}$ , No loading on DRVH & DRVL                           |  | 4.2  |     | mA |
| Standby Current | $I_{CC} + I_{BST}$ , $EN = \text{HIGH}$ , $PWM = \text{HIGH}$ , No loading on DRVH & DRVL                          |  | 4.4  |     | mA |

## BOOTSTRAP DIODE

|                 |   |     |     |     |   |
|-----------------|---|-----|-----|-----|---|
| Forward Voltage | $V_{VCC} = 12\text{ V}$ , forward bias current = 2 mA | 0.1 | 0.4 | 0.6 | V |
|-----------------|---|-----|-----|-----|---|

## PWM INPUT

|                    |  |     |     |     |    |
|--------------------|--|-----|-----|-----|----|
| PWM Input High     |  | 3.4 |     |     | V  |
| PWM Mid-State      |  | 1.3 |     | 2.7 | V  |
| PWM Input Low      |  |     |     | 0.7 | V  |
| ZCD blanking timer |  |     | 250 |     | ns |

## HIGH SIDE DRIVER (VCC = 12 V)

|  |   |     |     |     |            |
|--|---|-----|-----|-----|------------|
| Output Impedance, Sourcing Current           | $VBST-VSW = 12\text{ V}$                                      |     | 2.0 | 3.5 | $\Omega$   |
| Output Impedance, Sinking Current            | $VBST-VSW = 12\text{ V}$                                      |     | 1.0 | 2.0 | $\Omega$   |
| DRVH Rise Time $t_{r_{DRVH}}$                | $V_{VCC} = 12\text{ V}$ , 3 nF load, $VBST-VSW = 12\text{ V}$ |     | 16  | 30  | ns         |
| DRVH Fall Time $t_{f_{DRVH}}$                | $V_{VCC} = 12\text{ V}$ , 3 nF load, $VBST-VSW = 12\text{ V}$ |     | 11  | 25  | ns         |
| DRVH Turn-Off Propagation Delay $tpd_{DRVH}$ | $C_{LOAD} = 3\text{ nF}$                                      | 8.0 |     | 30  | ns         |
| DRVH Turn-On Propagation Delay $tpd_{DRVH}$  | $C_{LOAD} = 3\text{ nF}$                                      |     |     | 30  | ns         |
| SW pull down resistance                      | SW to PGND  |     | 45  |     | k $\Omega$ |
| DRVH pull down resistance                    | DRVH to SW, $BST-SW = 0\text{ V}$                             |     | 45  |     | k $\Omega$ |

## HIGH SIDE DRIVER (VCC = 5 V)

|  |   |  |     |  |            |
|--|---|--|-----|--|------------|
| Output Impedance, Sourcing Current           | $VBST-VSW = 5\text{ V}$                                     |  | 4.5 |  | $\Omega$   |
| Output Impedance, Sinking Current            | $VBST-VSW = 5\text{ V}$                                     |  | 2.9 |  | $\Omega$   |
| DRVH Rise Time $t_{r_{DRVH}}$                | $V_{VCC} = 5\text{ V}$ , 3 nF load, $VBST-VSW = 5\text{ V}$ |  | 30  |  | ns         |
| DRVH Fall Time $t_{f_{DRVH}}$                | $V_{VCC} = 5\text{ V}$ , 3 nF load, $VBST-VSW = 5\text{ V}$ |  | 27  |  | ns         |
| DRVH Turn-Off Propagation Delay $tpd_{DRVH}$ | $C_{LOAD} = 3\text{ nF}$                                    |  | 20  |  | ns         |
| DRVH Turn-On Propagation Delay $tpd_{DRVH}$  | $C_{LOAD} = 3\text{ nF}$                                    |  | 27  |  | ns         |
| SW pull down resistance                      | SW to PGND  |  | 45  |  | k $\Omega$ |
| DRVH pull down resistance                    | DRVH to SW, $BST-SW = 0\text{ V}$                           |  | 45  |  | k $\Omega$ |

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| Parameter  | Test Conditions                      | Min | Typ | Max | Unit             |
|--|--------------------------------------|-----|-----|-----|------------------|
| <b>LOW SIDE DRIVER (VCC = 12 V)</b>              |                                      |     |     |     |                  |
| Output Impedance, Sourcing Current               |                                      |     | 2.0 | 3.5 | $\Omega$         |
| Output Impedance, Sinking Current                |                                      |     | 0.8 | 1.8 | $\Omega$         |
| DRVL Rise Time $t_{r_{DRVL}}$                    | $C_{LOAD} = 3\text{ nF}$             |     | 16  | 35  | ns               |
| DRVL Fall Time $t_{f_{DRVL}}$                    | $C_{LOAD} = 3\text{ nF}$             |     | 11  | 15  | ns               |
| DRVL Turn-Off Propagation Delay $tpd_{l_{DRVL}}$ | $C_{LOAD} = 3\text{ nF}$             |     |     | 35  | ns               |
| DRVL Turn-On Propagation Delay $tpd_{h_{DRVL}}$  | $C_{LOAD} = 3\text{ nF}$             | 8.0 |     | 30  | ns               |
| DRVL pull down resistance                        | DRVL to PGND, $V_{CC} = \text{PGND}$ |     | 45  |     | $\text{k}\Omega$ |

|  |                                      |  |     |  |                  |
|--|--------------------------------------|--|-----|--|------------------|
| <b>LOW SIDE DRIVER (VCC = 5 V)</b>               |                                      |  |     |  |                  |
| Output Impedance, Sourcing Current               |                                      |  | 4.5 |  | $\Omega$         |
| Output Impedance, Sinking Current                |                                      |  | 2.4 |  | $\Omega$         |
| DRVL Rise Time $t_{r_{DRVL}}$                    | $C_{LOAD} = 3\text{ nF}$             |  | 30  |  | ns               |
| DRVL Fall Time $t_{f_{DRVL}}$                    | $C_{LOAD} = 3\text{ nF}$             |  | 22  |  | ns               |
| DRVL Turn-Off Propagation Delay $tpd_{l_{DRVL}}$ | $C_{LOAD} = 3\text{ nF}$             |  | 27  |  | ns               |
| DRVL Turn-On Propagation Delay $tpd_{h_{DRVL}}$  | $C_{LOAD} = 3\text{ nF}$             |  | 12  |  | ns               |
| DRVL pull down resistance                        | DRVL to PGND, $V_{CC} = \text{PGND}$ |  | 45  |  | $\text{k}\Omega$ |

## EN INPUT

|   |  |     |     |     |               |
|---|--|-----|-----|-----|---------------|
| Input Voltage High                      |  | 2.0 |     |     | V             |
| Input Voltage Low                       |  |     |     | 1.0 | V             |
| Hysteresis                              |  |     | 500 |     | mV            |
| Normal mode bias current                |  | -1  |     | 1   | $\mu\text{A}$ |
| Fault mode Enable pin pull down current |  | 4   |     | 30  | mA            |
| Propagation Delay Time                  |  |     | 20  | 40  | ns            |

## SW Node

|  |  |  |    |    |               |
|--|--|--|----|----|---------------|
| SW node leakage current                |  |  |    | 20 | $\mu\text{A}$ |
| Zero Cross Detection Threshold Voltage | SW to $-20\text{ mV}$ , ramp slowly until BG go off. (start in DCM mode) |  | -6 |    | mV            |

## DECODER TRUTH TABLE

| PWM INPUT | ZCD                                   | DRVL | DRVH |
|-----------|---------------------------------------|------|------|
| PWM High  | ZCD Reset                             | Low  | High |
| PWM Mid   | Positive current through the inductor | High | Low  |
| PWM Mid   | Zero current through the inductor     | Low  | Low  |
| PWM Low   | ZCD Reset                             | High | Low  |

# NCP81061

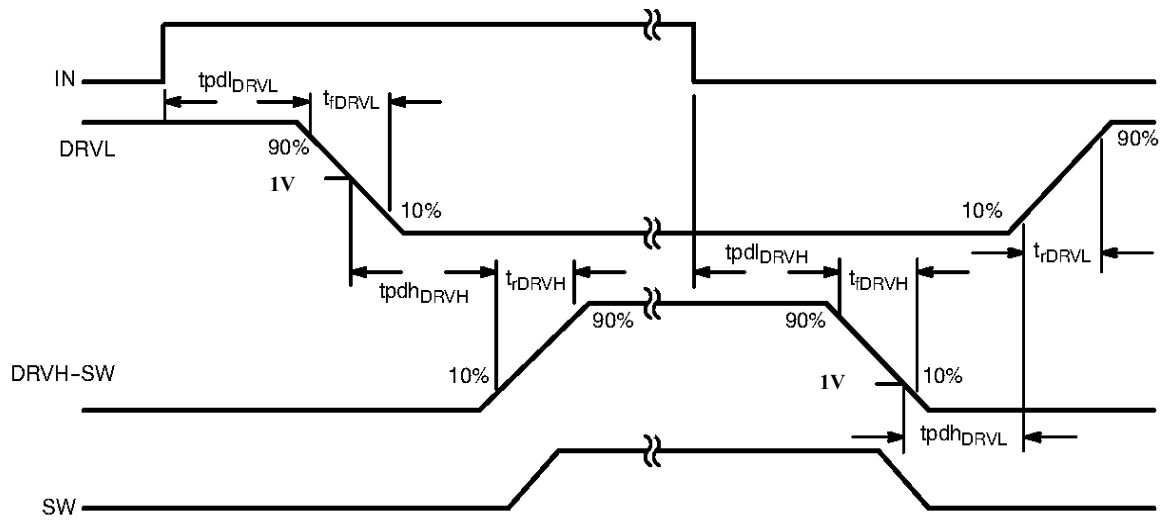


Figure 2.

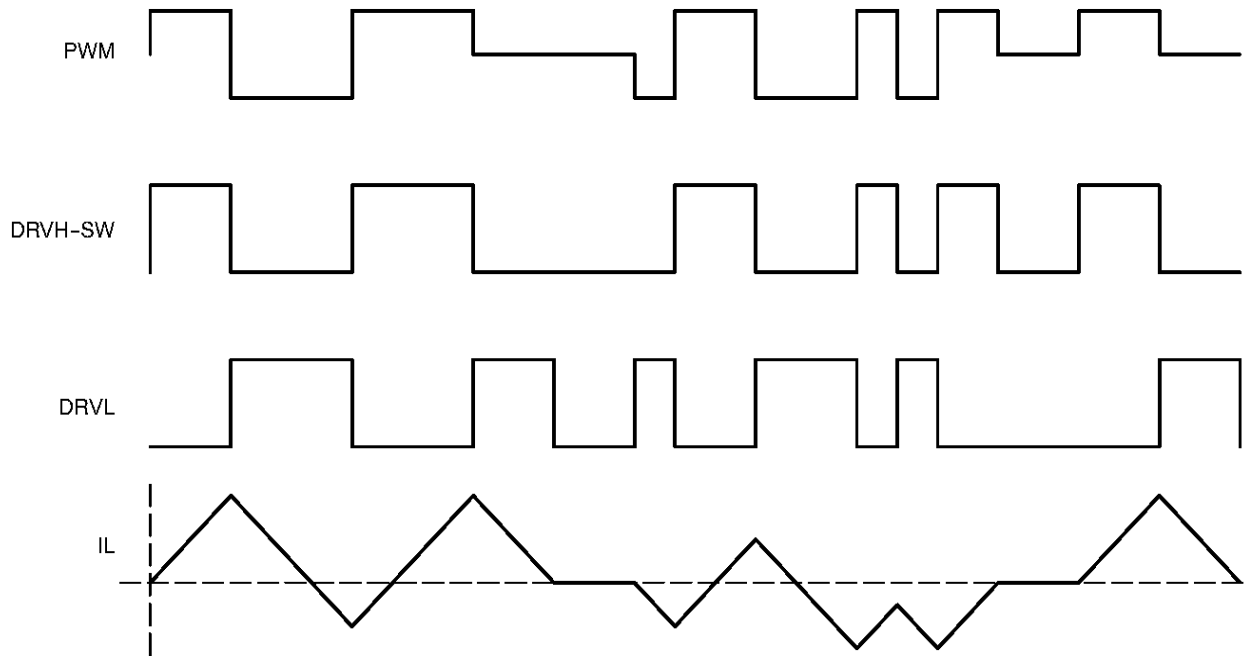


Figure 3. Timing Diagram

APPLICATION INFORMATION

The NCP81061 gate driver is a dual phase MOSFET driver designed for driving N-channel MOSFETs in a synchronous buck converter topology. The NCP81061 is designed to work with ON Semiconductor’s NCP6151 multi-phase controller.

**Under-voltage Lockout**

DRVH and DRVL are held low until V<sub>CC</sub> reaches 4.5 V during start-up. The PWM signals will control the gate status when the V<sub>CC</sub> threshold is exceeded. If V<sub>CC</sub> decreases to 200 mV below the threshold, the driver outputs will be forced low until V<sub>CC</sub> rises above the start-up threshold.

**Power-On Reset**

The power-on reset feature is used to protect a gate driver from abnormal status during start-up. When the initial V<sub>CC</sub> soft-start voltage is higher than 2.75 V, the gate driver will monitor the SW pin. If the SW pin is higher than 2.25 V, bottom gate will be forced high to discharge the output capacitor. The fault mode will be latched and the EN pin will be forced low until the driver is recycled. When the V<sub>CC</sub> voltage is higher than 4.5 V, and EN is high, the driver will enter normal operation.

**Bi-directional EN Signal**

When the driver is in a fault mode such as Power-On Reset and Under-Voltage Lockout, it will de-assert the EN pin by pulling it low. This will pull down the DRON pin of the controller as well.

**PWM Input and Zero Cross Detect (ZCD)**

The PWM input, along with EN and ZCD, control the state of DRVH and DRVL. When PWM is set high, DRVH will be set high after the adaptive non-overlap delay. When PWM is set low, DRVL will be set high after the adaptive non-overlap delay. When the PWM is set to the mid state, DRVH will be set low, and after the adaptive non-overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer is expired, the SW pin will be monitored for zero cross detection. After the detection, the DRVL will be set low.

**Adaptive Non-overlap**

The non-overlap dead time control is used to avoid shoot-through current from damaging the power MOSFETs. When the PWM signal is pulled high, DRVL will start to go low after a propagation delay (tpd<sub>DRVL</sub>). The driver will monitor the DRVL voltage until a threshold where an internal timer (tpdh<sub>DRVH</sub>) will delay turn-on of the high-side MOSFET. When the PWM signal is pulled low, DRVH will start to go low after a propagation delay (tpd<sub>DRVH</sub>). The driver will monitor the difference between the DRVH and SW voltages until a threshold where an internal timer (tpdh<sub>DRVL</sub>) delays turn-on of the low-side MOSFET.

**Layout Guidelines**

Layout for DC-DC converter is very important. The bootstrap and V<sub>CC</sub> bypass capacitors should be placed as close the driver IC as possible.

Connect GND pin to a local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. The thermal slug should be tied to the ground plane for good heat dissipation. To minimize the ground loop for low side MOSFET, the driver GND pin should be close to the low-side MOSFET source pin. The gate drive trace should be routed to minimize the length, with a minimum width of 20 mils.

**Gate Driver Power Loss Calculation**

The gate driver power loss consists of the gate drive loss and quiescent power loss.

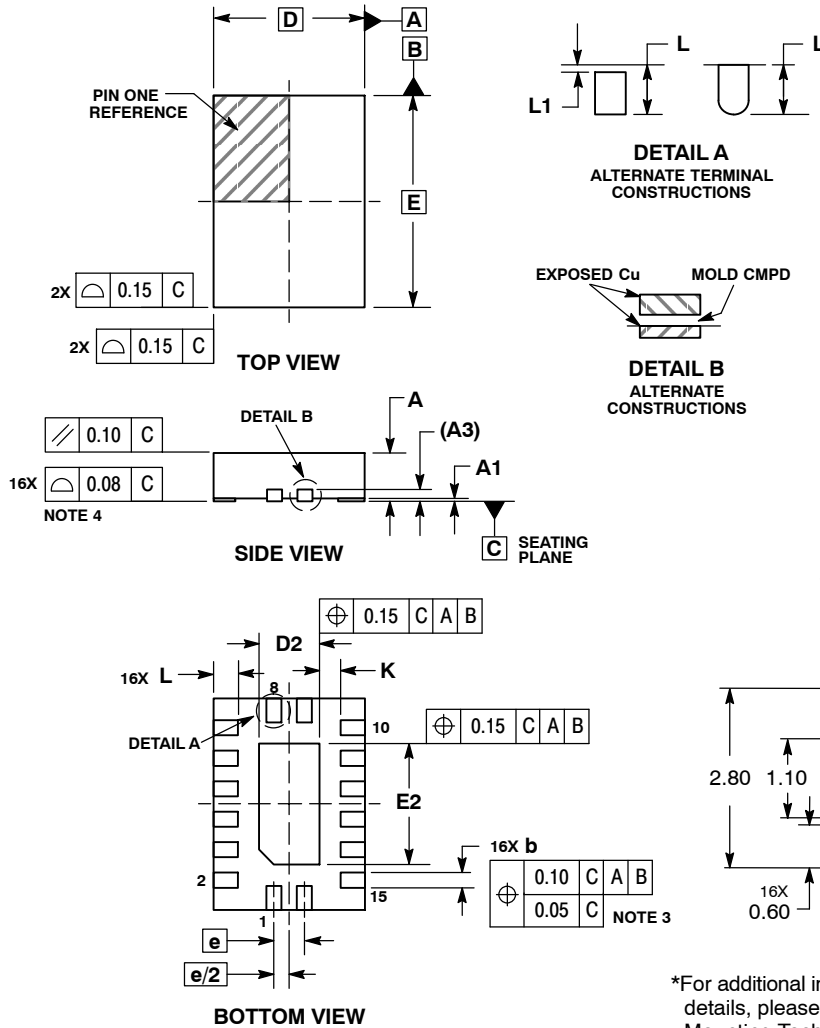
The equation below can be used to calculate the power dissipation of the gate driver. Where Q<sub>GMF</sub> is the total gate charge for each main MOSFET and Q<sub>QSF</sub> is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[ \frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{QFS}) + I_{CC} \right] \times V_{CC}$$

# NCP81061

## PACKAGE DIMENSIONS

**QFN16, 2.5x3.5, 0.5P**  
CASE 485AW  
ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.50 BSC    |      |
| D2  | 0.85        | 1.15 |
| E   | 3.50 BSC    |      |
| E2  | 1.85        | 2.15 |
| e   | 0.50 BSC    |      |
| K   | 0.20        | ---  |
| L   | 0.35        | 0.45 |
| L1  | ---         | 0.15 |

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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