0.9 V, Rail-to-Rail, Single Operational Amplifier
NCS2001, NCV2001

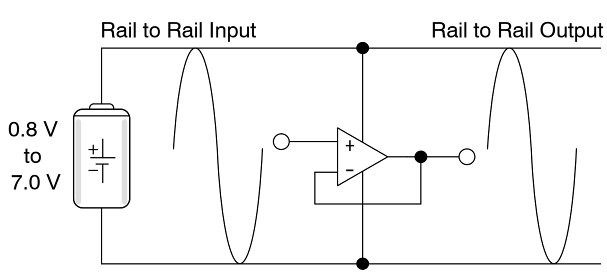
The NCS2001 is an industry first sub–one voltage operational amplifier that features a rail–to–rail common mode input voltage range, along with rail–to–rail output drive capability. This amplifier is guaranteed to be fully operational down to 0.9 V, providing an ideal solution for powering applications from a single cell Nickel Cadmium (NiCd) or Nickel Metal Hydride (NiMH) battery. Additional features include no output phase reversal with overdriven inputs, trimmed input offset voltage of 0.5 mV, extremely low input bias current of 40 pA, and a unity gain bandwidth of 1.4 MHz at 5.0 V. The tiny NCS2001 is the ideal solution for small portable electronic applications and is available in the space saving SOT23–5 and SC70–5 packages with two industry standard pinouts.

Features

- 0.9 V Guaranteed Operation
- Rail–to–Rail Common Mode Input Voltage Range
- Rail–to–Rail Output Drive Capability
- No Output Phase Reversal for Over–Driven Input Signals
- 0.5 mV Trimmed Input Offset
- 10 pA Input Bias Current
- 1.4 MHz Unity Gain Bandwidth at ±2.5 V, 1.1 MHz at ±0.5 V
- Tiny SC70–5 and SOT23–5 Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

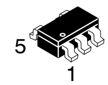
- Single Cell NiCd/NiMH Battery Powered Applications
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand–Held Instruments



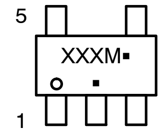
This device contains 63 active transistors.

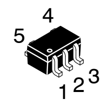
Figure 1. Typical Application

MARKING DIAGRAMS

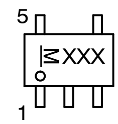


SOT23–5
SN SUFFIX
CASE 483





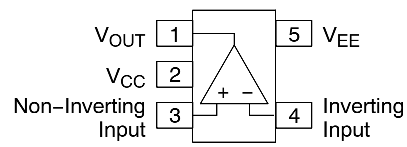
SC70–5
SQ SUFFIX
CASE 419A



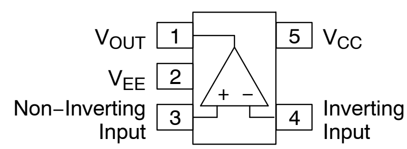
XXX = Specific Device Code
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



Style 1 Pinout (SN1T1, SQ1T2)



Style 2 Pinout (SN2T1, SQ2T2)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the dimensions section on page 14 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	7.0	V
Input Differential Voltage Range (Note 1)	V_{IDR}	V_{EE} −300 mV to 7.0 V	V
Input Common Mode Voltage Range (Note 1)	V_{ICR}	V_{EE} −300 mV to 7.0 V	V
Output Short Circuit Duration (Note 2)	t_{Sc}	Indefinite	sec
Junction Temperature	T_J	150	°C
Power Dissipation and Thermal Characteristics SOT23−5 Package Thermal Resistance, Junction−to−Air Power Dissipation @ T_A = 70°C SC70−5 Package Thermal Resistance, Junction−to−Air Power Dissipation @ T_A = 70°C	 $R_{\theta JA}$ P_D $R_{\theta JA}$ P_D	 235 340 280 286	 °C/W mW °C/W mW
Operating Ambient Temperature Range NCS2001 NCV2001 (Note 3)	T_A	 −40 to +105 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
ESD Protection at any Pin Human Body Model (Note 4)	V_{ESD}	1500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Either or both inputs should not exceed the range of V_{EE} −300 mV to V_{EE} +7.0 V.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. $T_J = T_A + (P_D\ R_{\theta JA})$.
3. NCV prefix is qualified for automotive usage.
4. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}				mV
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−8.5	–	8.5	
T_A = −40°C to 125°C		−9.5	–	9.5	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−7.0	–	7.0	
T_A = −40°C to 125°C		−7.5	–	7.5	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		−6.0	0.5	6.0	
T_A = 0°C to 70°C		−7.5	–	7.5	
T_A = −40°C to 125°C		−7.5	–	7.5	
Input Offset Voltage Temperature Coefficient (R_S = 50) T_A = −40°C to 125°C	$\Delta V_{IO}/\Delta T$	–	8.0	–	µV/°C
Input Bias Current (V_{CC} = 1.0 V to 5.0 V)	I_{IB}	–	10	–	pA
Input Common Mode Voltage Range	V_{ICR}	–	V_{EE} to V_{CC}	–	V
Large Signal Voltage Gain	A_{VOL}				kV/V
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
R_L = 10 k		–	40	–	
R_L = 2.0 k		–	20	–	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
R_L = 10 k		–	40	–	
R_L = 2.0 k		–	40	–	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
R_L = 10 k		20	40	–	
R_L = 2.0 k		15	40	–	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, High State Output (V_{ID} = +0.5 V)	V_{OH}				V
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
T_A = 25°C					
R_L = 10 k		0.40	0.494	–	
R_L = 2.0 k		0.35	0.466	–	
T_A = 0°C to 70°C					
R_L = 10 k		0.40	–	–	
R_L = 2.0 k		0.35	–	–	
T_A = −40°C to 125°C					
R_L = 10 k		0.40	–	–	
R_L = 2.0 k		0.35	–	–	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
T_A = 25°C					
R_L = 10 k		1.45	1.498	–	
R_L = 2.0 k		1.40	1.480	–	
T_A = 0°C to 70°C					
R_L = 10 k		1.45	–	–	
R_L = 2.0 k		1.40	–	–	
T_A = −40°C to 125°C					
R_L = 10 k		1.45	–	–	
R_L = 2.0 k		1.40	–	–	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C					
R_L = 10 k		2.45	2.498	–	
R_L = 2.0 k		2.40	2.475	–	
T_A = 0°C to 70°C					
R_L = 10 k		2.45	–	–	
R_L = 2.0 k		2.40	–	–	
T_A = −40°C to 125°C					
R_L = 10 k		2.45	–	–	
R_L = 2.0 k		2.40	–	–	
Output Voltage Swing, Low State Output (V_{ID} = −0.5 V)	V_{OL}				V
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
T_A = 25°C					
R_L = 10 k		–	−0.494	−0.40	
R_L = 2.0 k		–	−0.480	−0.35	
T_A = 0°C to 70°C					
R_L = 10 k		–	–	−0.40	
R_L = 2.0 k		–	–	−0.35	
T_A = −40°C to 125°C					
R_L = 10 k		–	–	−0.40	
R_L = 2.0 k		–	–	−0.35	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
T_A = 25°C					
R_L = 10 k		–	−1.493	−1.45	
R_L = 2.0 k		–	−1.480	−1.40	
T_A = 0°C to 70°C					
R_L = 10 k		–	–	−1.45	
R_L = 2.0 k		–	–	−1.40	
T_A = −40°C to 125°C					
R_L = 10 k		–	–	−1.45	
R_L = 2.0 k		–	–	−1.40	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		–			
R_L = 10 k		–	−2.492	−2.45	
R_L = 2.0 k			−2.479	−2.40	
T_A = 0°C to 70°C					
R_L = 10 k		–	–	−2.45	
R_L = 2.0 k		–	–	−2.40	
T_A = −40°C to 125°C					
R_L = 10 k		–	–	−2.45	
R_L = 2.0 k		–	–	−2.40	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Common Mode Rejection Ratio (V_{in} = 0 to 5.0 V)	CMRR	60	70	–	dB
Power Supply Rejection Ratio (V_{CC} = 0.5 V to 2.5 V, V_{EE} = −2.5 V)	PSRR	55	65	–	dB
Output Short Circuit Current	I_{SC}				mA
V_{CC} = 0.45 V, V_{EE} = −0.45 V, V_{ID} = ±0.4 V					
Source Current High Output State		0.5	1.2	–	
Sink Current Low Output State		–	−3.0	−1.5	
V_{CC} = 1.5 V, V_{EE} = −1.5 V, V_{ID} = ±0.5 V					
Source Current High Output State		15	29	–	
Sink Current Low Output State		–	−40	−20	
V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{ID} = ±0.5 V					
Source Current High Output State		40	76	–	
Sink Current Low Output State		–	−96	−50	
Power Supply Current (Per Amplifier, V_O = 0 V)	I_D				mA
V_{CC} = 0.45 V, V_{EE} = −0.45 V					
T_A = 25°C		–	0.51	1.10	
T_A = 0°C to 70°C		–	–	1.10	
T_A = −40°C to 125°C		–	–	1.10	
V_{CC} = 1.5 V, V_{EE} = −1.5 V					
T_A = 25°C		–	0.72	1.40	
T_A = 0°C to 70°C		–	–	1.40	
T_A = −40°C to 125°C		–	–	1.40	
V_{CC} = 2.5 V, V_{EE} = −2.5 V					
T_A = 25°C		–	0.82	1.50	
T_A = 0°C to 70°C		–	–	1.50	
T_A = −40°C to 125°C		–	–	1.50	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5 V, V_{EE} = −2.5 V, V_{CM} = V_O = 0 V, R_L to GND, T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	>1.0	–	tera Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	–	3.0	–	pF
Equivalent Input Noise Voltage (f = 1.0 kHz)	e_n	–	100	–	nV/√Hz
Gain Bandwidth Product (f = 100 kHz)	GBW				MHz
V_{CC} = 0.45 V, V_{EE} = −0.45 V		–	1.1	–	
V_{CC} = 1.5 V, V_{EE} = −1.5 V		–	1.3	–	
V_{CC} = 2.5 V, V_{EE} = −2.5 V		0.5	1.4	–	
Gain Margin (R_L = 10 k, C_L = 5.0 pf)	Am	–	6.5	–	dB
Phase Margin (R_L = 10 k, C_L = 5.0 pf)	φm	–	60	–	°
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 2.0 k, THD = 1.0%, A_V = 1.0)	BW_P	–	80	–	kHz
Total Harmonic Distortion (V_O = 4.0 V_{pp}, R_L = 2.0 k, A_V = 1.0)	THD				%
f = 1.0 kHz		–	0.008	–	
f = 10 kHz		–	0.08	–	
Slew Rate (V_S = ±2.5 V, V_O = −2.0 V to 2.0 V, R_L = 2.0 k, A_V = 1.0)	SR				V/μs
Positive Slope		1.0	1.6	6.0	
Negative Slope		1.0	1.6	6.0	

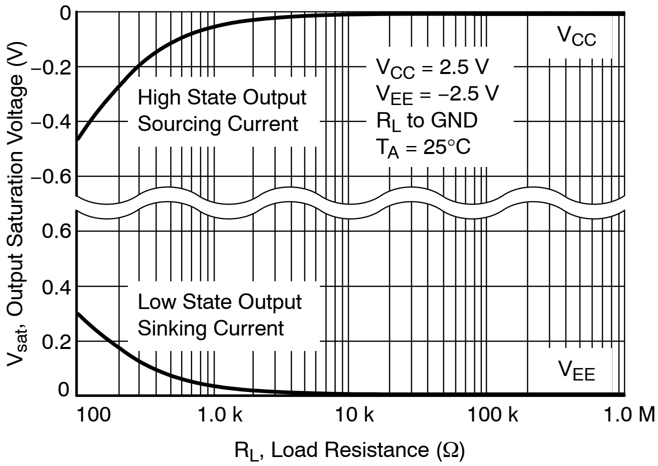


Figure 2. Split Supply Output Saturation vs. Load Resistance

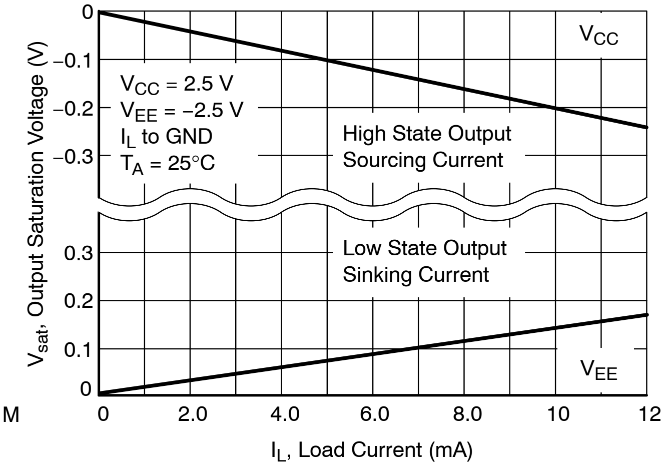


Figure 3. Split Supply Output Saturation vs. Load Current

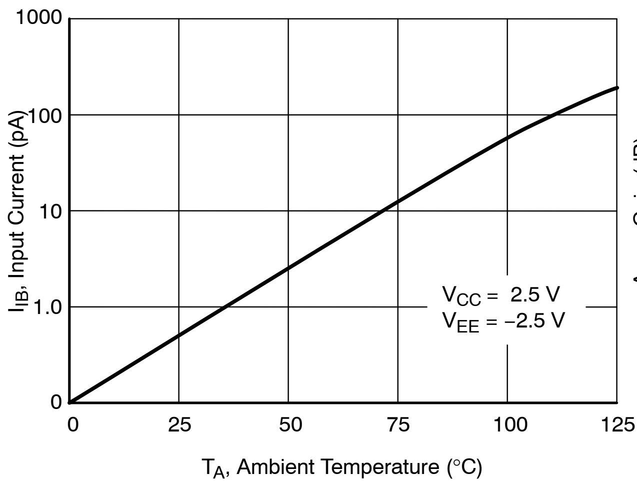


Figure 4. Input Bias Current vs. Temperature

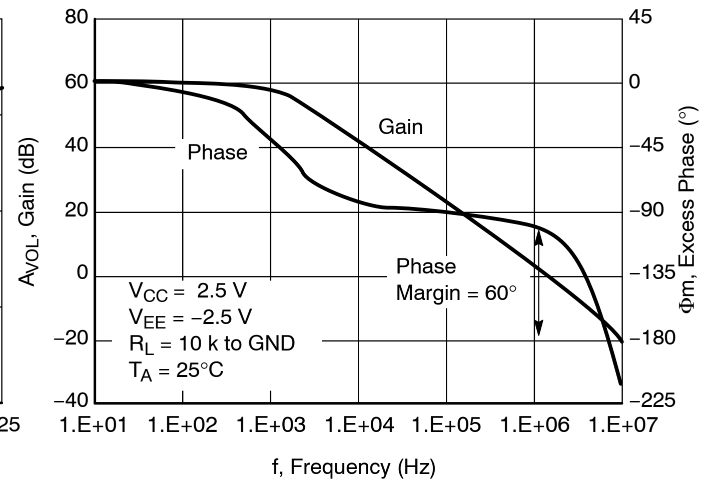


Figure 5. Gain and Phase vs. Frequency

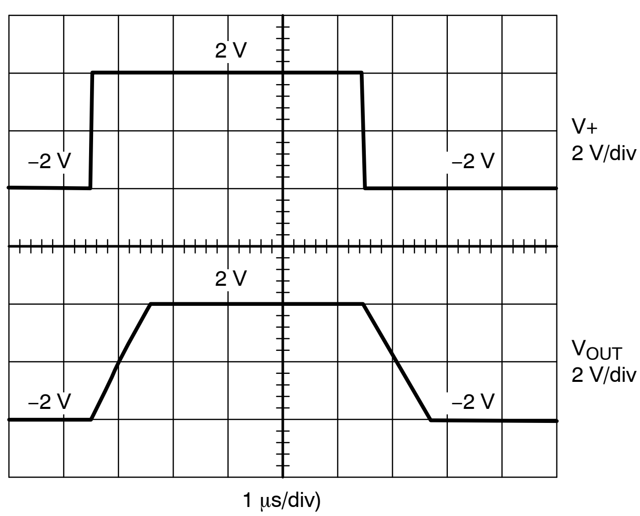


Figure 6. Transient Response

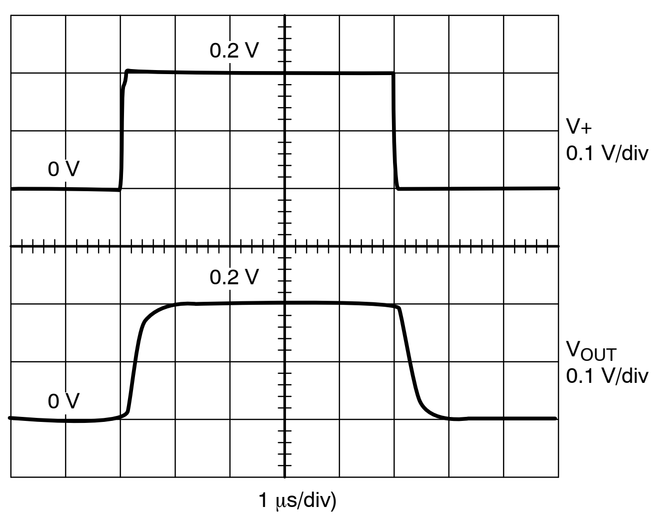


Figure 7. Slew Rate

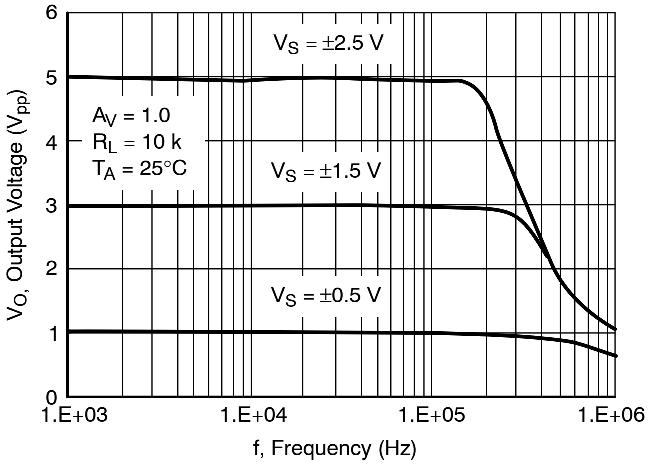


Figure 8. Output Voltage vs. Frequency

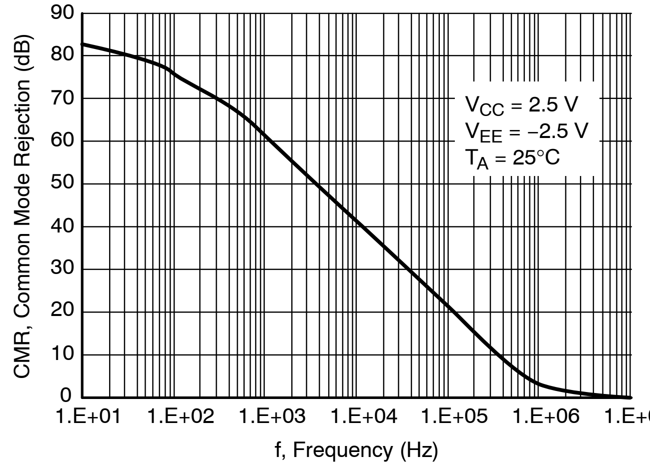


Figure 9. Common Mode Rejection vs. Frequency

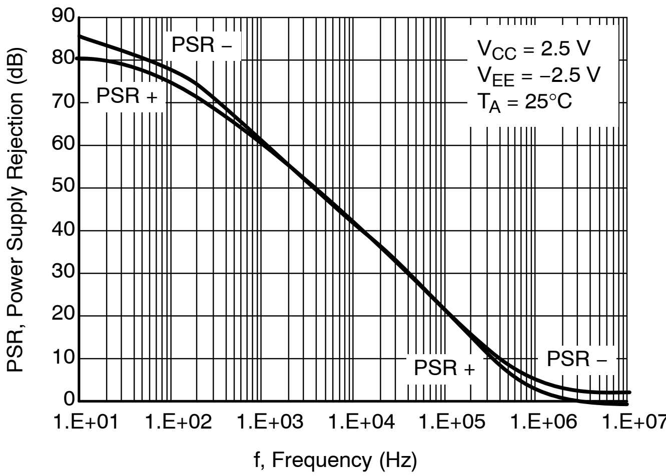


Figure 10. Power Supply Rejection vs. Frequency

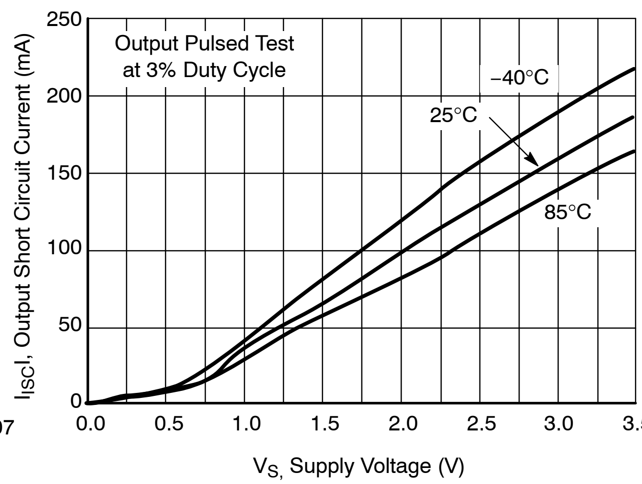


Figure 11. Output Short Circuit Sinking Current vs. Supply Voltage

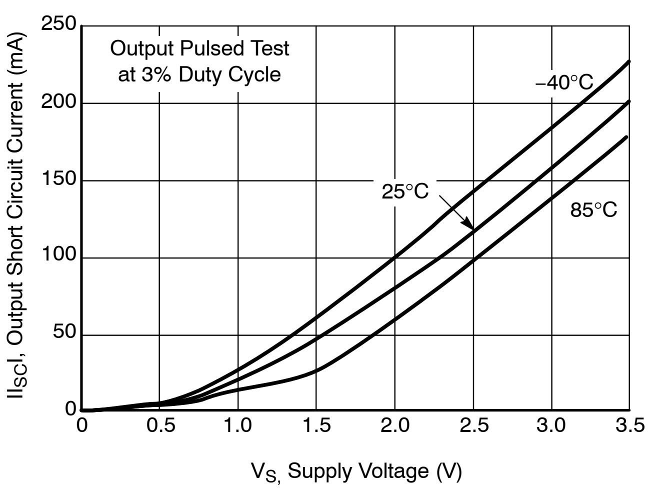


Figure 12. Output Short Circuit Sourcing Current vs. Supply Voltage

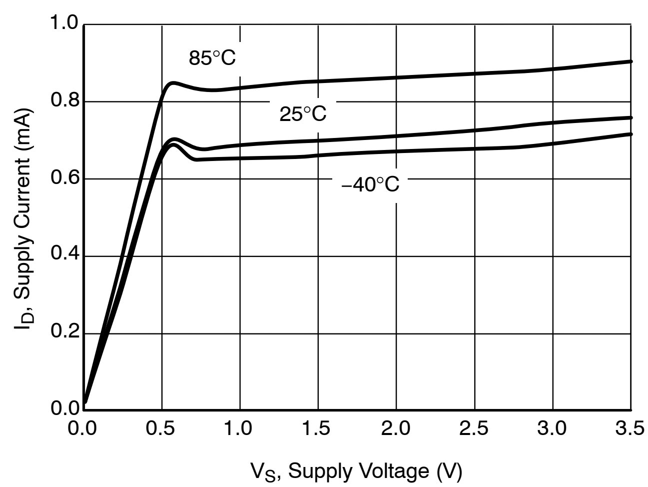


Figure 13. Supply Current vs. Supply Voltage

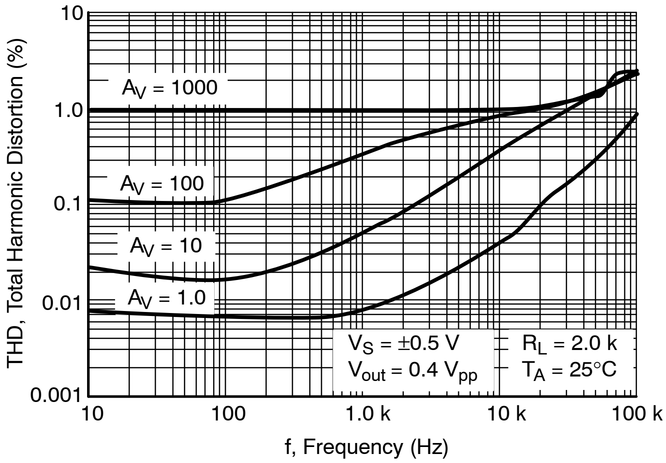


Figure 14. Total Harmonic Distortion vs. Frequency with 1.0 V Supply

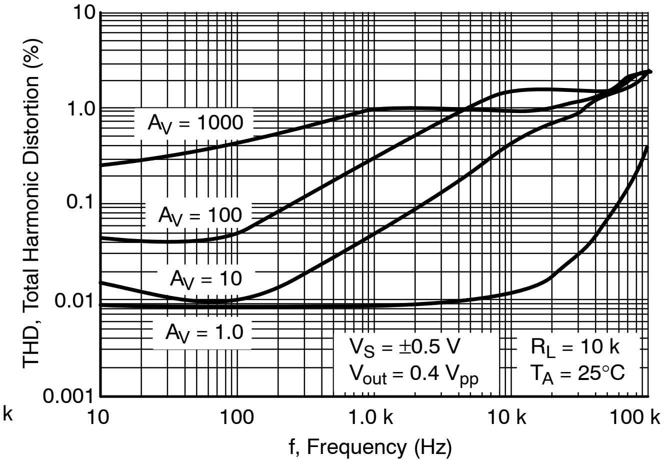


Figure 15. Total Harmonic Distortion vs. Frequency with 1.0 V Supply

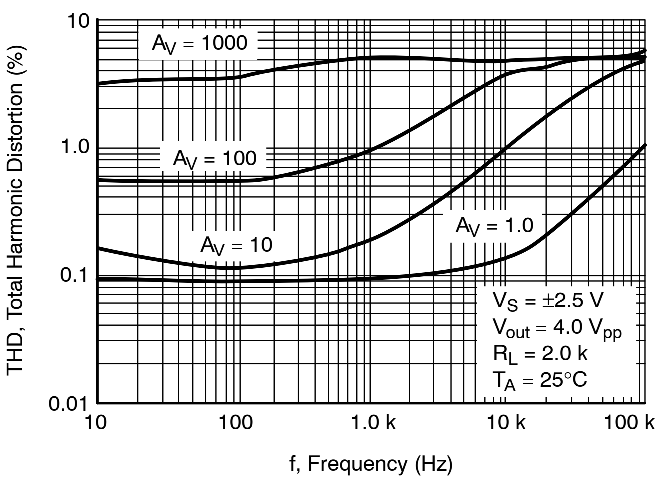


Figure 16. Total Harmonic Distortion vs. Frequency with 5.0 V Supply

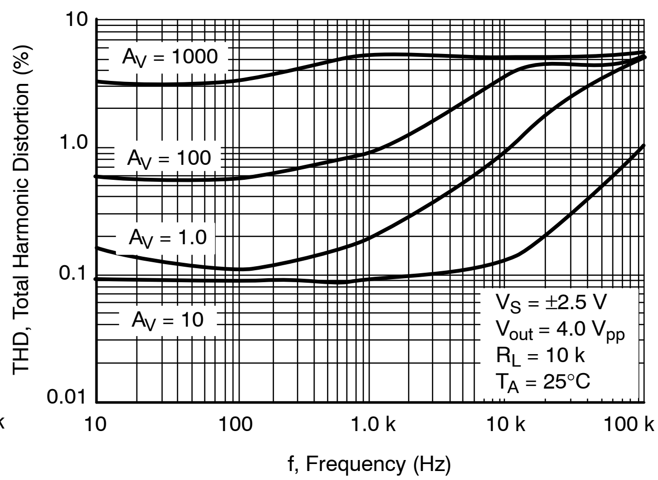


Figure 17. Total Harmonic Distortion vs. Frequency with 5.0 V Supply

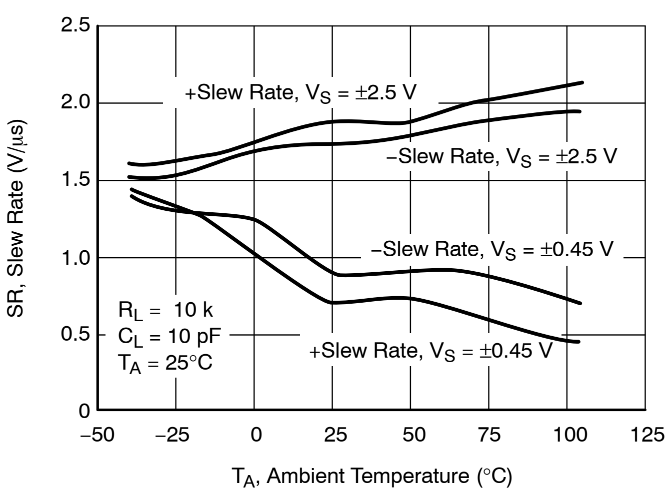


Figure 18. Slew Rate vs. Temperature

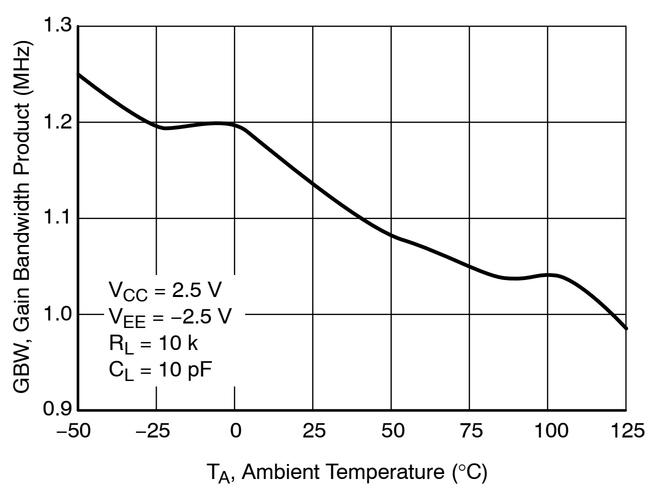


Figure 19. Gain Bandwidth Product vs. Temperature

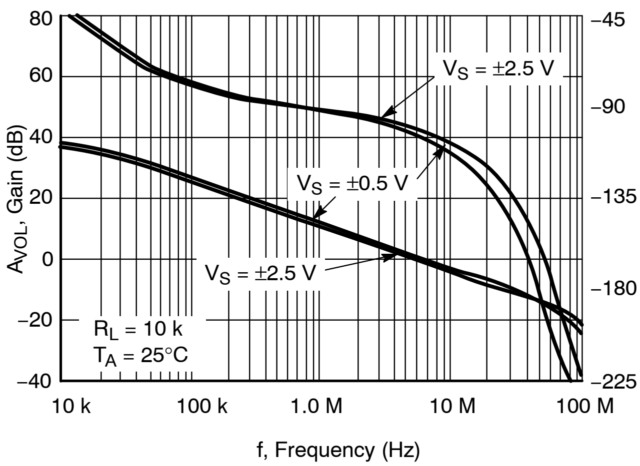


Figure 20. Voltage Gain and Phase vs. Frequency

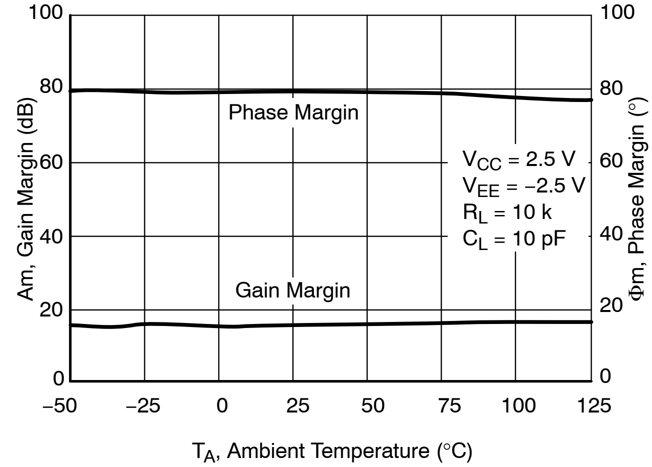


Figure 21. Gain and Phase Margin vs. Temperature

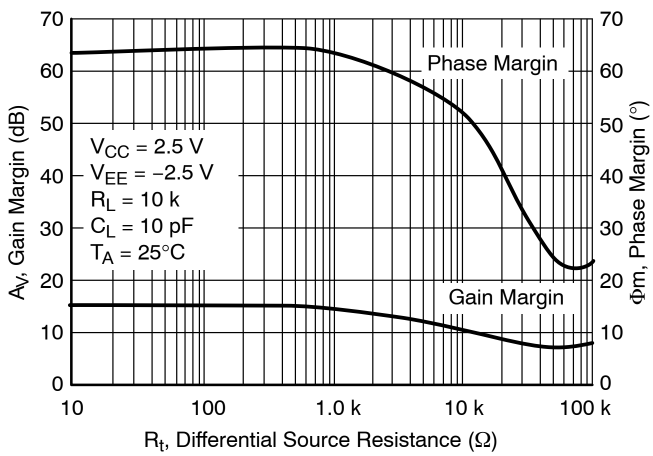


Figure 22. Gain and Phase Margin vs. Differential Source Resistance

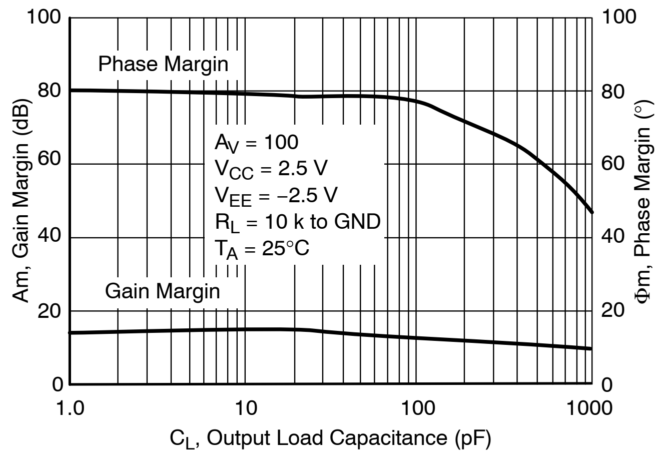


Figure 23. Gain and Phase Margin vs. Output Load Capacitance

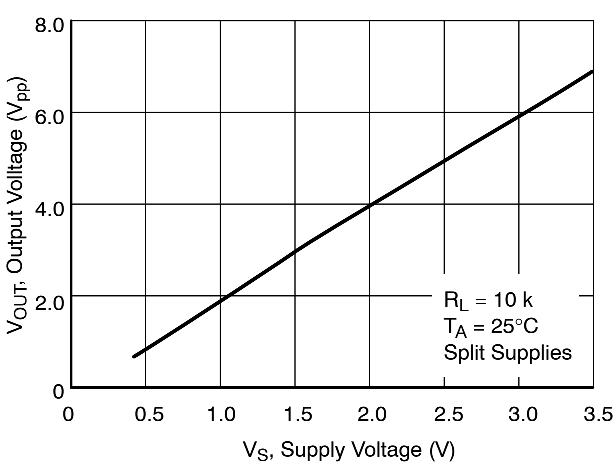


Figure 24. Output Voltage Swing vs. Supply Voltage

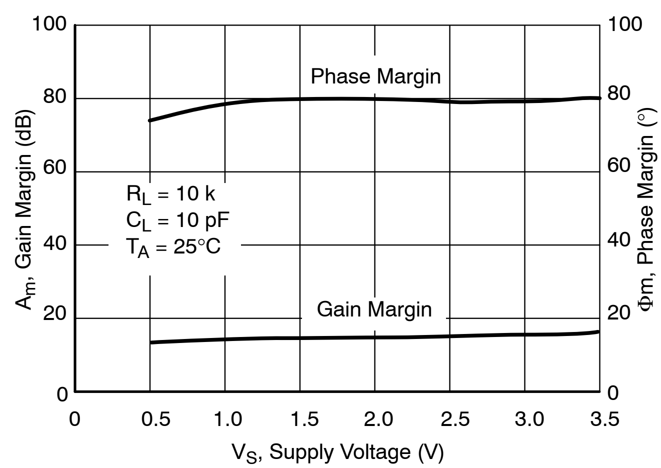


Figure 25. Gain and Phase Margin vs. Supply Voltage

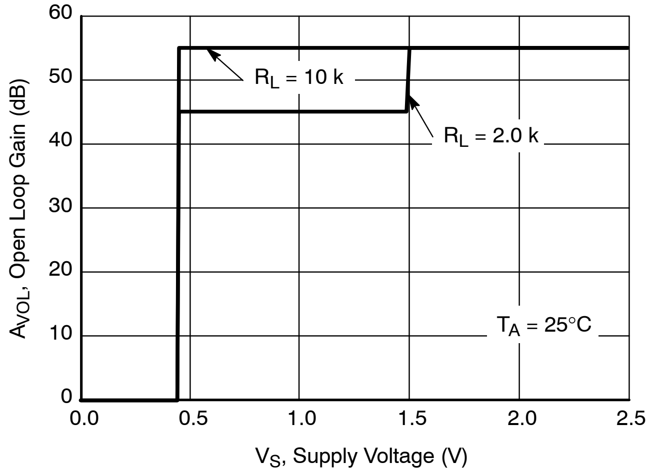


Figure 26. Open Loop Voltage Gain vs. Supply Voltage

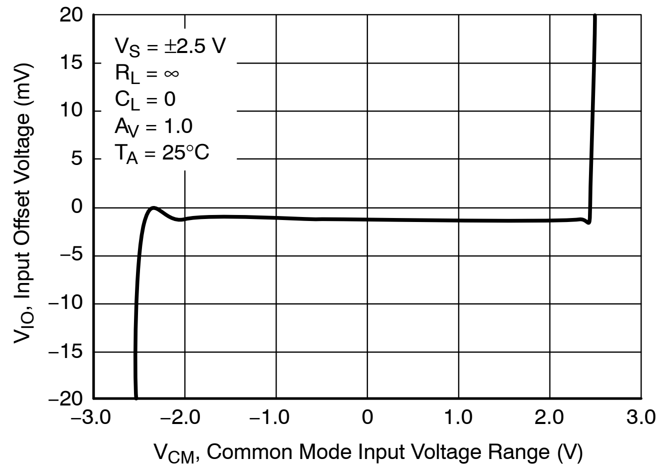


Figure 27. Input Offset Voltage vs. Common Mode Input Voltage Range V_S = ±2.5 V

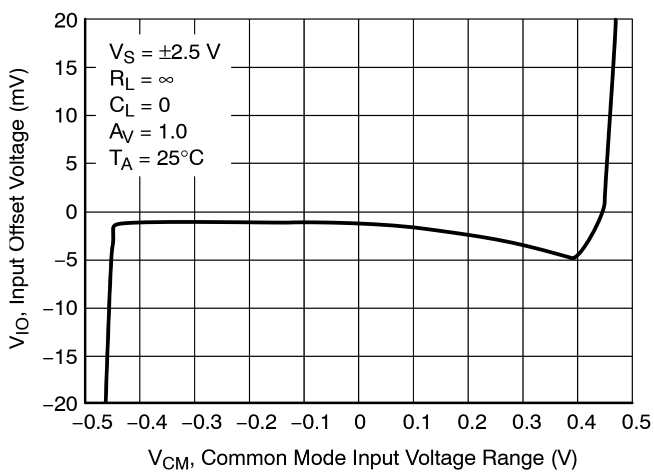


Figure 28. Input Offset Voltage vs. Common Mode Input Voltage Range, V_S = ±0.45 V

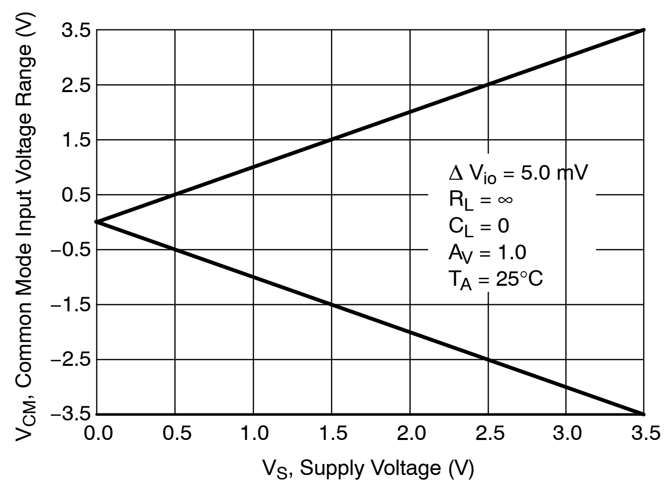


Figure 29. Common−Mode Input Voltage Range vs. Power Supply Voltage

APPLICATION INFORMATION AND OPERATING DESCRIPTION

GENERAL INFORMATION

The NCS2001 is an industry first rail−to−rail input, rail−to−rail output amplifier that features guaranteed sub−one voltage operation. This unique feature set is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, 2.2 V/μs slew rate and is operational over a power supply range less than 0.9 V to as high as 7.0 V.

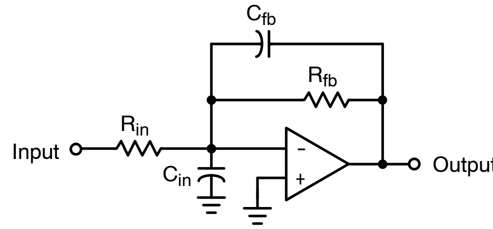
Inputs

The input topology chosen for this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N−Channel depletion mode differential transistor pair that drives a folded cascade stage and current mirror. This configuration extends the input common mode voltage range to encompass the V_{EE} and V_{CC} power supply rails, even when powered from a combined total of less than 0.9 V. Figures 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N−Channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 10 pA. The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as V_{EE} minus 300 mV to as high as 7.0 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA.

The ultra low input bias current of the NCS2001 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances C_{in}, will add an additional pole to the single pole amplifier in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of C_{in}, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor C_{fb}. An approximate value for C_{fb} can be calculated by:

$$C_{fb} = \frac{R_{in} \times C_{in}}{R_{fb}}$$



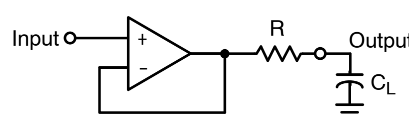
C_{in} = Input and printed circuit board capacitance

Figure 30. Input Capacitance Pole Cancellation

Output

The output stage consists of complementary P and N−Channel devices connected to provide rail−to−rail output drive. With a 2.0 k load, the output can swing within 50 mV of either rail. It is also capable of supplying over 75 mA when powered from 5.0 V and 1.0 mA when powered from 0.9 V.

When connected as a unity gain follower, the NCS2001 can directly drive capacitive loads in excess of 820 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under−damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 820 pF, it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in Figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to Figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 Ω. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.



Isolation resistor R = 50 to 500

Figure 31. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.

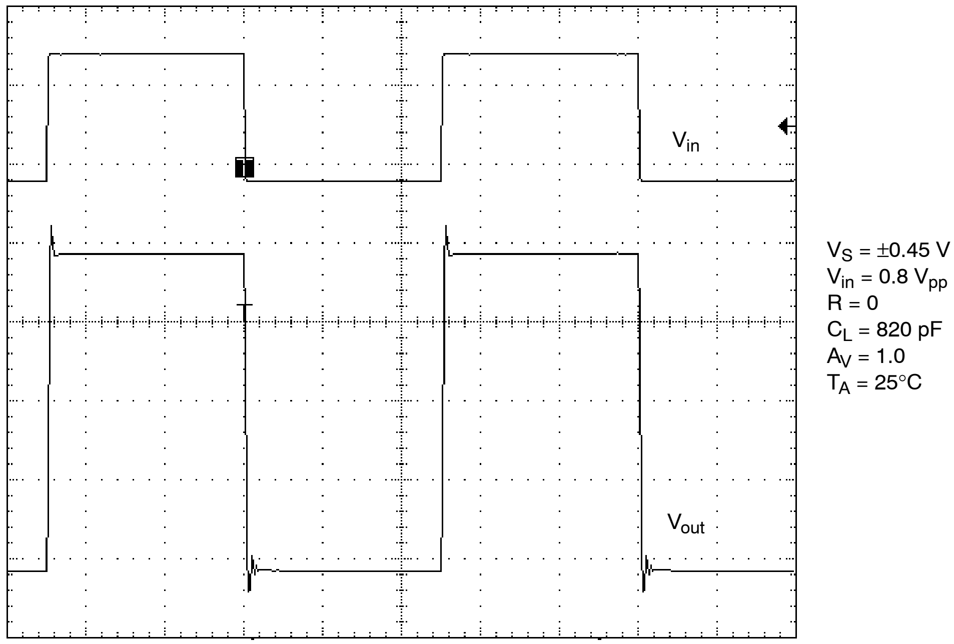


Figure 32. Small Signal Transient Response with Large Capacitive Load

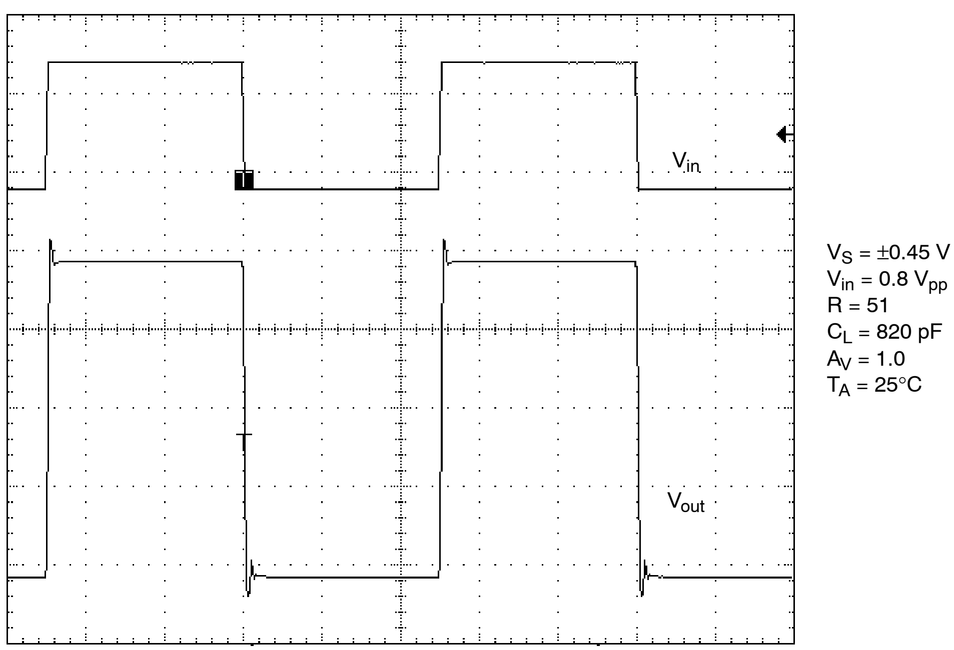
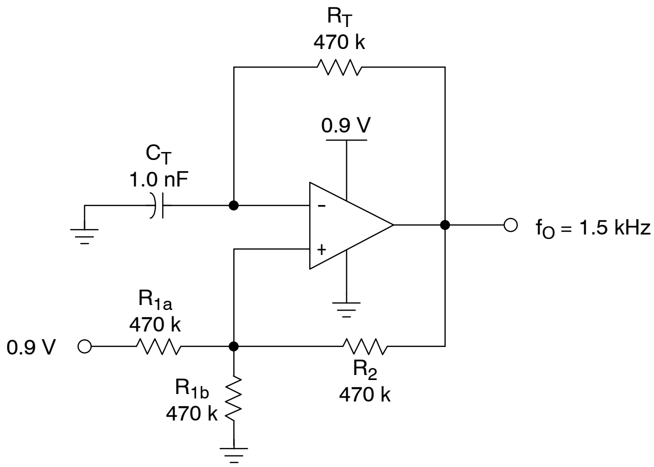
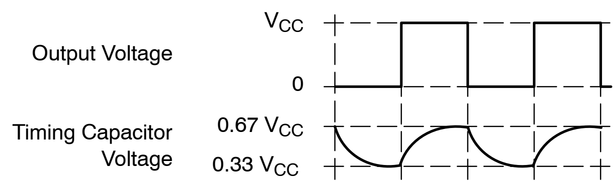


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor

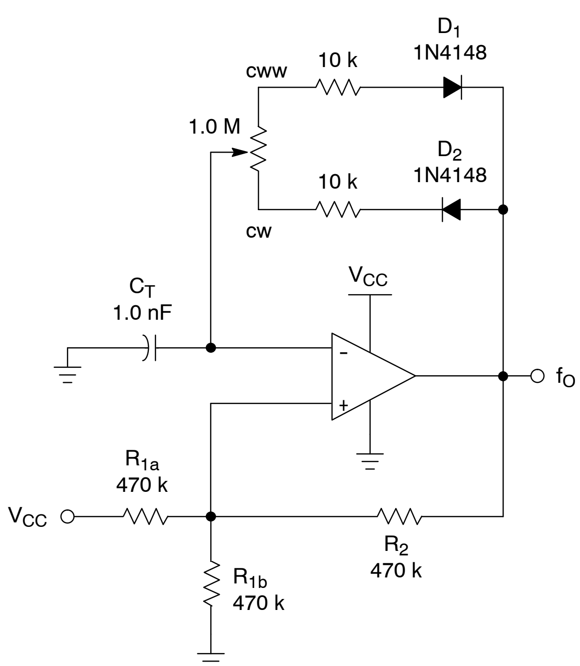


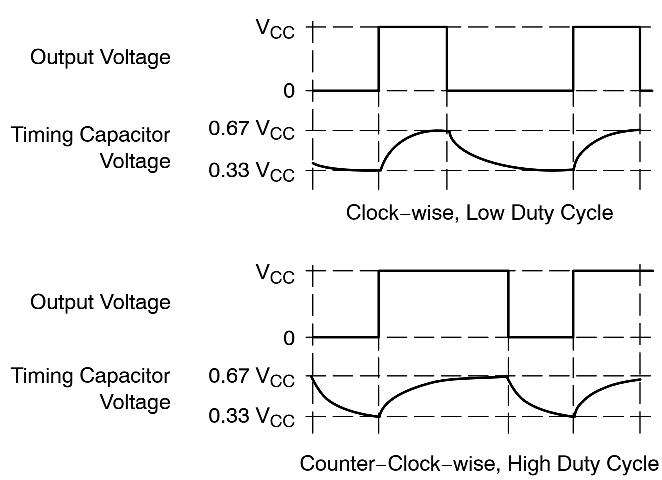


The non−inverting input threshold levels are set so that the capacitor voltage oscillates between 1/3 and 2/3 of V_{CC}. This requires the resistors R_{1a}, R_{1b} and R_2 to be of equal value. The following formula can be used to approximate the output frequency.

$$f_O = \frac{1}{1.39\ R_T C_T}$$

Figure 34. 0.9 V Square Wave Oscillator





The timing capacitor C_T will charge through diode D_2 and discharge through diode D_1, allowing a variable duty cycle. The pulse width of the signal can be programmed by adjusting the value of the trimpot. The capacitor voltage will oscillate between 1/3 and 2/3 of V_{CC}, since all the resistors at the non−inverting input are of equal value.

Figure 35. Variable Duty Cycle Pulse Generator

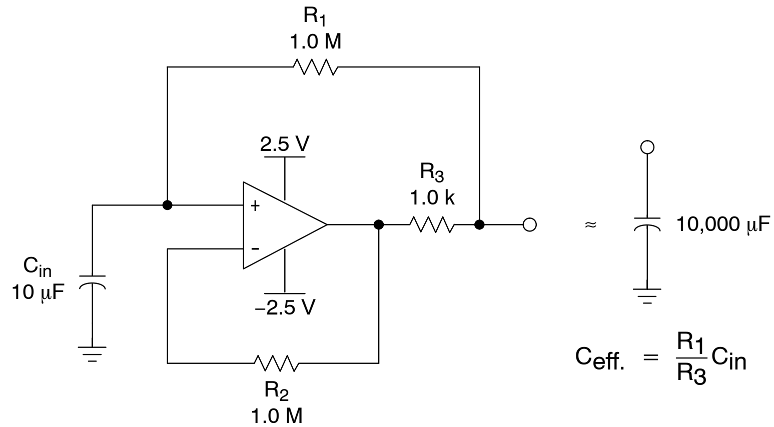


Figure 36. Positive Capacitance Multiplier

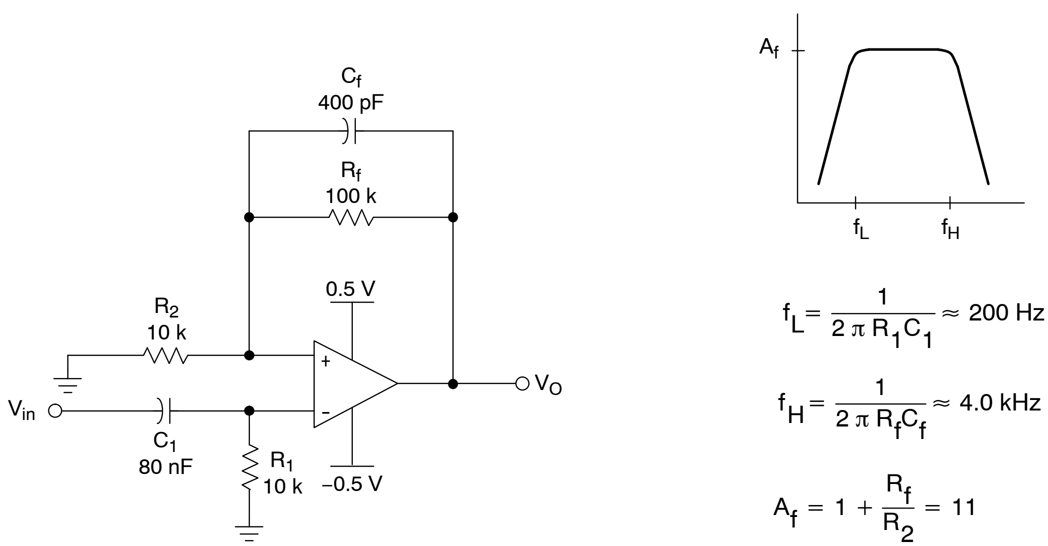


Figure 37. 1.0 V Voiceband Filter

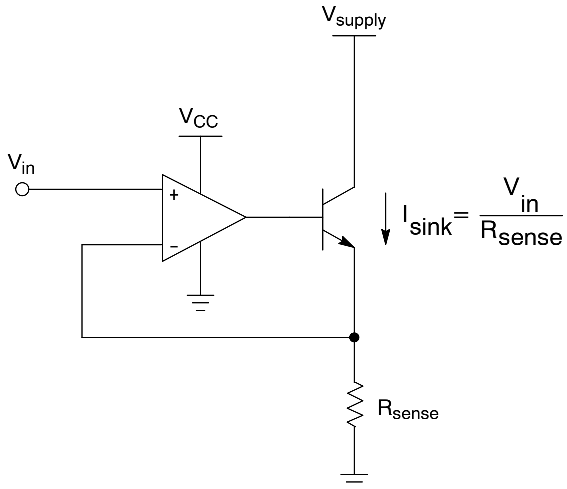
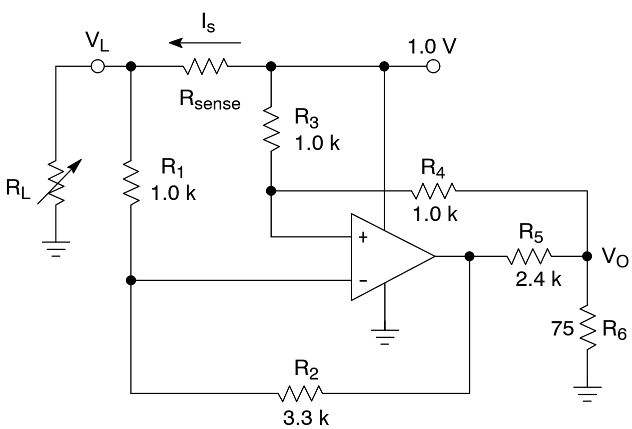


Figure 38. High Compliance Current Sink



I_s	V_O
435 mA	34.7 mV
212 mA	36.9 mV

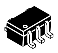
For best performance, use low tolerance resistors.

Figure 39. High Side Current Sense

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCS2001SN1T1G	AAG	SOT23−5 (Pb−Free)	3000 / Tape & 7” Reel
NCS2001SN2T1G	AAH		
NCV2001SN2T1G*	MBB		
NCS2001SQ2T2G	AAJ	SC70−5 (Pb−Free)	
NCV2001SQ2T2G*	AAJ		

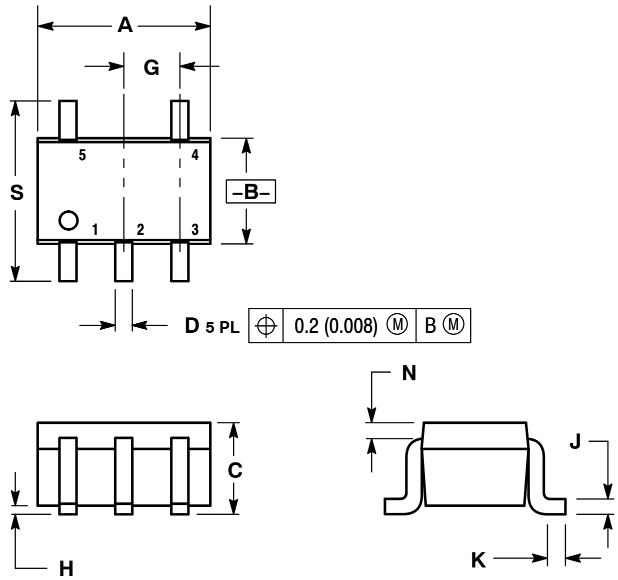
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



SCALE 2:1

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

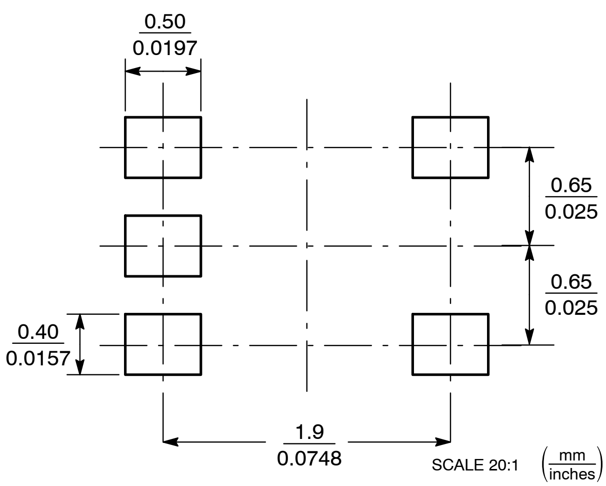
DATE 17 JAN 2013



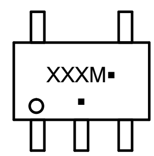
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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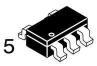

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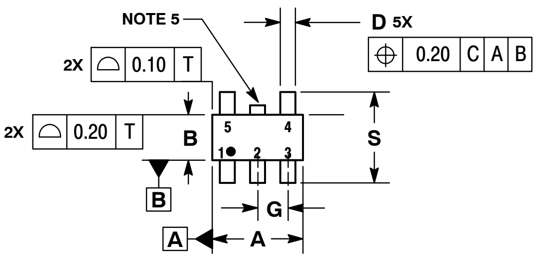
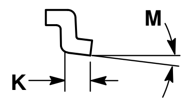
TSOP−5
CASE 483
ISSUE N

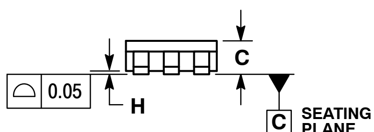
DATE 12 AUG 2020



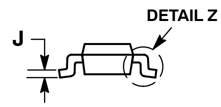
TOP VIEW



DETAIL Z



SIDE VIEW

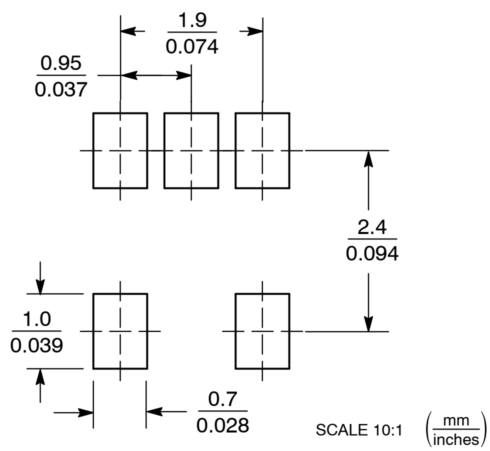


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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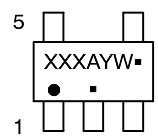
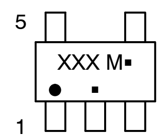


Analog



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A = Assembly Location	M = Date Code
Y = Year	▪ = Pb−Free Package
W = Work Week	
▪ = Pb−Free Package	

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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