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NCS2211, NCV2211

Low Distortion Audio Power Amplifier with Differential Output and Shutdown Mode

Product Description

The NCS2211 is a high performance, low distortion Class A/B audio amplifier. It is capable of delivering 1 W of output power into an 8 Ω speaker bridge−tied load (BTL). The NCS2211 will operate over a wide temperature range, and it is specified for single−supply voltage operation for portable applications.

It features low distortion performance, 0.2% typical THD + N @ 1 W and incorporates a shutdown/enable feature to extend battery life. The shutdown/enable feature will reduce the quiescent current to 1 μA maximum.

The NCS2211 is designed to operate over the −40°C to +85°C temperature range, and is available in an 8−lead SOIC package and a 3 X 3 mm DFN8 package. The SOIC package is pin compatible with equivalent function and comparable performance to competitive devices as is the DFN8 package. The DFN8 has a low thermal resistance of only 70°C/W plus has an exposed metal pad to facilitate heat conduction to copper PCB material.

Low distortion, high power, low quiescent current, and small packaging makes the NCS2211 suitable for applications including notebook and desktop computers, PDA's, and speaker phones.

Features

- Differential Output
- 1.0 W into an 8 Ω Speaker
- 1.5 W into a 4 Ω Speaker
- Single Supply Operation: 2.7 V to 5.5 V
- THD+N: 0.2% @ 1 W Output
- Low Quiescent Current: 20 mA Max
- Shutdown Current < 1.0 μA
- Excellent Power Supply Rejection
- Two Package Options: SOIC−8 Package and DFN8
- Pin Compatible with Competitive Devices
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Desktop Computers
- Notebook Computers
- PDA's
- Speaker Phones
- Games

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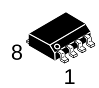
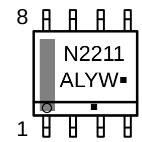
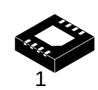
MARKING DIAGRAMS

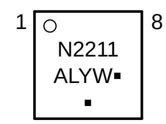


SOIC−8
D SUFFIX
CASE 751





DFN8
MN SUFFIX
CASE 506BJ



N2211	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

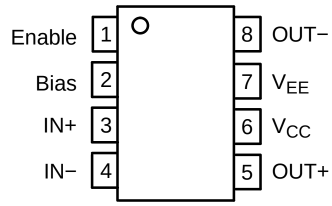
PIN	NAME	DESCRIPTION
1	Enable	Enable (LOW)/Shutdown (HIGH)
2	Bias	Bias Output at (V_{CC}−V_{EE})/2; Bypass with Capacitor to Reduce Noise
3	IN+	Non−Inverting Input
4	IN−	Inverting Input
5	OUT+	Output+
6	V_{CC}	Positive Supply (Bypass with 10 μF in parallel with 0.1 μF)
7	V_{EE}	Negative Supply (Connect to GND for Single−Supply Operation)
8	OUT−	Output−

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

May, 2014 − Rev. 3
Publication Order Number:
NCS2211/D

PIN CONNECTIONS for SOIC−8 and DFN8



(Top View)

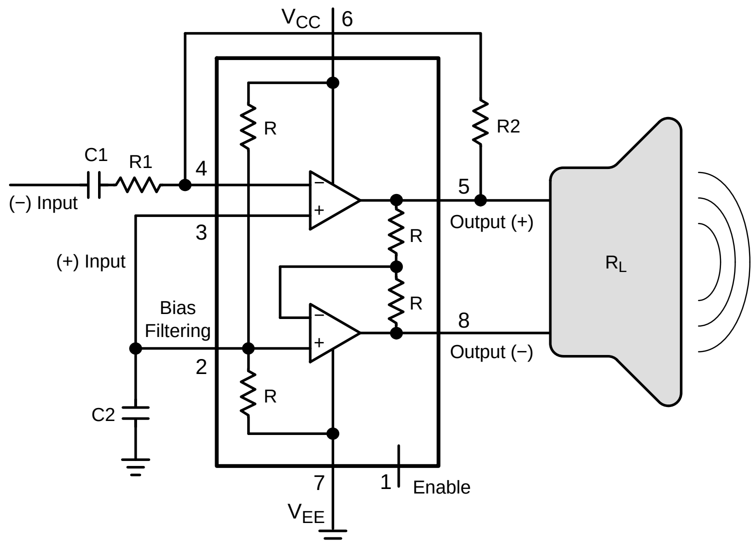


Figure 1. Block Diagram

	High	Low
Enable (Note 1)	Shutdown	Enabled

1. Enable (pin 1) must be actively driven for proper operation and cannot be left floating. See ENABLE/SHUTDOWN CONTROL in the specification table for proper logic threshold levels.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltages	V_{CC}	5.5	Vdc
Output Current	I_O	500	mA
Maximum Junction Temperature (Note 2)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air − SOIC−8 − DFN8 (Note 4)	θ_{JA}	117 70	°C/W
Moisture Sensitivity (Note 3)		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. For additional information, see Application Note AND8003/D
4. As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5 V, A_{VD} = 2, R_L = 8 Ω, C2 = 0.1 μF, T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.7		5.5	V
$I_{S, ON}$	Power Supply Current − Enabled	V_{CC} = 2.7 V to 5.5 V T_A = −40°C to +85°C (Note 5)			20	mA
$I_{S, OFF}$	Power Supply Current − Shutdown	V_{CC} = 2.7 V to 5.5 V			1.0	μA
PSRR	Power Supply Rejection Ratio	V_{CC} = 2.7 V to 5.5 V T_A = −40°C to +85°C		75		dB
ENABLE/SHUTDOWN CONTROL						
V_{IH}	Enable Input High	Device Shutdown V_{CC} = 2.7 V to 5.5 V	90% X V_{CC}		V_{CC}	V
V_{IL}	Enable Input Low	Device Enabled V_{CC} = 2.7 V to 5.5 V	GND		10% x V_{CC}	V
OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	From Either Output to GND R_L = 8 Ω		V_{CC} − 0.400		V
V_{OL}	Output Low Voltage	From Either Output to GND R_L = 8 Ω		0.400		V
V_{out} −off	Differential Output Offset Voltage	V_{CC} = 2.7 V to 5.5 V (Note 5) T_A = −40°C to +85°C			±50	mV
I_O	Output Current	Output to Output		350		mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5 V, A_{VD} = 2, R_L = 8 Ω, C2 = 0.1 μF, T_A = 25°C, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
GBW	Gain Bandwidth Product			12		MHz
	Phase Margin	A_{VD} = +2, R_L = 8 Ω, V_{CC} = 5 V		80		°
THD+N	Total Harmonic Distortion	V_{CC} = 5 V, f = 1 kHz, P = 1.0 W into 8 Ω V_{CC} = 5 V, f = 1 kHz, P = 0.5 W into 8 Ω V_{CC} = 3.3 V, f = 1 kHz, P = 0.35 W into 8 Ω V_{CC} = 2.7 V, f = 1 kHz, P = 0.25 W into 8 Ω		0.2 0.15 0.1 0.1		%
TIME DOMAIN RESPONSE						
t_{ON}	Turn on delay	V_{CC} = 5 V		1		μs
t_{OFF}	Turn off delay	V_{CC} = 5 V		4		μs

5. Guaranteed by design and/or characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

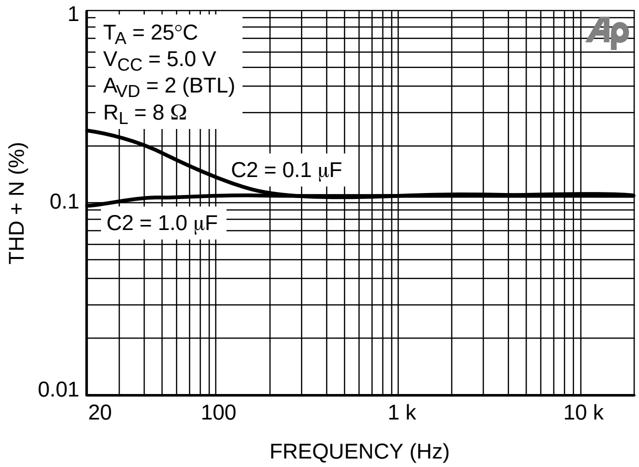


Figure 2. THD + N vs. Frequency (P_L = 500 mW)

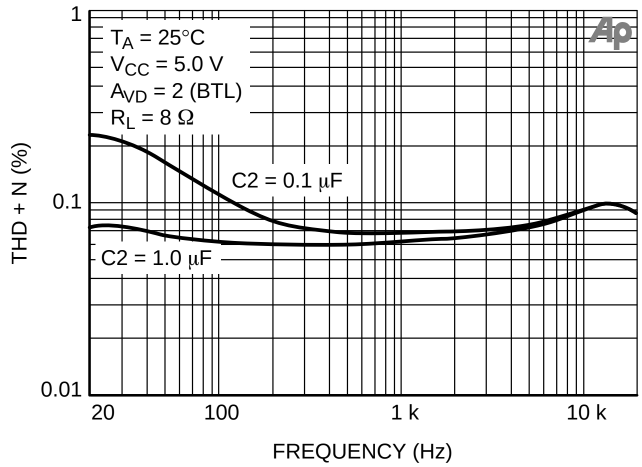


Figure 3. THD + N vs. Frequency (P_L = 1 W)

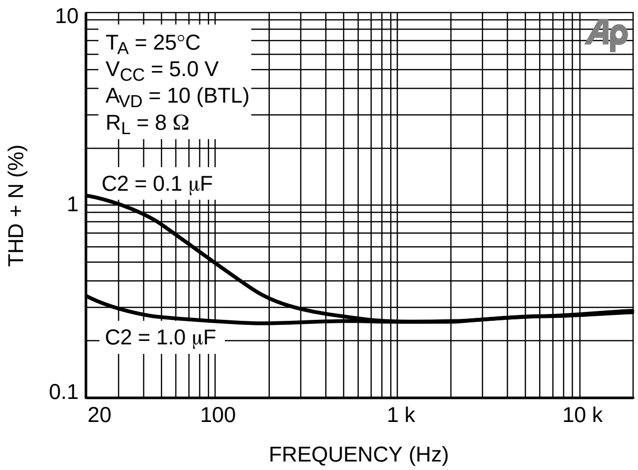


Figure 4. THD + N vs. Frequency (P_L = 500 mW)

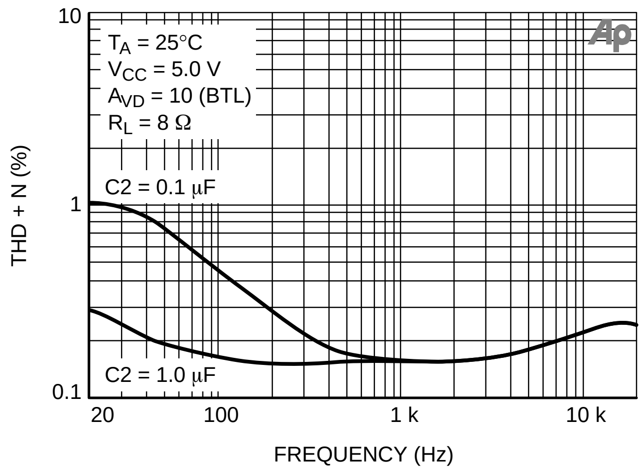


Figure 5. THD + N vs. Frequency (P_L = 1 W)

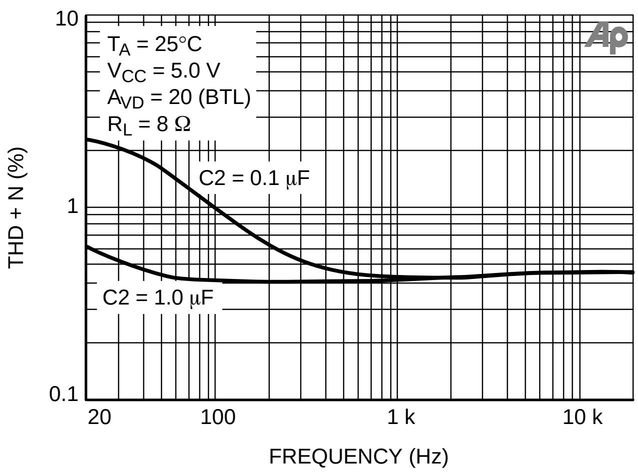


Figure 6. THD + N vs. Frequency (P_L = 500 mW)

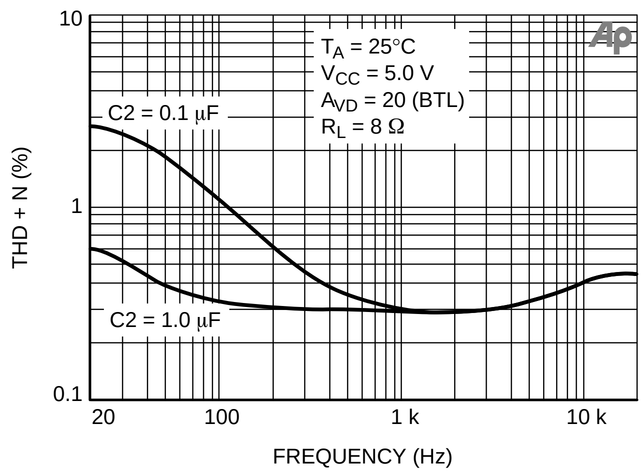


Figure 7. THD + N vs. Frequency (P_L = 1 W)

TYPICAL PERFORMANCE CHARACTERISTICS

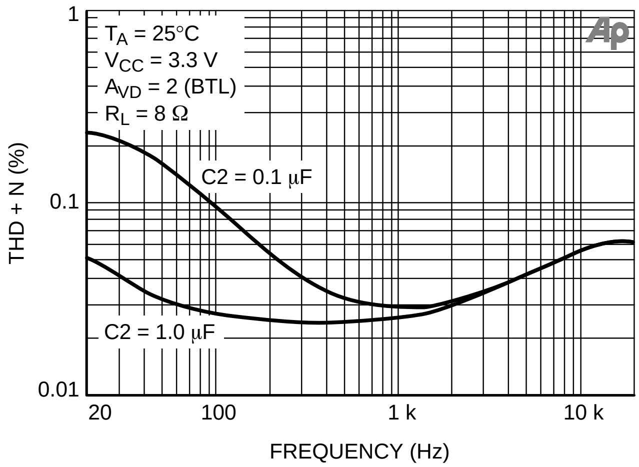


Figure 8. THD + N vs. Frequency (P_L = 350 mW)

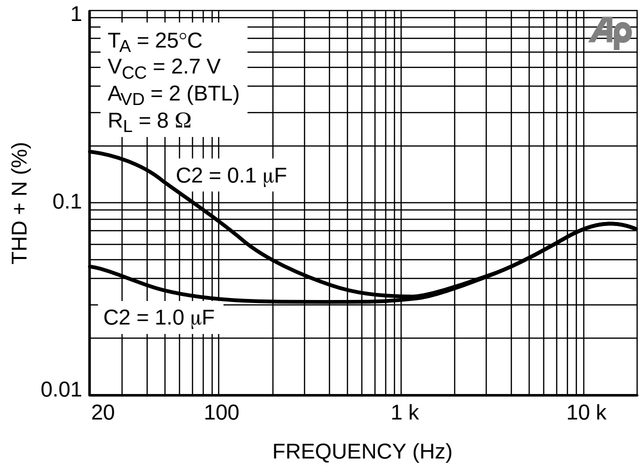


Figure 9. THD + N vs. Frequency (P_L = 250 mW)

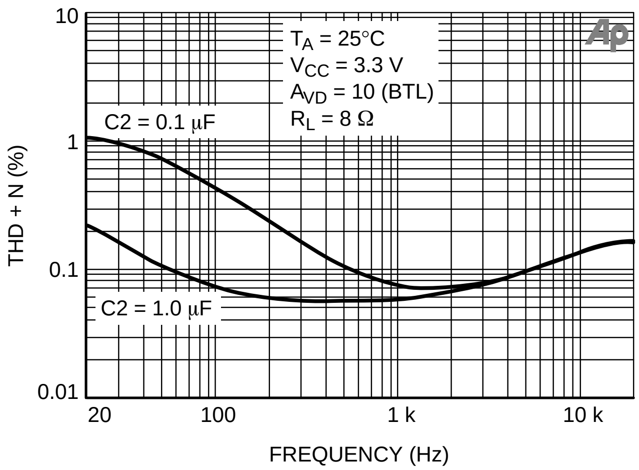


Figure 10. THD + N vs. Frequency (P_L = 350 mW)

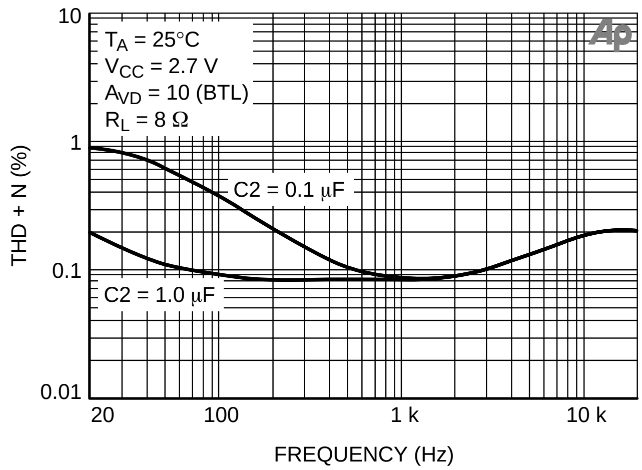


Figure 11. THD + N vs. Frequency (P_L = 250 mW)

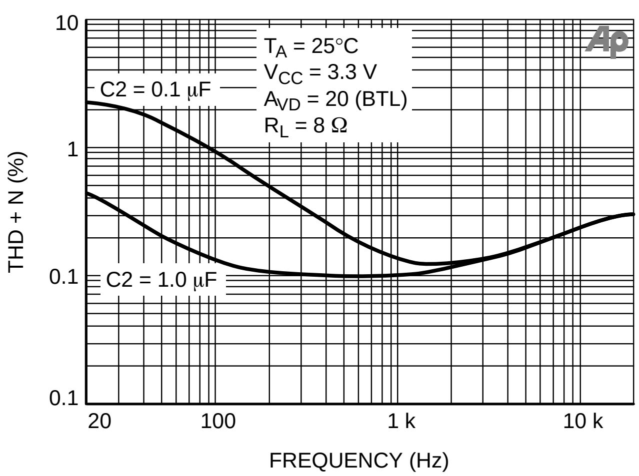


Figure 12. THD + N vs. Frequency (P_L = 350 mW)

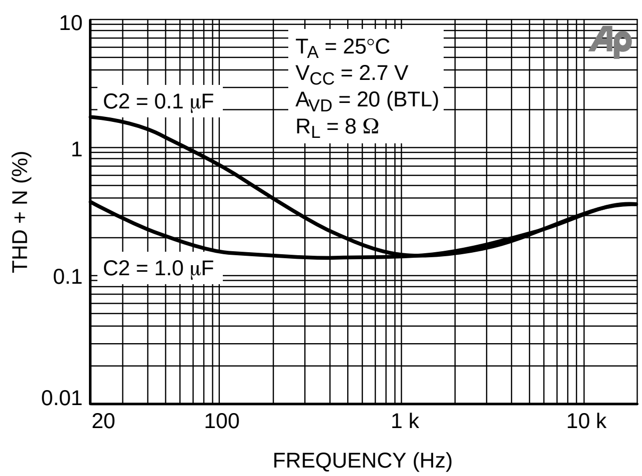


Figure 13. THD + N vs. Frequency (P_L = 250 mW)

TYPICAL PERFORMANCE CHARACTERISTICS

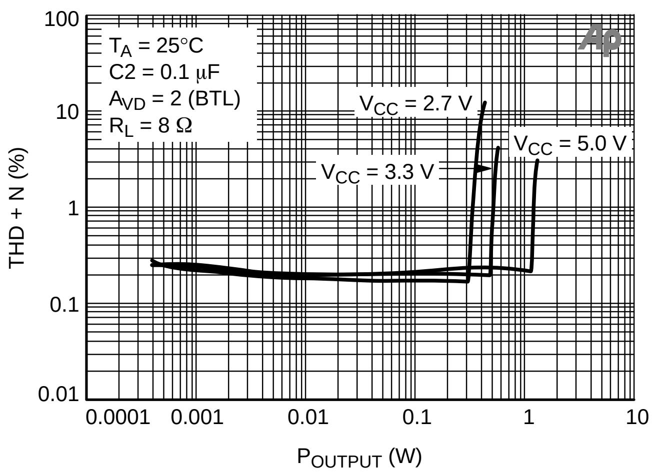


Figure 14. THD + N vs. P_{OUTPUT} (Frequency = 20 Hz)

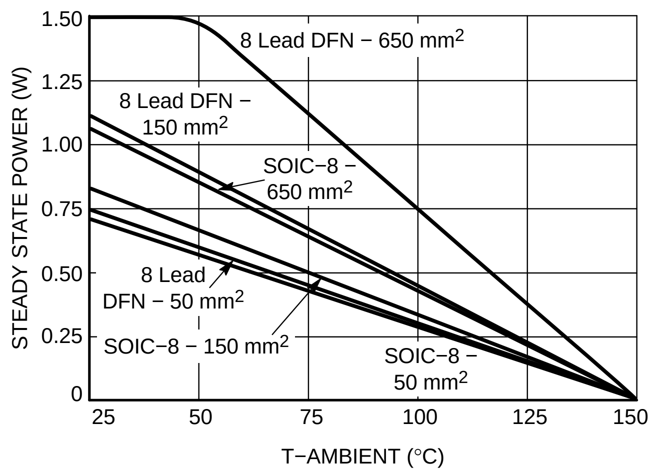


Figure 15. SOA Curve with PCB Copper Thickness 2 oz and Various Areas

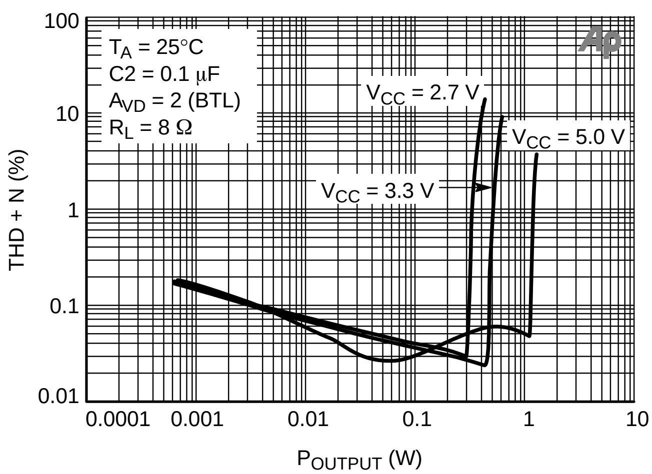


Figure 16. THD + N vs. P_{OUTPUT} (Frequency = 1 kHz)

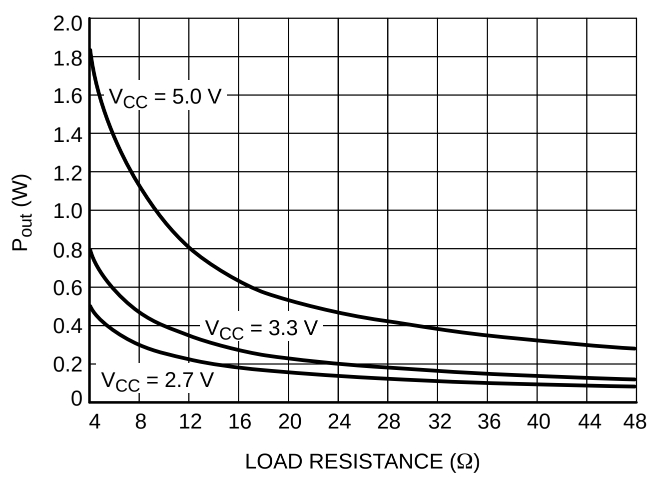


Figure 17. P_{out} vs. Load Resistance

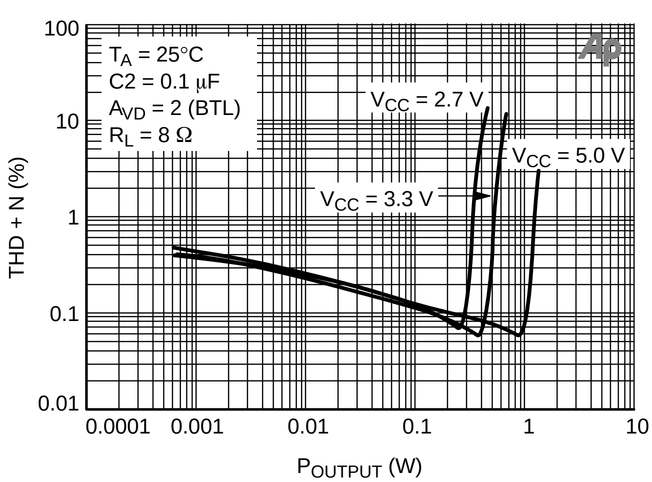


Figure 18. THD + N vs. P_{OUTPUT} (Frequency = 20 kHz)

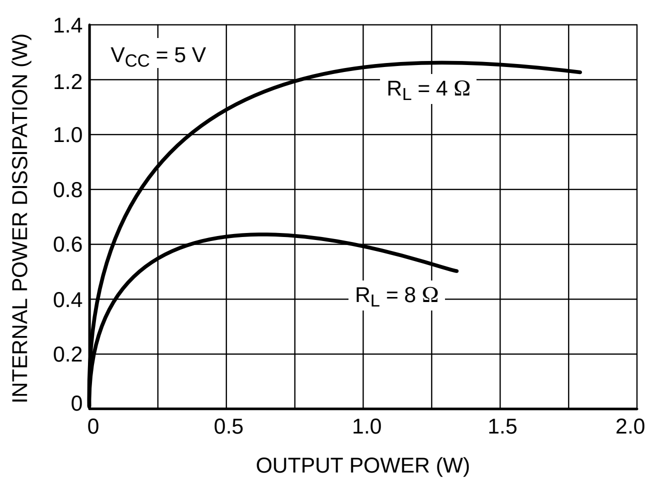


Figure 19. Power Dissipation vs. Output Power

TYPICAL PERFORMANCE CHARACTERISTICS

Channel 1: Enable Logic and OUT+ and OUT−

Channel 2: Differential Output

Time Base: 1 μSec per Division

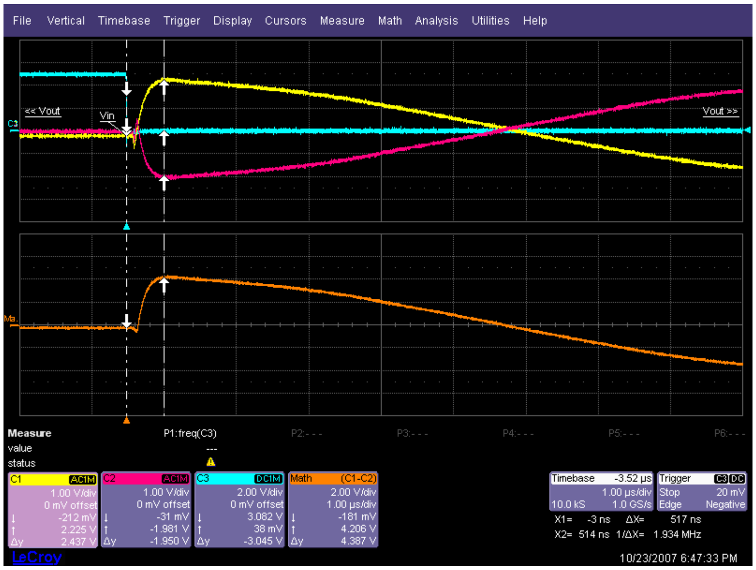


Figure 20. Turn−on Time

Channel 1: SHUTDOWN Logic and OUT+ and OUT−

Channel 2: Differential Output

Time Base: 5 μSec per Division

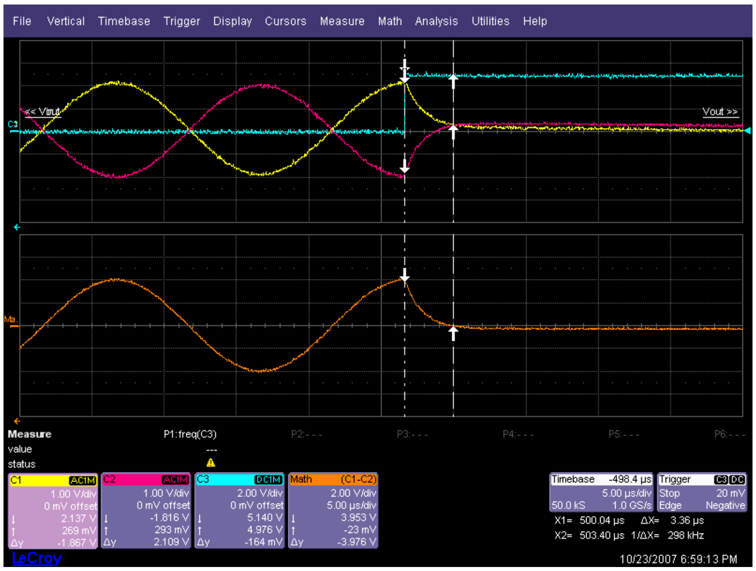


Figure 21. Turn−off Time

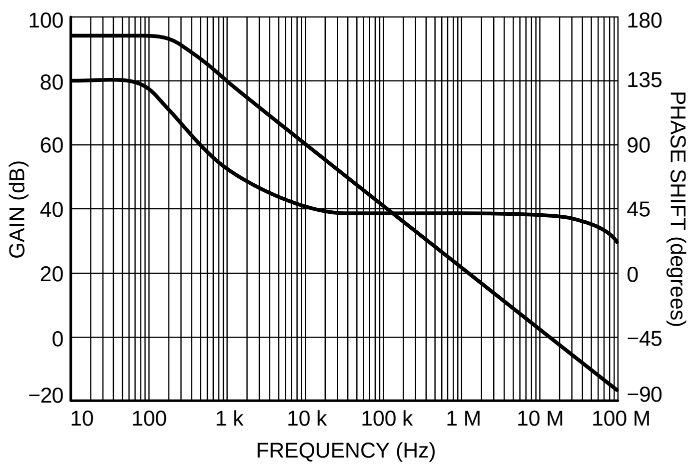


Figure 22. Gain and Phase Shift vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

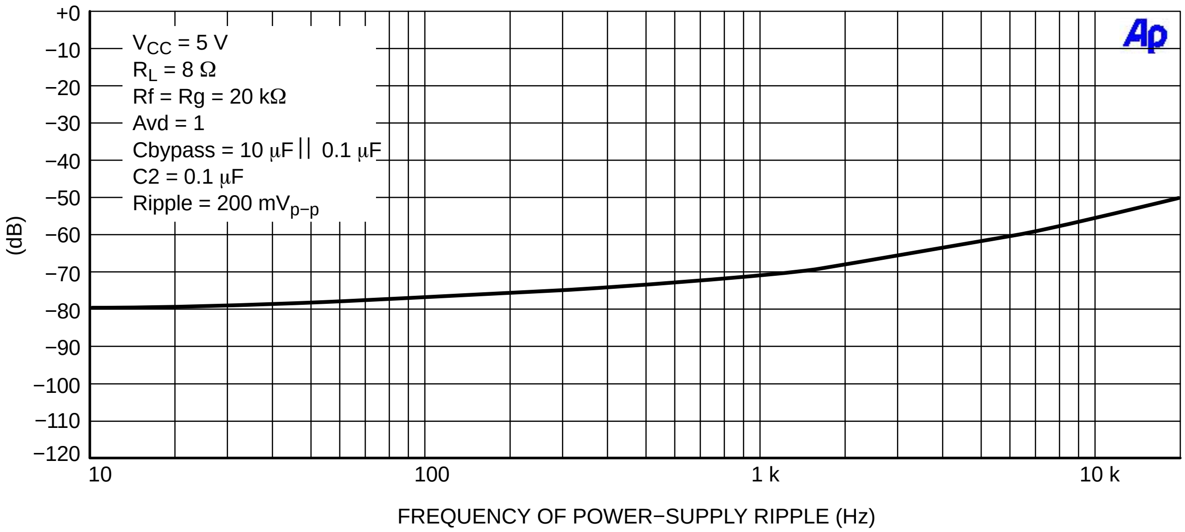


Figure 23. Power−Supply Rejection

APPLICATIONS INFORMATION

The NCS2211 is unity gain stable and therefore does not require any compensation, but a proper power−supply bypass is required as shown in Figure 24. Performance will be enhanced by adding a filter capacitor (C2) to the mid−supply node (pin 2). See Typical Performance Characteristics for details.

It is preferable to AC couple the input to avoid a large DC output offset.

Both outputs can be driven to within 400 mV of either supply rail with an 8 Ω load.

Typical Application of the Device:

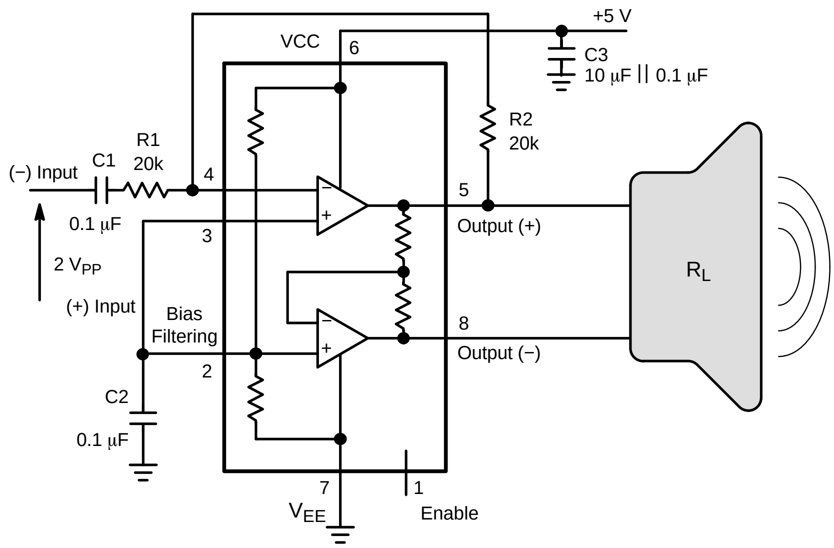


Figure 24.

THERMAL CONSIDERATIONS

Care must be taken to not exceed the maximum junction temperature of the device (150°C). Figure 15 shows the tradeoff between output power and junction temperature for different areas of exposed PCB copper (2 oz). If the maximum power is exceeded momentarily, normal circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in an “overheated” condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the SOA curves.

GAIN

Since the output is differential, the gain from input to the speaker is: A_{VD} = 2 x R2/R1. For low level input signals, THD will be optimized by pre−amplifying the signal and running the NCS2211 at gain A_{VD} = 2 and C2=1 μF.

BIAS FILTERING

Even though the NCS2211 will operate nominally with no filter capacitor on pin 2, THD performance will be improved dramatically with a filter capacitor installed (see Typical Performance Characteristics). In addition a C2 filter capacitor at pin 2 will suppress start−up popping noise. To insure optimal suppression the time constant of the bias filtering needs to be greater than the time constant of the input capacitive coupling circuit, that is C2 x 25 k > C1 x R1.

ORDERING INFORMATION

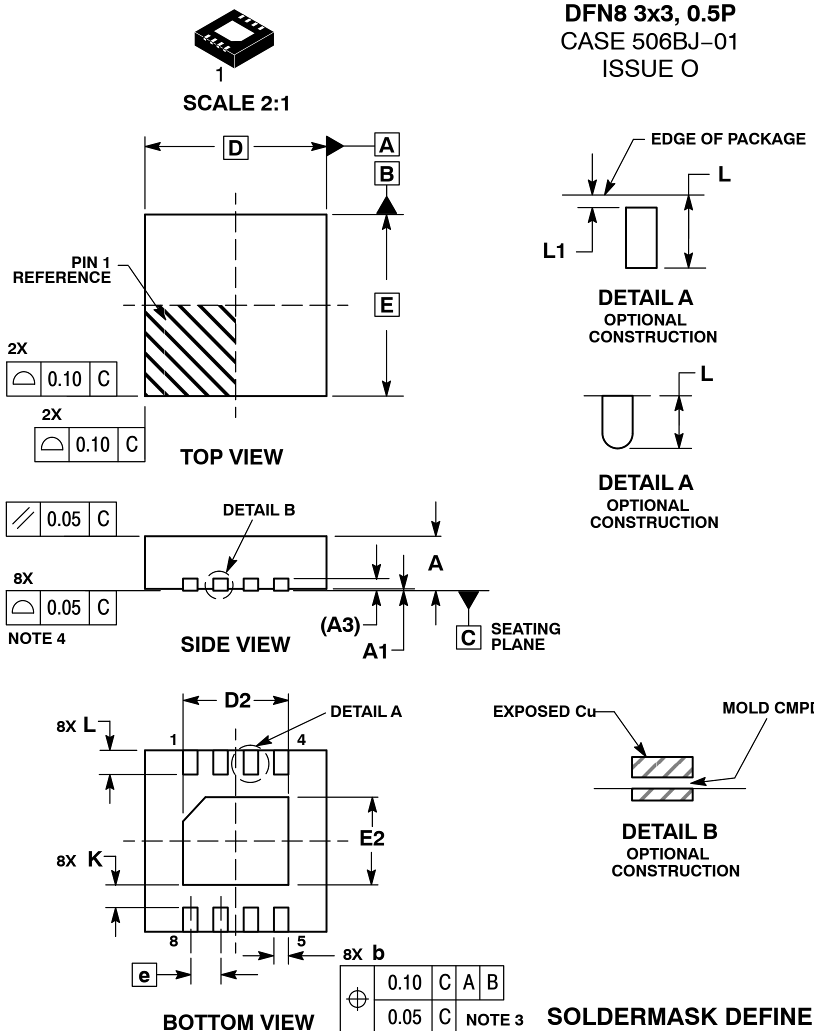
Device	Package	Shipping†
NCS2211DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2211DR2G*	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCS2211MNTXG	DFN−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

DFN8 3x3, 0.5P
CASE 506BJ−01
ISSUE O

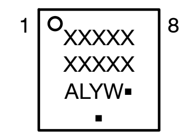
DATE 08 NOV 2007



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

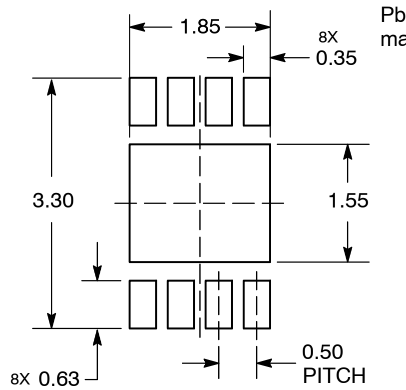
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 3X3, 0.5P	PAGE 1 OF 1

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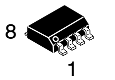
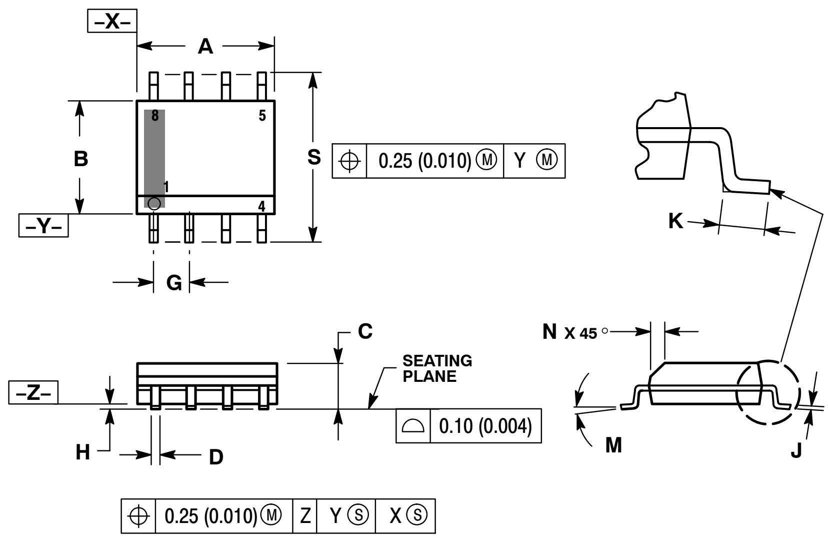


SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

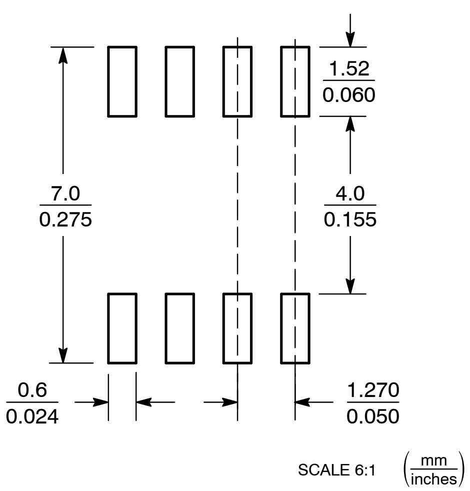
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

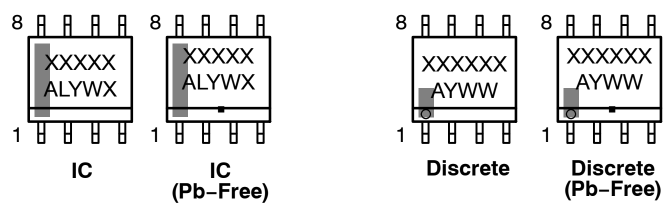
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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