NCS2563

Video Amplifier, 3-Channel, with High Definition Reconstruction Filters

Description

NCS2563 is a 3−Channel high speed video amplifier with 6th order Butterworth High Definition (HD) reconstruction filters and 6 dB gain.

All three channels can accommodate all Component and RGB video signals. All channels can accept DC or AC coupled signals. If AC coupled, the internal clamps are employed. The outputs can drive both AC and DC coupled 150 Ω loads.

It is designed to be compatible with most Digital−Analog Converters (DAC) embedded in most video processors.

Features

- Three 6th Order High Definition 30 MHz Filter
- Internally Fixed Gain = 6 dB
- Transparent Input Clamping for Each Channel
- DC or AC Coupled Inputs
- DC or AC Coupled Outputs
- Integrated Level Shifter
- Operating Voltage +5 V
- Available in SOIC−8 Package
- These are Pb−Free Devices

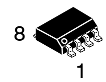
Applications

- Digital Set−Top Box
- DVD and Video Players
- HDTV
- Video−On−Demand (VOD)

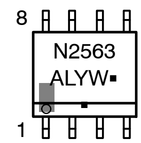
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM*



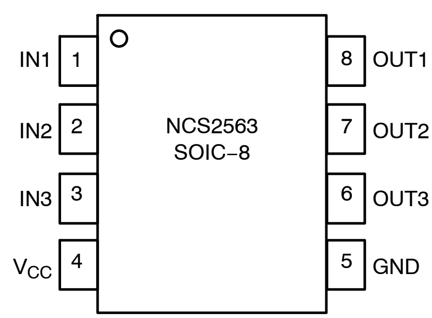
SOIC−8
D SUFFIX
CASE 751



A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
NCS2563DG	SOIC−8 (Pb−Free)	98 Units / Rail
NCS2563DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	IN1	Input	Video Input 1 for Video Signal featuring a frequency bandwidth compatible with High Definition Video (30 MHz) − Channel 1
2	IN2	Input	Video Input 2 for Video Signal featuring a frequency bandwidth compatible with High Definition Video (30 MHz) − Channel 2
3	IN3	Input	Video Input 3 for Video Signal featuring a frequency bandwidth compatible with High Definition Video (30 MHz) − Channel 3
4	VCC	Power	Device Power Supply Voltage: +5 V
5	GND	GND	Connected to Ground
6	OUT3	Output	HD Video Output 3 − Channel 3
7	OUT2	Output	HD Video Output 2 − Channel 2
8	OUT1	Output	HD Video Output 1 − Channel 1

ATTRIBUTES

Characteristics		Value
ESD		
Human Body Model	All Pins (Note 1)	8 kV
Machine Model	Pins 1 to 5 (Note 2)	400 V
	All Output Pins (Note 2)	600 V
Moisture Sensitivity (Note 3)		Level 1
Flammability Rating − Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in

1. Human Body Model (HBM): R = 1500 Ω, C = 100 pF
2. Machine Model (MM)
3. For additional information, see Application Note AND8003/D.

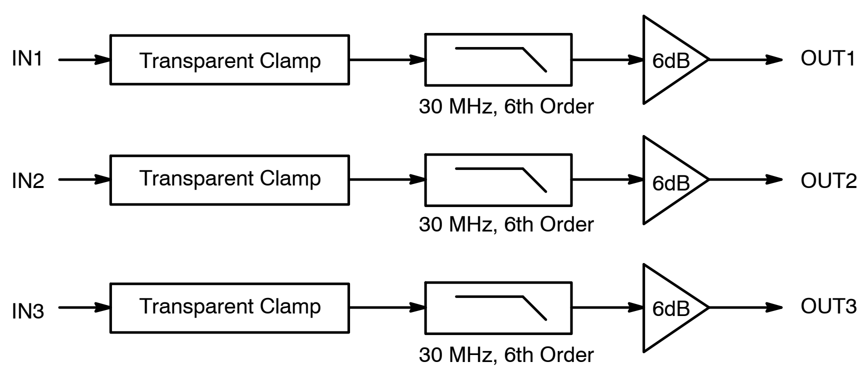


Figure 1. Block Diagram

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltages	V_{CC}	$-0.35 \le V_{CC} \le 5.5$	Vdc
Input Voltage Range	V_I	$-0.3 \le V_I \le V_{CC}$	Vdc
Input Differential Voltage Range	V_{ID}	$V_I \le V_{CC}$	Vdc
Output Current	I_O	50	mA
Maximum Junction Temperature (Note 4)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	112.7	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Maximum Power Dissipation

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves.

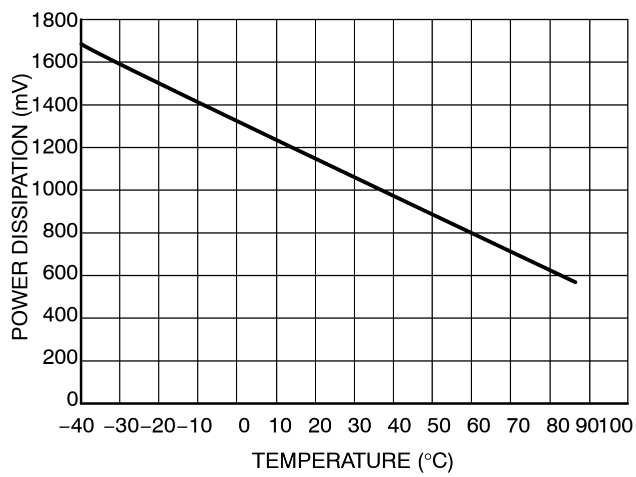


Figure 2. Power Dissipation vs Temperature

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, T_A = 25°C, 0.1 μF AC coupled inputs, R_{source} = 37.5 Ω, 220 μF AC coupled outputs into 150 Ω load, referenced to 400 kHz, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range		4.75	5	5.25	V
I_{CC}	Power Supply Current			22	33	mA
V_{IN}	Input Common Mode Voltage Range		GND		1.4	V
V_{OH}	Output High Voltage			2.8		V
V_{OL}	Output Low Voltage			280		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, T_A = 25°C, 0.1 μF AC coupled inputs, R_{source} = 37.5 Ω,220 μF AC coupled outputs into 150 Ω load, referenced to 400 kHz, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
A_{VOL}	Voltage Gain (Note 5)	V_{IN} = 1 V	5.8	6.0	6.2	dB
BW	Bandwidth of Low Pass Filter	−1 dB −3 dB	23	30 33		MHz
A_R	Attenuation (Stopband Reject)	f = 44.25 MHz f = 74.25 MHz	 28	14.5 36		
dG	Differential Gain	A_V = +2, R_L = 150 Ω		0.2		%
dP	Differential Phase	A_V = +2, R_L = 150 Ω		0.1		°
THD	Total Harmonic Distortion	V_{OUT} = 1.4 V_{PP}, f = 10 MHz V_{OUT} = 1.4 V_{PP}, f = 15 MHz V_{OUT} = 1.4 V_{PP}, f = 22 MHz		0.2 0.4 1.2		%
x_{talk}	Channel−to−Channel Crosstalk	V_{IN} = 1.4 V_{PP}, f = 1 MHz		60		dB
SNR	Signal to Noise Ratio* (Note 6)	100% White Signal, 100 kHz to 30 MHz		65		dB
t_{PD}	Propagation Delay	Input to Output		20		ns
ΔTg	Group Delay Variation*	100 kHz to 30 MHz		6		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Guaranteed by design

5. 100% of tested IC fit to the bandwidth tolerance.
6. SNR = 20 x log (714 mV/RMS noise)

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5 V, R_{source} = 37.5 Ω, 0.1 μF AC−Coupled Inputs, 220 μF AC−Coupled Outputs with 150 Ω

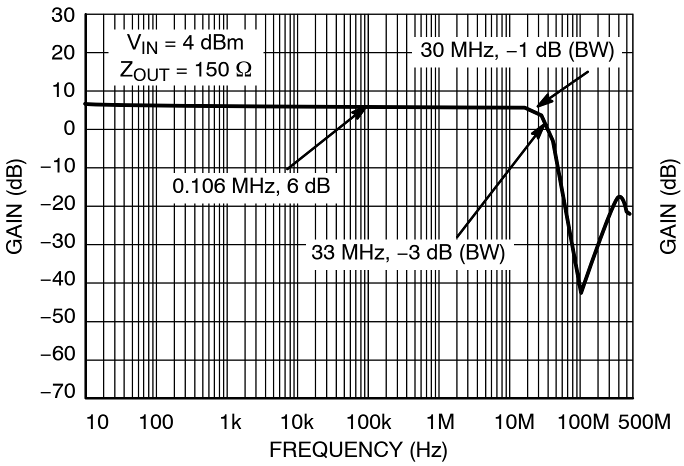


Figure 3. Gain vs. Frequency

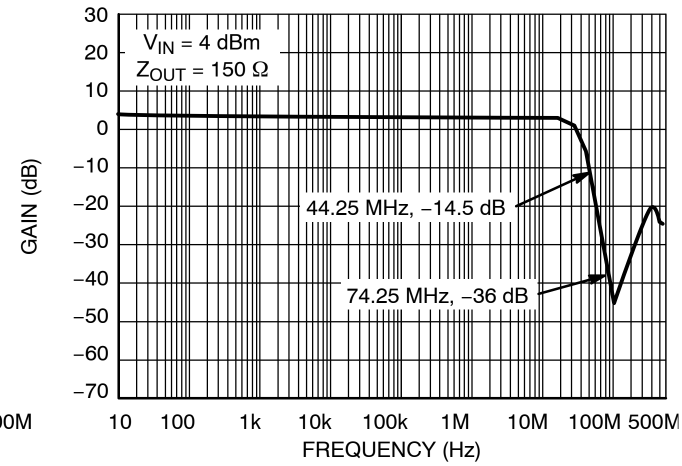


Figure 4. Attenuation

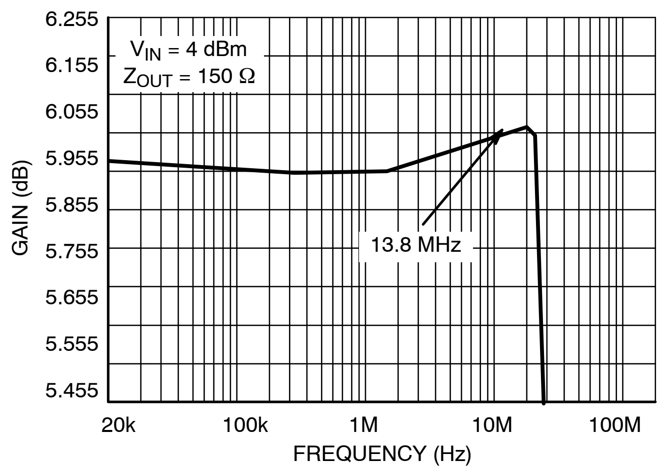


Figure 5. Flatness Bandwidth 0.1 dB

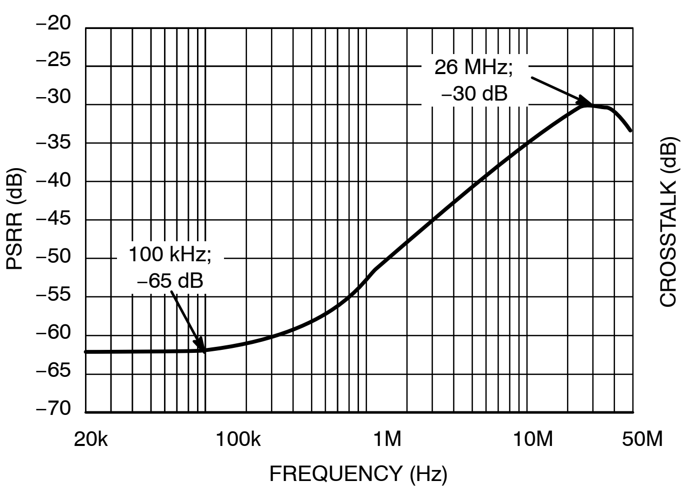


Figure 6. PSRR vs. Frequency (No Bypass Capacitor)

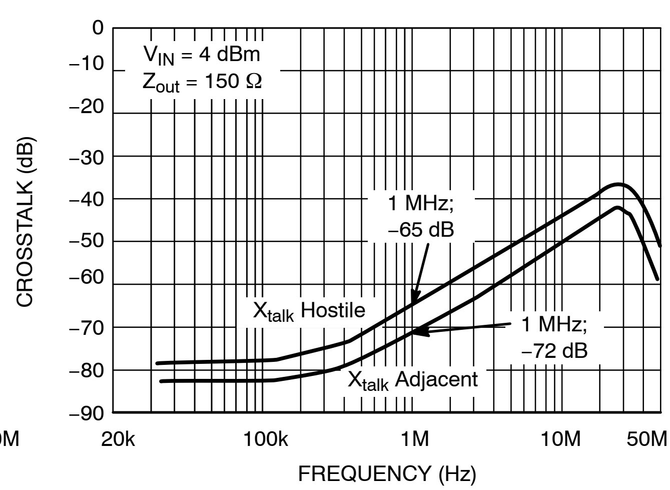


Figure 7. Crosstalk vs. Frequency, CH2/CH3 (100 μF AC−Coupled Input, DC−Coupled Output)

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5 V, R_{source} = 37.5 Ω, 0.1 μF AC−Coupled Inputs, 220 μF AC−Coupled Outputs with 150 Ω

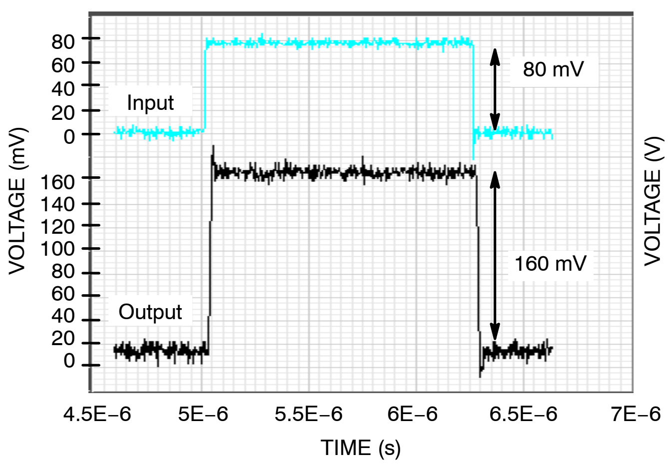


Figure 8. Small Signal Step Response
$T_r = T_f$ = 1 ns

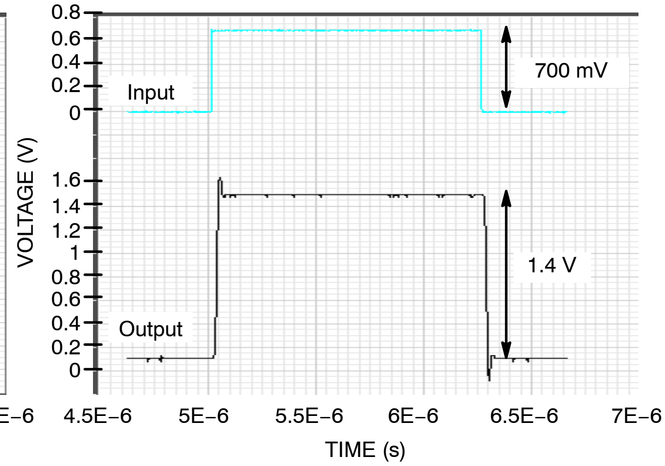


Figure 9. Large Signal Step Response
$T_r = T_f$ = 1.0 ns

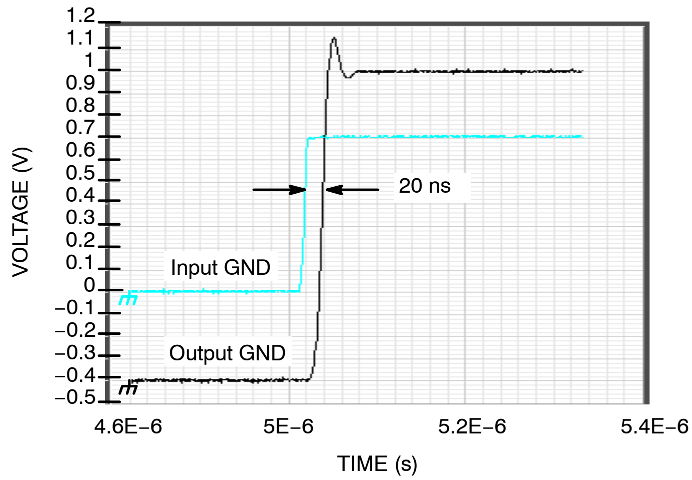


Figure 10. Propagation Delay vs. Time

APPLICATIONS INFORMATION

The NCS2563 triple video driver has been optimized for High Definition video applications covering the requirements of the standards 720p, 1080i and related (RGB). All the 3 channels feature the same specifications and similar behaviors guaranteed by a high channel−to−channel crosstalk isolation (down to 60 dB at 1 MHz). Each channel provides an internal voltage−to−voltage gain of 2 from its input to its output reducing by the way the number of external components usually needed in the case of some discrete approaches (using stand−alone op amps). An internal level shifter is employed shifting up the output voltage by adding an offset of about 280 mV. This avoids sync pulse clipping and allows DC−coupled output to the 150 Ω video load. In addition, the NCS2563 integrates a 6^{th} order Butterworth filter per channel with a 3 dB frequency bandwidth of 30 MHz. This allows rejecting out the aliases or unwanted over−sampling effects produced by the video DAC. It works the same way for DVD recorders using ADC, this anti−aliasing filter (reconstruction filter) will avoid picture quality issue and will help also to filter out parasitic signals caused by EMI interference.

A built−in diode−like clamp is used into the chip for each channel to support AC−coupled mode of operation. The clamp is active when the input signal goes below 0 V.

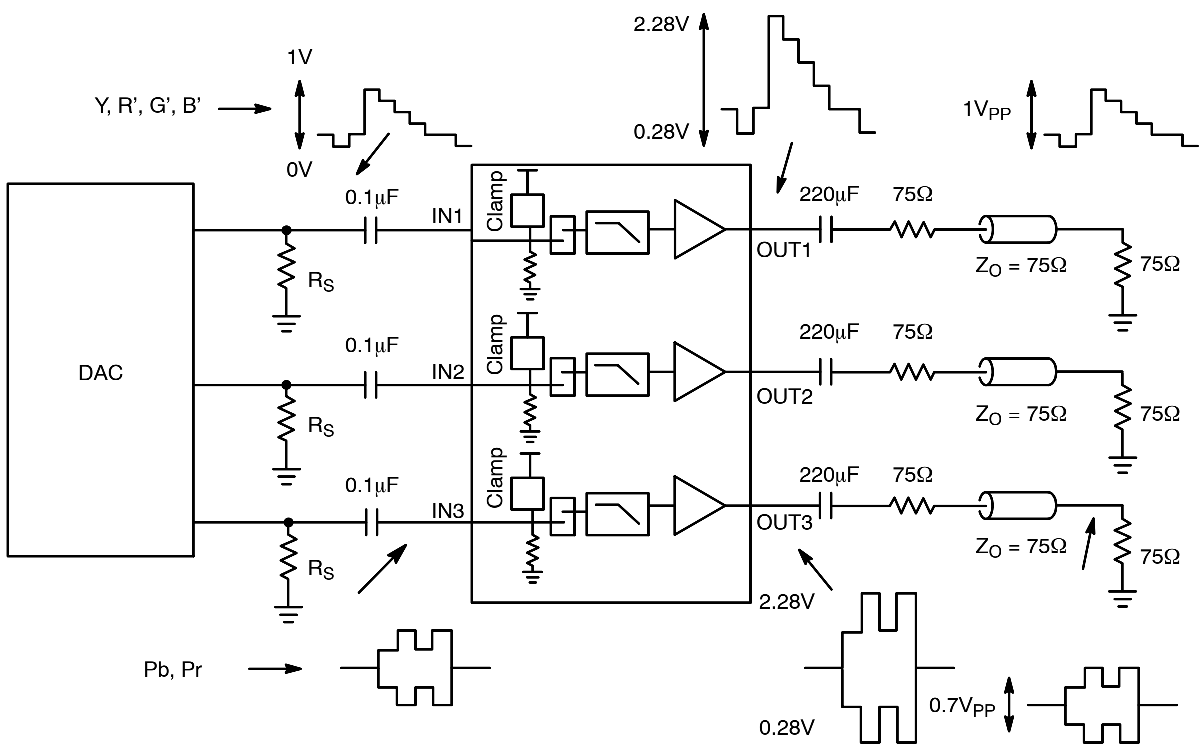


Figure 11. AC−Coupled Inputs and Outputs

Figure 11 shows an example for which the external video source coming from the DAC is AC−coupled at the input and output. But thanks to the built−in transparent clamp and level shifter the device can operate in different configuration modes depending essentially on the DAC output signal level High and Low and how it fits the input common mode voltage of the video driver. When the configuration is DC−Coupled at the Inputs and Outputs the 0.1 μF and 220 μF coupling capacitors are no longer used, the clamps are in that case inactive; this configuration has the big advantage of being relatively low cost with the use of less external components.

The input is AC−coupled if the input−signal amplitude goes over the range 0 V to 1.4 V or if the video source requires a coupling. In some circumstances it may be necessary to auto−bias signals by the addition of a pull−up and pull−down resistor or only pullup resistor (Typical 7.5 MΩ combined with the internal 800 kΩ pulldown) making the clamp inactive.

The output AC−coupling configuration has the advantage of eliminating DC ground loop with the drawback of making the device more sensitive to video line or field tilt issues in the case of a too low output coupling capacitor. In some cases it may be necessary to increase the nominal 220 μF capacitor value.

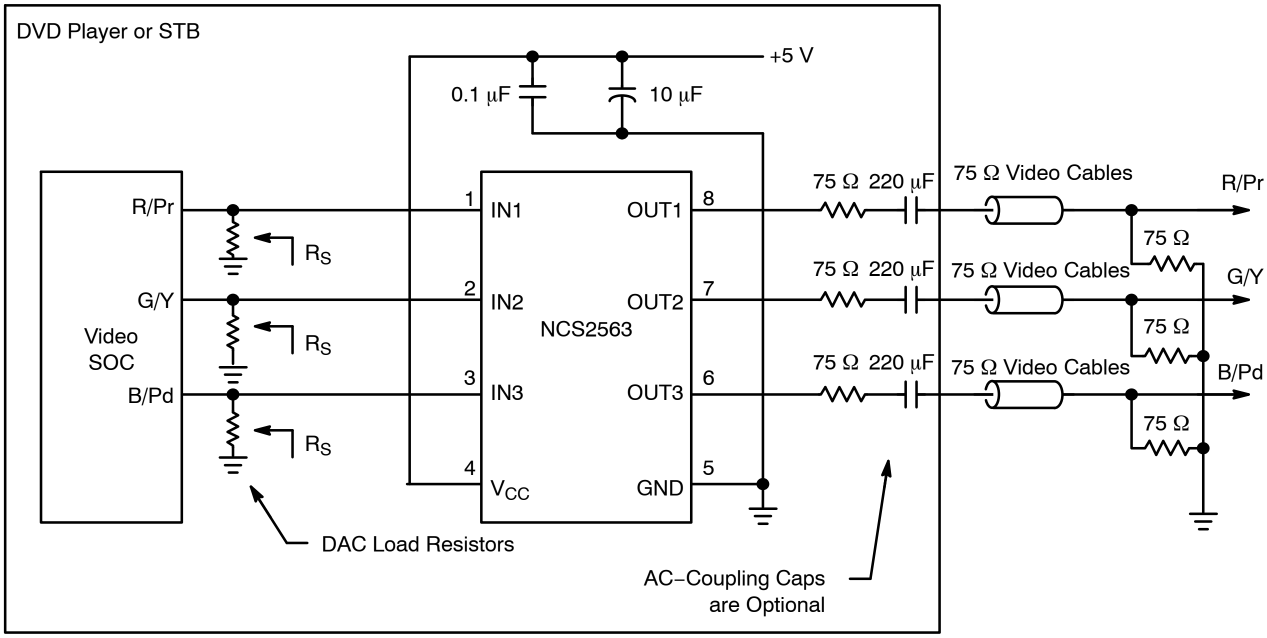
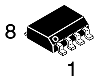


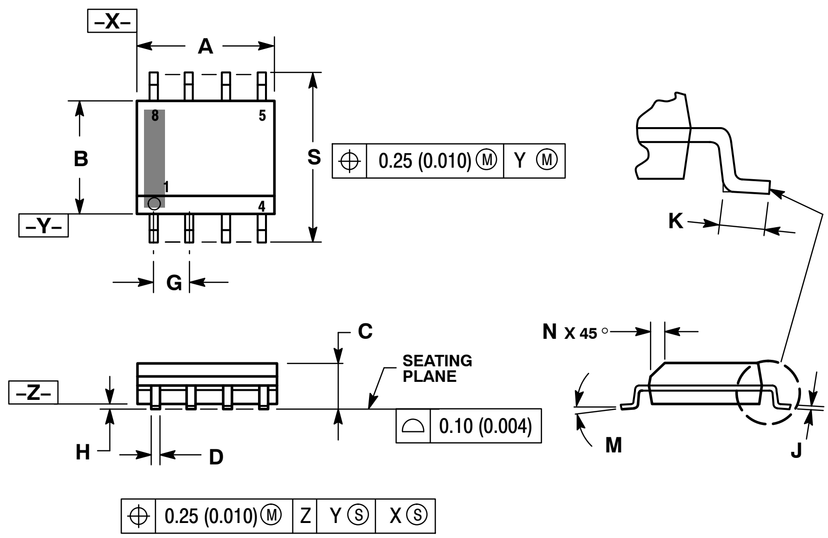
Figure 12. Typical Application Circuit



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

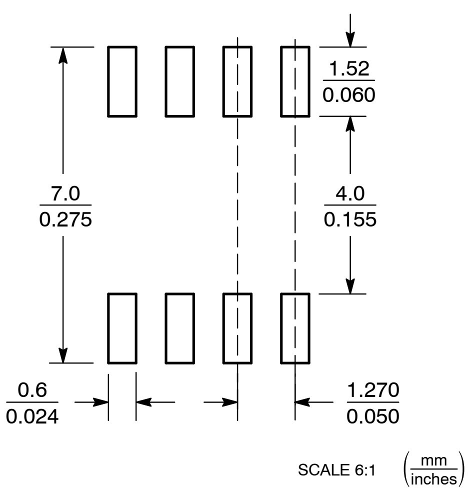
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

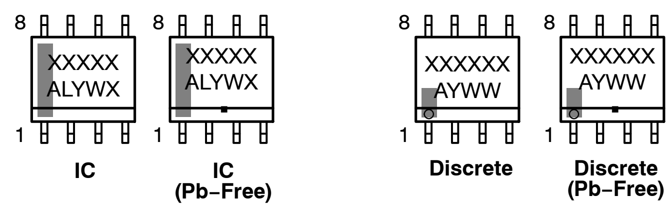
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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