NCV4290

Voltage Regulator - Low-Dropout, Power Good

5.0 V, 450 mA

The NCV4290 is an integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The output is regulated at 5.0 V and is rated to 450 mA of output current. It also provides a number of features, including overcurrent protection, overtemperature protection and a programmable microprocessor power good signal. The NCV4290 is available in the DPAK and D^{2}PAK surface mount packages. The output is stable over a wide output capacitance and ESR range.

Features

- 5.0 V, ±2% Output Voltage Options
- 450 mA Output Current
- Very Low Current Consumption
- Active Power Good Output
- Power Good Low Down to V_Q = 1.0 V
- 500 mV (max) Dropout Voltage
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit Protection
  - Thermal Overload Protection
- AEC−Q100 Qualified
- These are Pb−Free Devices

Applications

- Auto Body Electronics

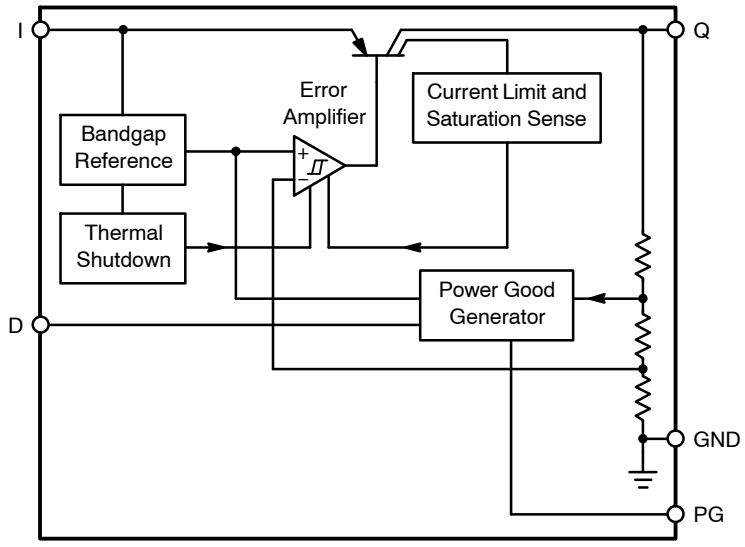

Figure 1. Block Diagram

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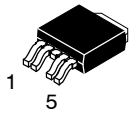
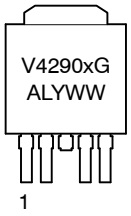
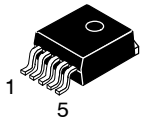
http://onsemi.com

MARKING DIAGRAMS



DPAK, 5−PIN
DT SUFFIX
CASE 175AA





D^{2}PAK, 5−PIN
DS SUFFIX
CASE 936A

x	= 5 (5.0 V Output)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

Pin	1. I
	2. PG
Tab,	3. GND*
	4. D
	5. Q

* Tab is connected to Pin 3 on all packages

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 13 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Description
1	I	Input; Battery Supply Input Voltage. Bypass to ground with a ceramic capacitor.
2	PG	Power Good Output; Open Collector Active Power Good (accurate when V_Q > 1.0 V).
3, Tab	GND	Ground; Pin 3 internally connected to tab.
4	D	Power Good Delay; timing capacitor to GND for Power Good Delay function.
5	Q	Output; ±2.0%, 450 mA output. Bypass with 22 μF capacitor, ESR < 4.0 Ω.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage	V_I	−42	45	V
Input Peak Transient Voltage	V_I	−	45	V
Output Voltage	V_Q	−1.0	16	V
Power Good Output Voltage	V_{PG}	−0.3	25	V
Power Good Output Current	I_{PG}	−5.0	5.0	mA
Power Good Delay Voltage	V_D	−0.3	7.0	V
Power Good Delay Current	I_D	−2.0	2.0	mA
ESD Susceptibility (Note 1) − Human Body Model − Machine Model − Charge Device Model	ESD_{HBM} ESD_{MM} ESD_{CDM}	4.0 200 1000	− − −	kV V V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{stg}	−55	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device incorporates ESD protection and is tested by the following methods: ESD Human Body Model tested per AEC−Q100−002, ESD Machine Model tested per AEC−Q100−003, ESD Charged Device Model tested per AEC−Q100−011, Latch−up tested per AEC−Q100−004.

OPERATING RANGE

Rating	Symbol	Min	Max	Unit
Input Voltage Operating Range, 5.0 V Option	V_I	5.5	42	V
Junction Temperature	T_J	–40	150	°C

LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 2)

Rating	Symbol	Min	Max	Unit
Lead Free, 60 sec–150 sec above 217°C	T_{SLD}	–	265 Peak	°C
Moisture Sensitivity Level	MSL	1		

2. PR_R IPC / JEDEC J–STD–020C

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5–PIN PACKAGE			
	0.3 sq. in. Spreader Board (Note 3)	1.2 sq. in. Spreader Board (Note 4)	
Junction–to–Tab ($R_{\theta JT}$)	4.5	4.8	°C/W
Junction–to–Ambient ($R_{\theta JA}$)	76	53	°C/W
D^2PAK 5–PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	1.2 sq. in. Spreader Board (Note 6)	
Junction–to–Tab ($R_{\theta JT}$)	3.8	4.1	°C/W
Junction–to–Ambient ($R_{\theta JA}$)	60	50	°C/W

3. 1 oz. copper, 0.26 $inch^2$ (168 mm^2) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 $inch^2$ (736 mm^2) copper area, 0.062″ thick FR4.
5. 1 oz. copper, 0.373 $inch^2$ (241 mm^2) copper area, 0.062″ thick FR4.
6. 1 oz. copper, 1.222 $inch^2$ (788 mm^2) copper area, 0.062″ thick FR4.

ELECTRICAL CHARACTERISTICS (V_I = 13.5 V, C_Q = 22 μF, ESR = 1.5 Ω; −40°C < T_J < 150°C; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage (5.0 V Option)	V_Q	100 μA ≤ I_Q ≤ 400 mA 6.0 V ≤ V_I ≤ 28 V	4.9	5.0	5.1	V
Output Voltage (5.0 V Option)	V_Q	100 μA ≤ I_Q ≤ 200 mA 6.0 V ≤ V_I ≤ 40 V	4.9	5.0	5.1	V
Output Current Limitation	I_Q	V_Q = 0.9 x $V_{Q,typ}$	450	1000	–	mA
Quiescent Current $I_q = I_I - I_Q$	I_q	I_Q = 1.0 mA	–	170	230	μA
		I_Q = 1.0 mA, T_J = 25°C	–	170	200	μA
		I_Q = 250 mA	–	10	15	mA
		I_Q = 400 mA	–	23	35	mA
Dropout Voltage (5.0 V Option)	V_{dr}	I_Q = 300 mA $V_{dr} = V_I - V_Q$ (Note 7)	–	250	500	mV
Load Regulation	ΔV_Q	I_Q = 5.0 mA to 400 mA	–30	5.0	30	mV
Line Regulation	ΔV_Q	ΔV_I = 8.0 V to 32 V, I_Q = 5.0 mA	–15	5.0	15	mV
Power Supply Ripple Rejection	PSRR	f_r = 100 Hz, V_r = 0.5 V_{pp}	–	60	–	dB
Temperature Output Voltage Drift	dV_Q/dT	––	–	0.5	–	mV/K
DELAY TIMING D AND POWER GOOD OUTPUT						
PG Switching Threshold (5.0 V Option)	$V_{Q,pgt-i}$	VQ increasing	4.45	4.65	4.8	V
PG Switching Threshold (5.0 V Option)	$V_{Q,pgt-d}$	VQ decreasing	3.5	3.65	3.8	V
PG Output Low Voltage	V_{PG}	$R_{ext} \geq$ 5.0 kΩ, $V_Q \geq$ 1.0 V	–	0.1	0.4	V
PG Output Leakage Current	I_{PG}	V_{PGH} > 4.5 V	–	0	10	μA
PG Charging Current	$I_{D,C}$	V_D = 1.0 V	3.0	6.0	9.0	μA
Upper Timing Threshold	V_{DU}	––	1.5	1.8	2.2	V
Lower Timing Threshold	V_{DL}	––	0.6	0.85	1.1	V
PG Delay Time	t_{rd}	C_D = 47 nF	10	16	22	ms
PG Reaction Time	t_{rr}	C_D = 47 nF	0.2	0.75	2.0	μs
THERMAL SHUTDOWN						
Shutdown Temperature (Note 8)	T_{SD}	––	150	–	210	°C

7. Measured when output voltage V_Q falls 100 mV below the regulated voltage at V_I = 13.5 V. $V_{dr} = V_I - V_Q$.
8. Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

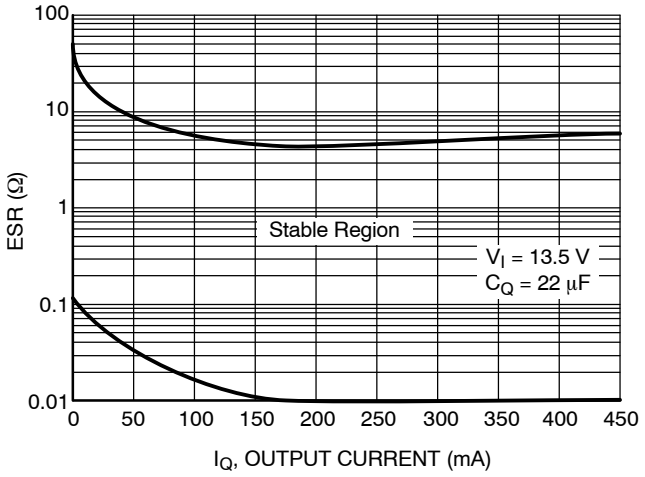


Figure 2. Output Stability with Output Capacitor ESR

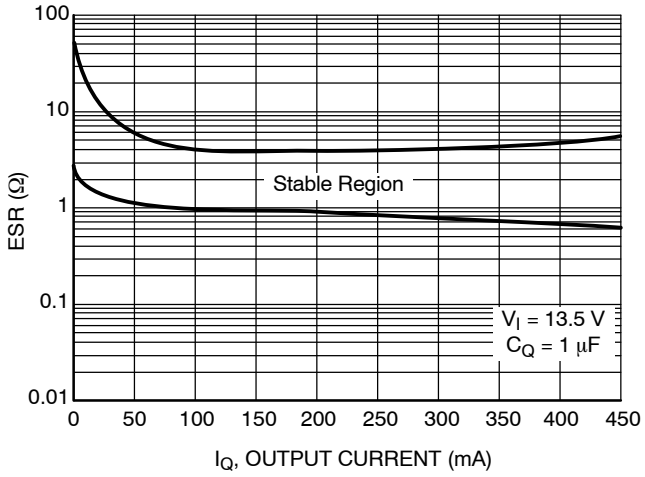


Figure 3. Output Stability with Output Capacitor ESR

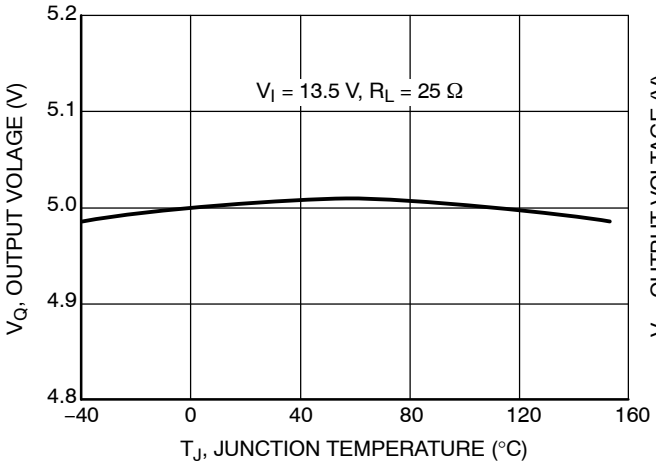


Figure 4. Output Voltage V_Q vs. Temperature T_J

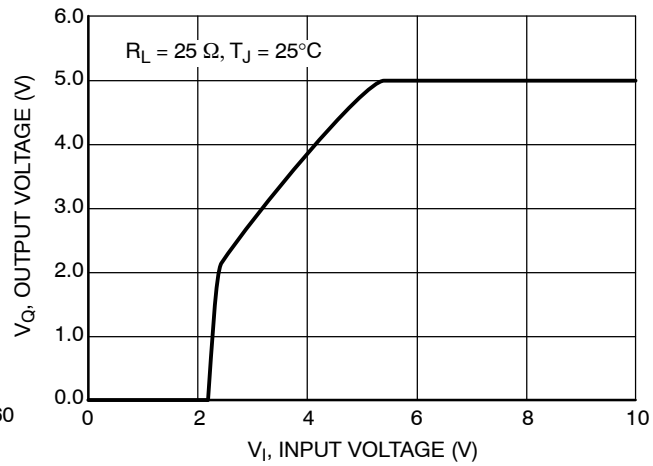


Figure 5. Output Voltage V_Q vs. Input Voltage V_I

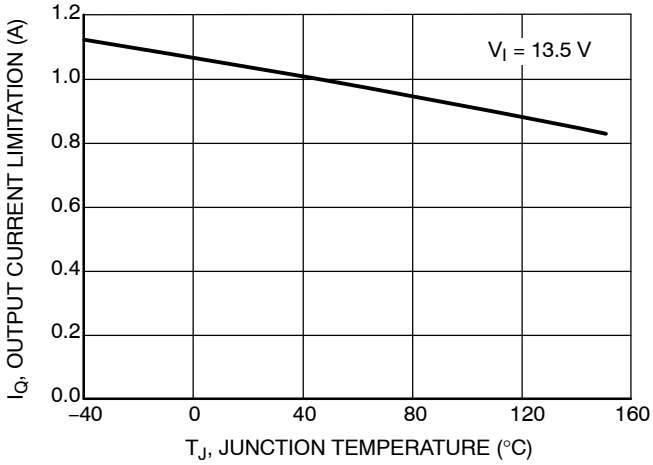


Figure 6. Output Current I_Q vs. Temperature T_J

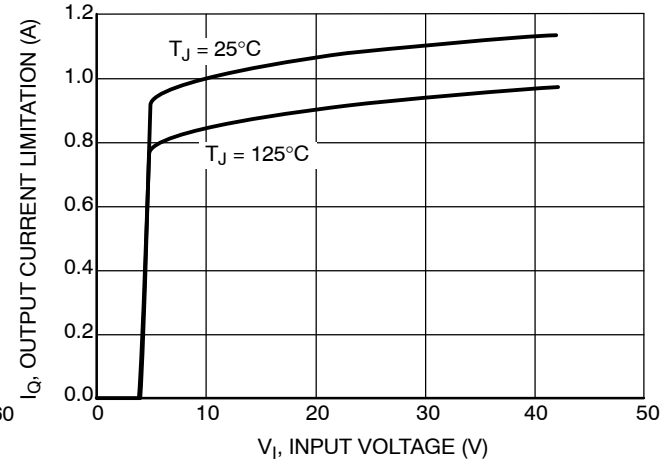


Figure 7. Output Current I_Q vs. Input Voltage V_I

TYPICAL PERFORMANCE CHARACTERISTICS

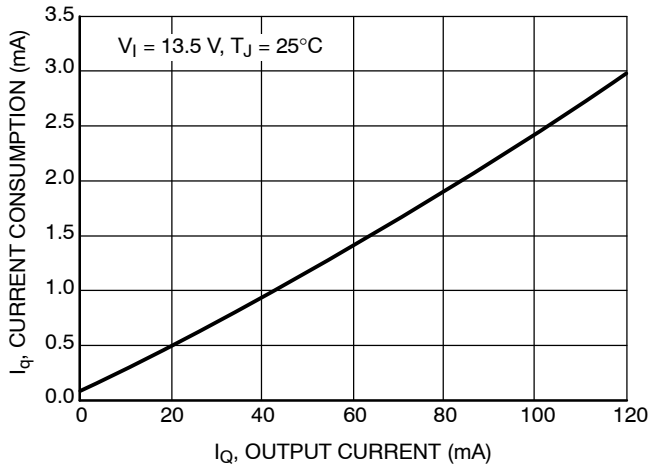


Figure 8. Current Consumption I_q vs. Output Current I_Q

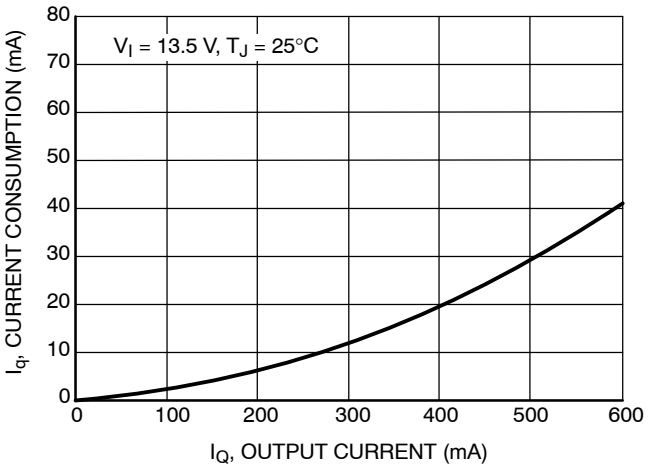


Figure 9. Current Consumption I_q vs. Output Current I_Q

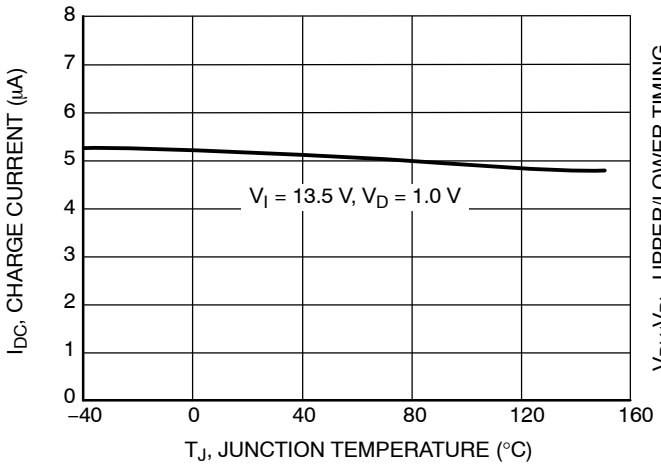


Figure 10. Charge Current $I_{D,C}$ vs. Temperature T_J

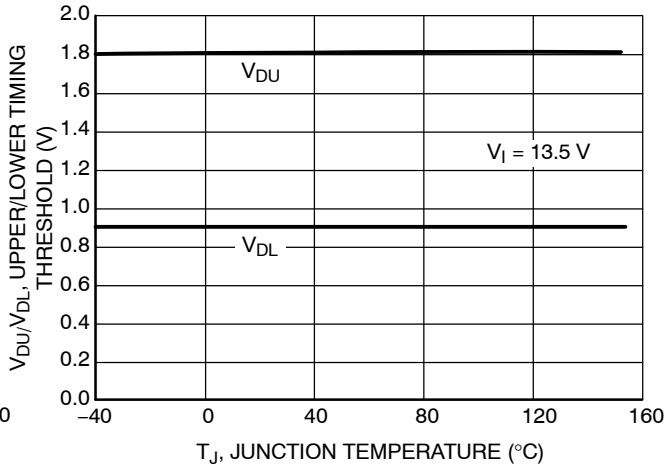


Figure 11. Delay Switching Threshold V_{DU}, V_{DL} vs. Temperature T_J

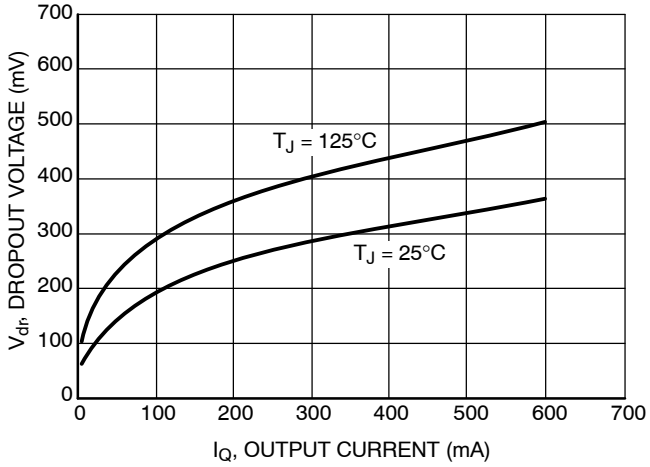


Figure 12. Drop Voltage V_{dr} vs. Output Current I_Q

APPLICATION INFORMATION

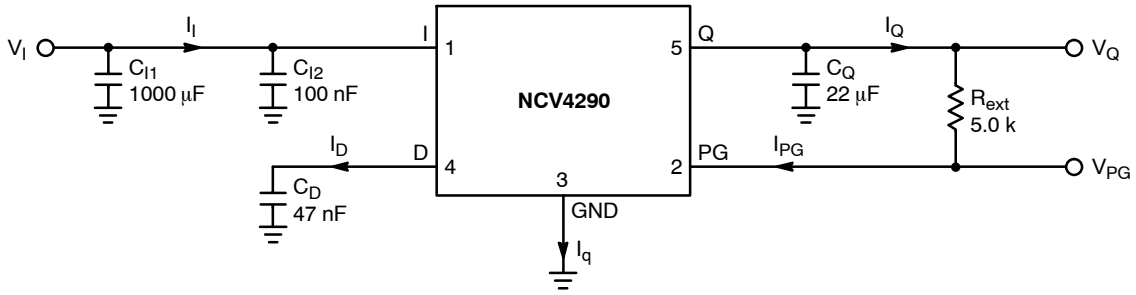


Figure 13. Test Circuit

Circuit Description

The NCV4290 is an integrated low dropout regulator that provides 5.0 V, 450 mA protected output and a signal for power on power good. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible drop out voltage and best possible temperature stability. The output current capability is 450 mA, and the base drive quiescent current is controlled to prevent over saturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures. The delay time for the power good output is adjustable by selection of the timing capacitor. See Figure 13, Test Circuit, for circuit element nomenclature illustration.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_Q) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with C_{I2} can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum, aluminum or ceramic capacitors can be used. The range of stability versus capacitance, load current and capacitive ESR is illustrated in Figures 2 and 3. Minimum ESR for C_Q = 22 μF is native ESR of ceramic capacitors. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the capacitance and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 13, Test Circuit, should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed for $C_Q \geq 22$ μF and an ESR ≤ 4.0 Ω.

ESR characteristics were measured with ceramic capacitors and additional resistors to emulate ESR. Murata ceramic capacitors were used, GRM32ER71C226ME18 (22 μF, 16 V, X7R, 1210), GRM219R71E105KA88 (1 μF, 25 V, X7R, 0805).

Power Good Output

The power good output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the controller. It pulls low when the output is not considered to be ready. PG is pulled up to V_Q by an external resistor, typically 5.0 kΩ in value. Hysteresis is implemented for PG signal. When output voltage is decreasing PG goes Low at VQ typ 3.65 V and when output voltage is increasing PG goes High at VQ typ 4.65 V. The input and output conditions that control the Power Good Output and the relative timing are illustrated in Figure 14, Power Good Timing.

Output voltage regulation must be maintained for the delay time before the power good output signals a valid condition. The delay for the power good output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0.0 V to the upper timing threshold voltage V_{DU}. The charging current for this is $I_{D,C}$ and D pin voltage in steady state is typically 2.85 V. By using typical IC parameters with a 47 nF capacitor on the D pin, the following time delay for 5.0 V regulator is derived:

$t_{RD} = C_D V_{DU} / I_{D,C}$

t_{RD} = 47 nF (1.8 V) / 6.0 μA = 14.1 ms

Other time delays can be obtained by changing the capacitor value.

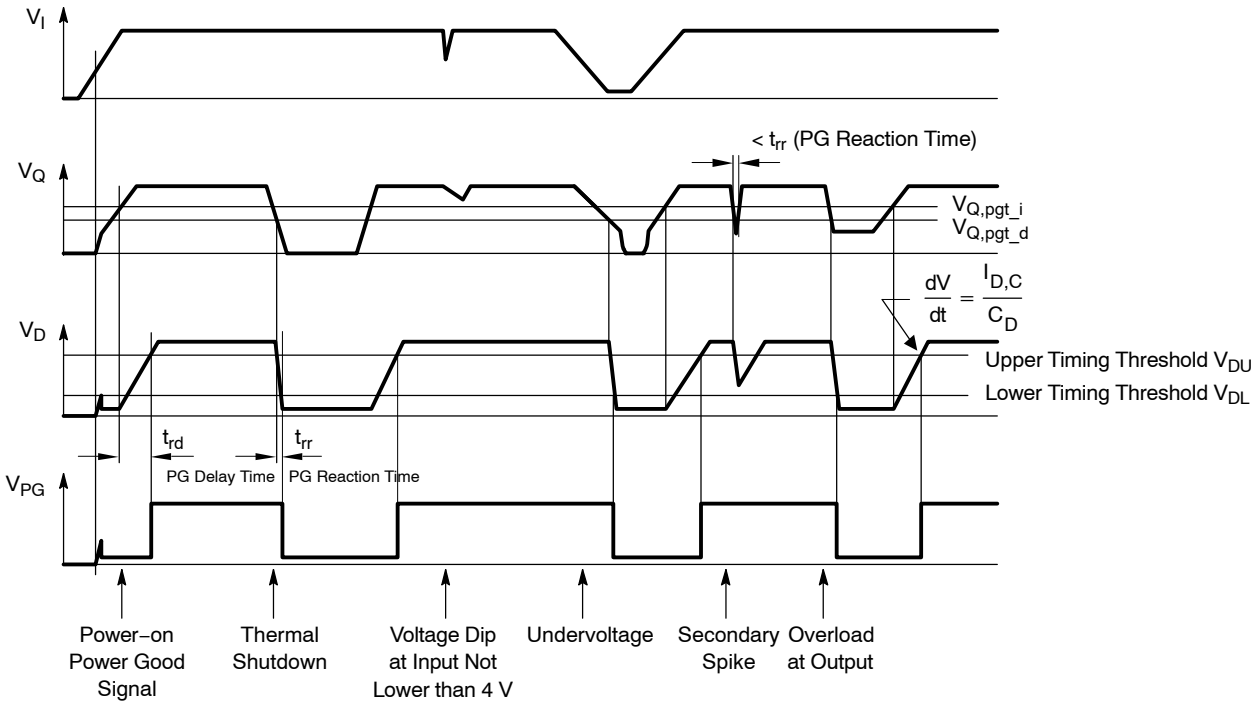


Figure 14. Power Good Timing

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 15) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application,
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

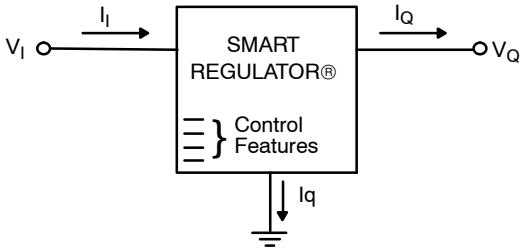


Figure 15. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

Thermal Model

A discussion of thermal modeling is in the ON Semiconductor web site: http://www.onsemi.com/pub/collateral/BR1487−D.PDF.

Table 1. DPAK 5−Lead Thermal RC Network Models

Drain Copper Area (1 oz thick)			**168 mm²**	**736 mm²**		**168 mm²**	**736 mm²**	
(SPICE Deck Format)			**Cauer Network**			**Foster Network**		
			168 mm²	736 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	9.5059E−06	9.5059E−06	W−s/C	1.000E−06	1.000E−06	sec
C_C2	**node1**	**Gnd**	3.7125E−05	3.7125E−05	W−s/C	1.000E−05	1.000E−05	sec
C_C3	**node2**	**Gnd**	1.1233E−05	1.1233E−05	W−s/C	1.000E−04	1.000E−04	sec
C_C4	**node3**	**Gnd**	6.5344E−04	6.5339E−04	W−s/C	4.893E−04	4.893E−04	sec
C_C5	**node4**	**Gnd**	2.1647E−02	2.1606E−02	W−s/C	4.770E−03	4.770E−03	sec
C_C6	node5	Gnd	2.1471E−02	2.1361E−02	W−s/C	4.129E−02	4.129E−02	sec
C_C7	node6	Gnd	7.9135E−02	7.8444E−02	W−s/C	4.237E−01	4.237E−01	sec
C_C8	node7	Gnd	2.8534E−01	3.1338E−01	W−s/C	3.499	3.499	sec
C_C9	node8	Gnd	6.6085E−01	1.5496	W−s/C	8.532	49.601	sec
C_C10	node9	Gnd	8.7266E−01	24.4877	W−s/C	77.552	88.429	sec
			168 mm²	736 mm²		R's	R's	
R_R1	**Junction**	**node1**	1.3480E−01	1.3480E−01	C/W	0.0803	0.0803	C/W
R_R2	**node1**	**node2**	3.0852E−01	3.0853E−01	C/W	0.1736	0.1736	C/W
R_R3	**node2**	**node3**	8.0674E−01	8.0676E−01	C/W	0.5491	0.5491	C/W
R_R4	**node3**	**node4**	5.8520E−01	5.8528E−01	C/W	0.9733	0.9733	C/W
R_R5	**node4**	**node5**	4.7850E−01	4.8022E−01	C/W	0.1096	0.1096	C/W
R_R6	node5	node6	1.3832	1.3916	C/W	0.7361	0.7361	C/W
R_R7	node6	node7	4.8520	4.8196	C/W	2.8713	2.8713	C/W
R_R8	node7	node8	18.0698	10.0128	C/W	3.0988	8.1070	C/W
R_R9	node8	node9	15.7788	31.8880	C/W	10.1005	14.0987	C/W
R_R10	node9	Gnd	33.5404	2.7829	C/W	57.2455	25.5115	C/W

NOTE: Bold face items represent the package without the external thermal system.

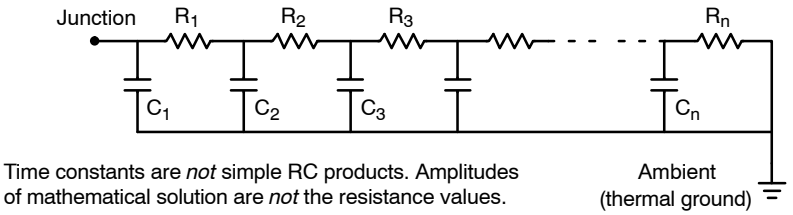


Figure 16. Grounded Capacitor Thermal Network ("Cauer" Ladder)

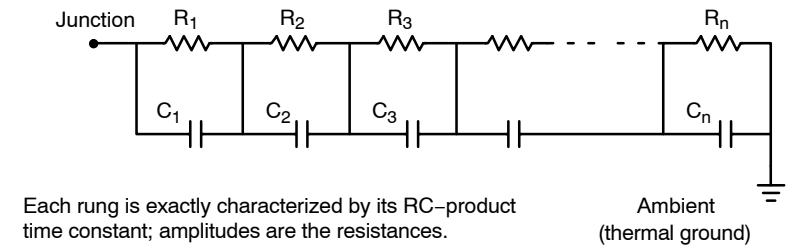


Figure 17. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)

Table 2. D²PAK 5−Lead Thermal RC Network Models

Drain Copper Area (1 oz thick)			241 mm²	788 mm²		241 mm²	788 mm²	
(SPICE Deck Format)			Cauer Network			Foster Network		
			241 mm²	788 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	9.5070E−06	9.5071E−06	W−s/C	1.000E−06	1.000E−06	sec
C_C2	**node1**	**Gnd**	3.7150E−05	3.7151E−05	W−s/C	1.000E−05	1.000E−05	sec
C_C3	**node2**	**Gnd**	1.1261E−04	1.1262E−04	W−s/C	1.000E−04	1.000E−04	sec
C_C4	**node3**	**Gnd**	6.6126E−04	6.6143E−04	W−s/C	4.893E−04	4.893E−04	sec
C_C5	**node4**	**Gnd**	2.9986E−02	3.0234E−02	W−s/C	4.770E−03	4.770E−03	sec
C_C6	node5	Gnd	5.2806E−02	5.4409E−02	W−s/C	4.129E−02	4.129E−02	sec
C_C7	node6	Gnd	3.9578E−01	4.6168E−01	W−s/C	1.294E+00	1.294E+00	sec
C_C8	node7	Gnd	9.6950E−01	1.66	W−s/C	2.089E+01	6.008E+01	sec
C_C9	node8	Gnd	2.26	37.44	W−s/C	5.824E+01	7.069E+01	sec
C_C10	node9	Gnd	231.58	4089.09	W−s/C			sec
			241 mm²	788 mm²		R's	R's	
R_R1	**Junction**	**node1**	1.3476E−01	1.3476E−01	C/W	0.0803	0.0803	C/W
R_R2	**node1**	**node2**	3.0817E−01	3.0817E−01	C/W	0.1736	0.1736	C/W
R_R3	**node2**	**node3**	8.0361E−01	8.0355E−01	C/W	0.5491	0.5491	C/W
R_R4	**node3**	**node4**	5.7370E−01	5.7346E−01	C/W	0.9733	0.9733	C/W
R_R5	**node4**	**node5**	2.6250E−01	2.5833E−01	C/W	0.1096	0.1096	C/W
R_R6	node5	node6	5.6022E−01	5.3623E−01	C/W	0.5367	0.5367	C/W
R_R7	node6	node7	4.0655	3.1454	C/W	1.8971	1.8971	C/W
R_R8	node7	node8	38.4592	42.3515	C/W	2.9679	2.9679	C/W
R_R9	node8	node9	14.9707	1.9244	C/W	1.9498	4.0572	C/W
R_R10	node9	gnd	2.5618E−01	1.6530E−02	C/W			C/W

NOTE: Bold face items represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

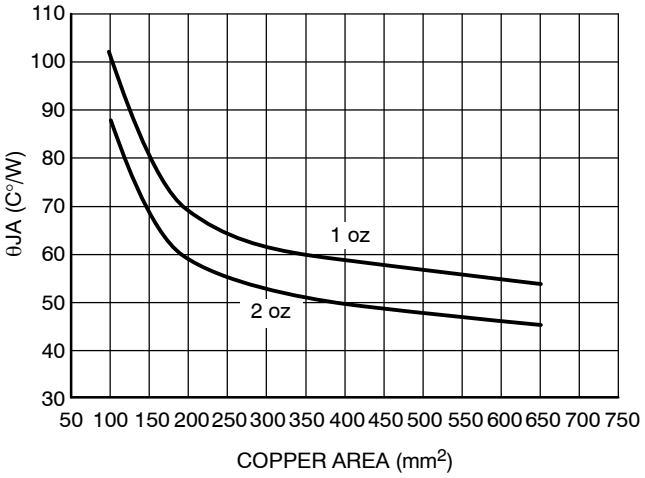


Figure 18. θJA vs. Copper Spreader Area, DPAK 5−Lead

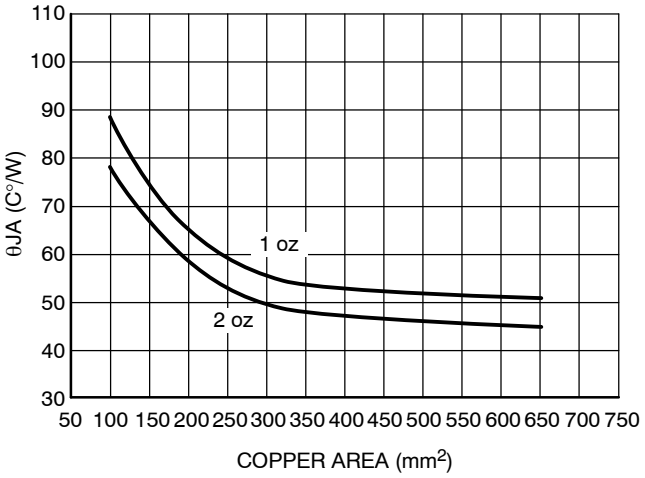


Figure 19. θJA vs. Copper Spreader Area, D²PAK 5−Lead

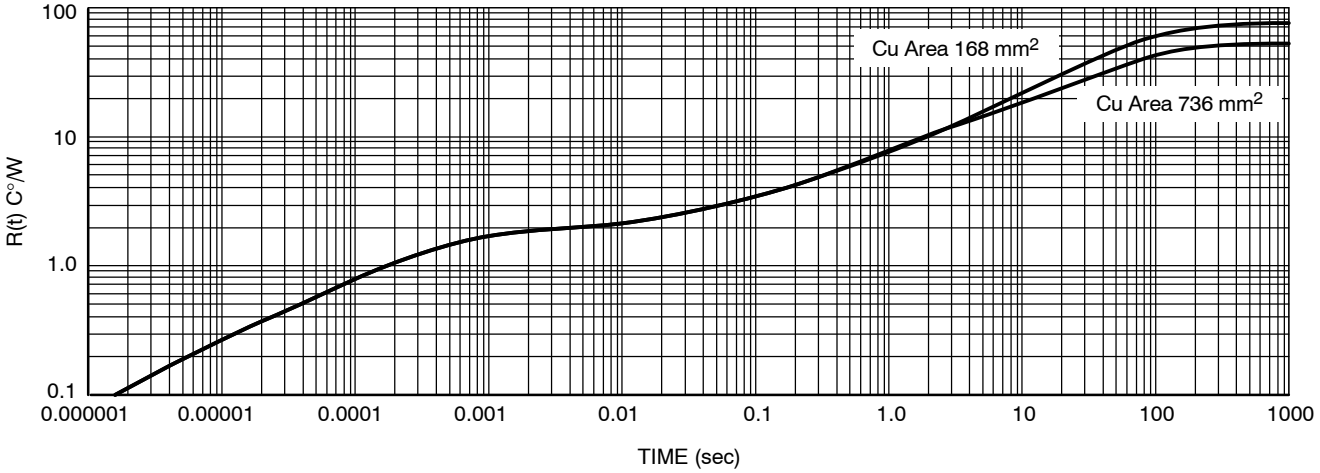


Figure 20. Single−Pulse Heating Curves, DPAK 5−Lead

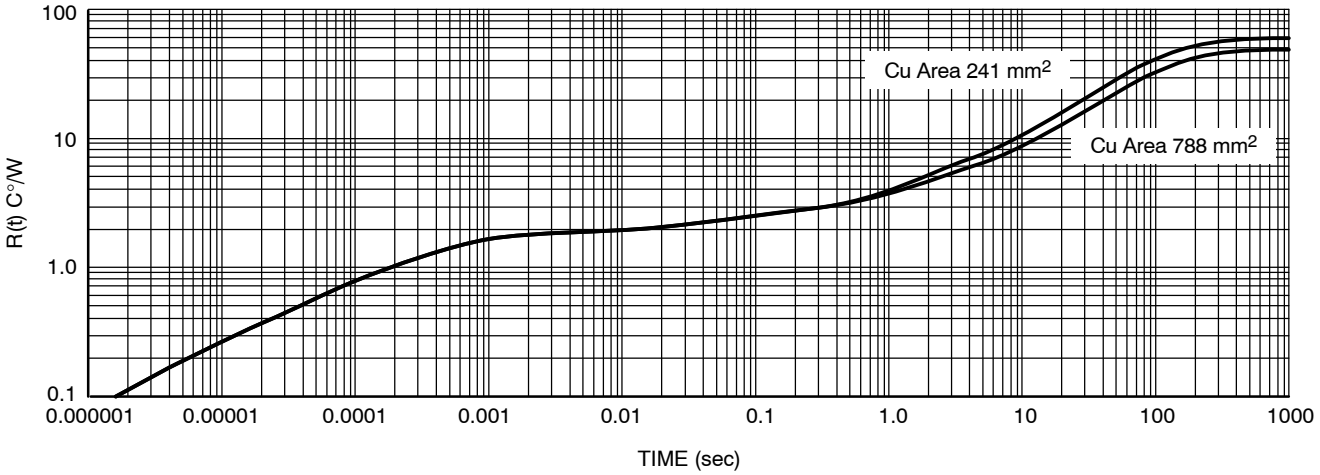


Figure 21. Single−Pulse Heating Curves, D²PAK 5−Lead

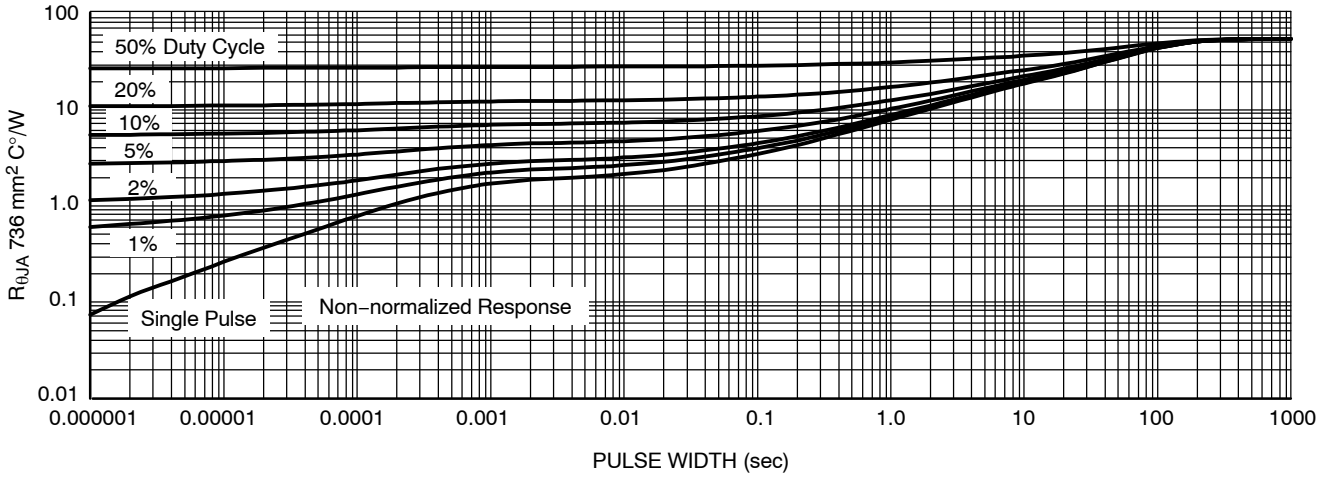


Figure 22. Duty Cycle for 1” Spreader Boards, DPAK 5−Lead

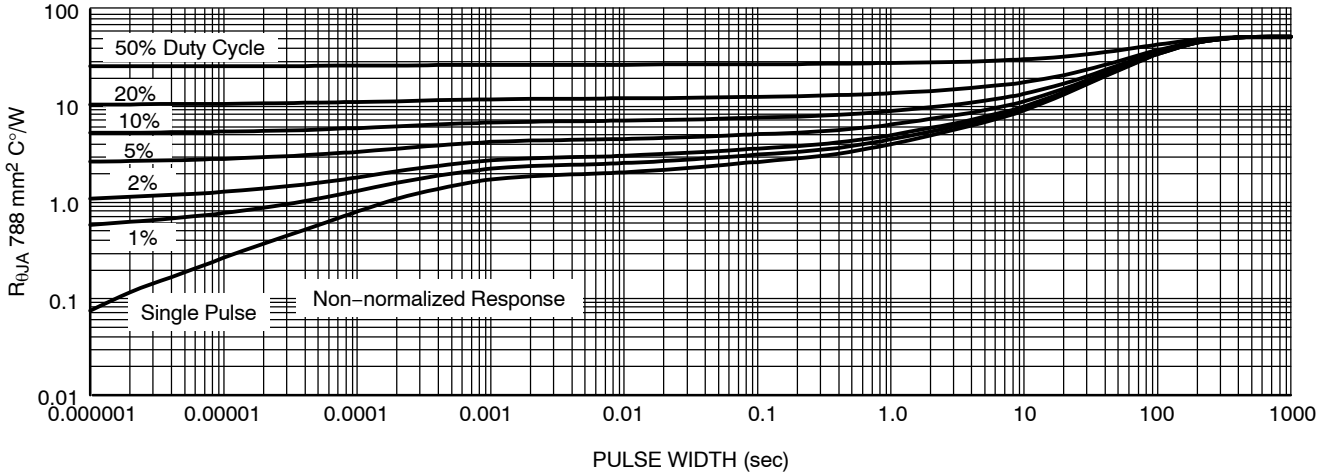


Figure 23. Duty Cycle for 1” Spreader Boards, D²PAK 5−Lead

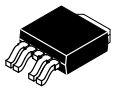
ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV4290DS50R4G	5.0 V	D²PAK (Pb−Free)	800 / Tape & Reel
NCV4290DT50RKG		DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

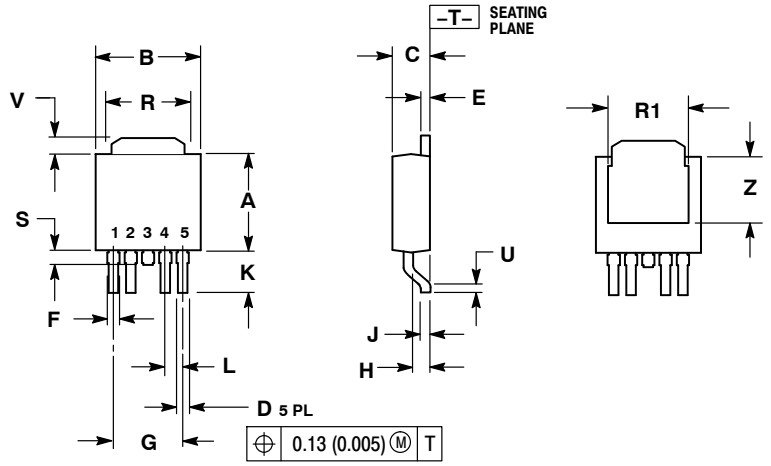
ON Semiconductor®



DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014

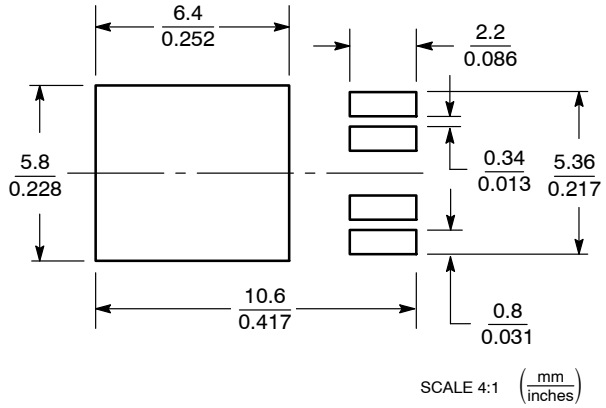
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

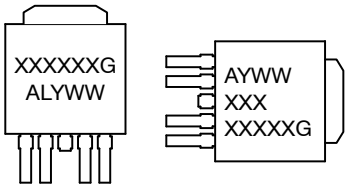
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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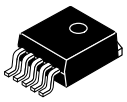
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



D²PAK 5−LEAD
CASE 936A−02
ISSUE E

DATE 28 JUL 2021

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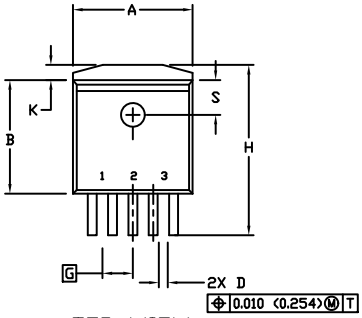
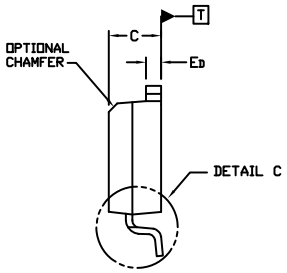
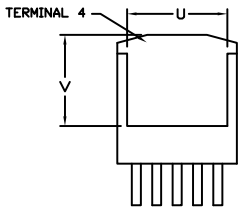


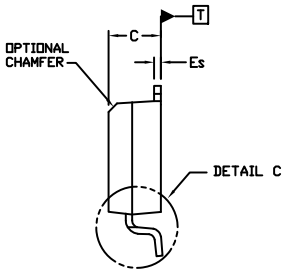
TOP VIEW



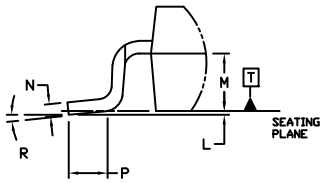
SIDE VIEW
DUAL GUAGE CONSTRUCTION



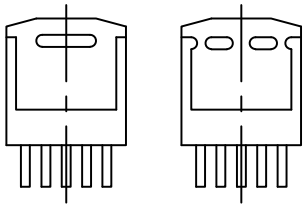
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW

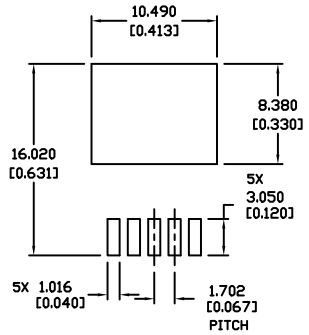


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

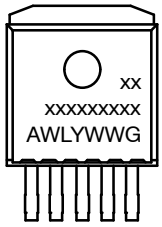
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D2PAK 5−LEAD**	**PAGE 1 OF 1**

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