

# High Side Switch with Adjustable Current Limit and Diagnostic Features



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## NCV47722

The NCV47722 High Side Switch (HSS) with 250 mA is designed for use in harsh automotive environments. The device has a high peak input voltage tolerance and reverse input voltage, reverse bias, overcurrent and overtemperature protections. The integrated current sense feature (adjustable by resistor connected to CSO pin) provides diagnosis and system protection functionality. The CSO pin output current creates voltage drop across CSO resistor which is proportional to output current. Extended diagnostic features in OFF state are also available and controlled by dedicated input and output pins.

### Features

- Output Current: up to 250 mA
- Enable Input (3.3 V Logic Compatible)
- Adjustable Current Limit: up to 350 mA
- Protection Features:
  - ◆ Current Limitation
  - ◆ Thermal Shutdown
  - ◆ Reverse Input Voltage and Reverse Bias Voltage
- Diagnostic Features:
  - ◆ Short To Battery (STB) and Open Load (OL) in OFF State
  - ◆ Internal Components for OFF State Diagnostics
  - ◆ Open Collector Flag Output
  - ◆ Output Voltage Monitoring Output (analog)
- AEC-Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Audio and Infotainment System
- Active Safety System

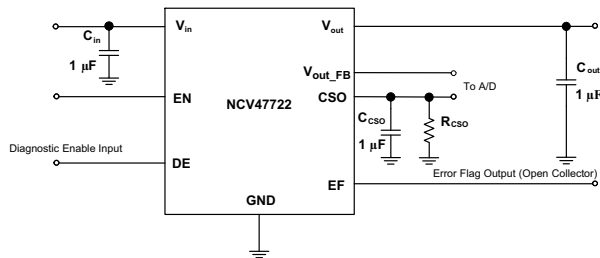


Figure 1. Application Schematic

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

### MARKING DIAGRAM



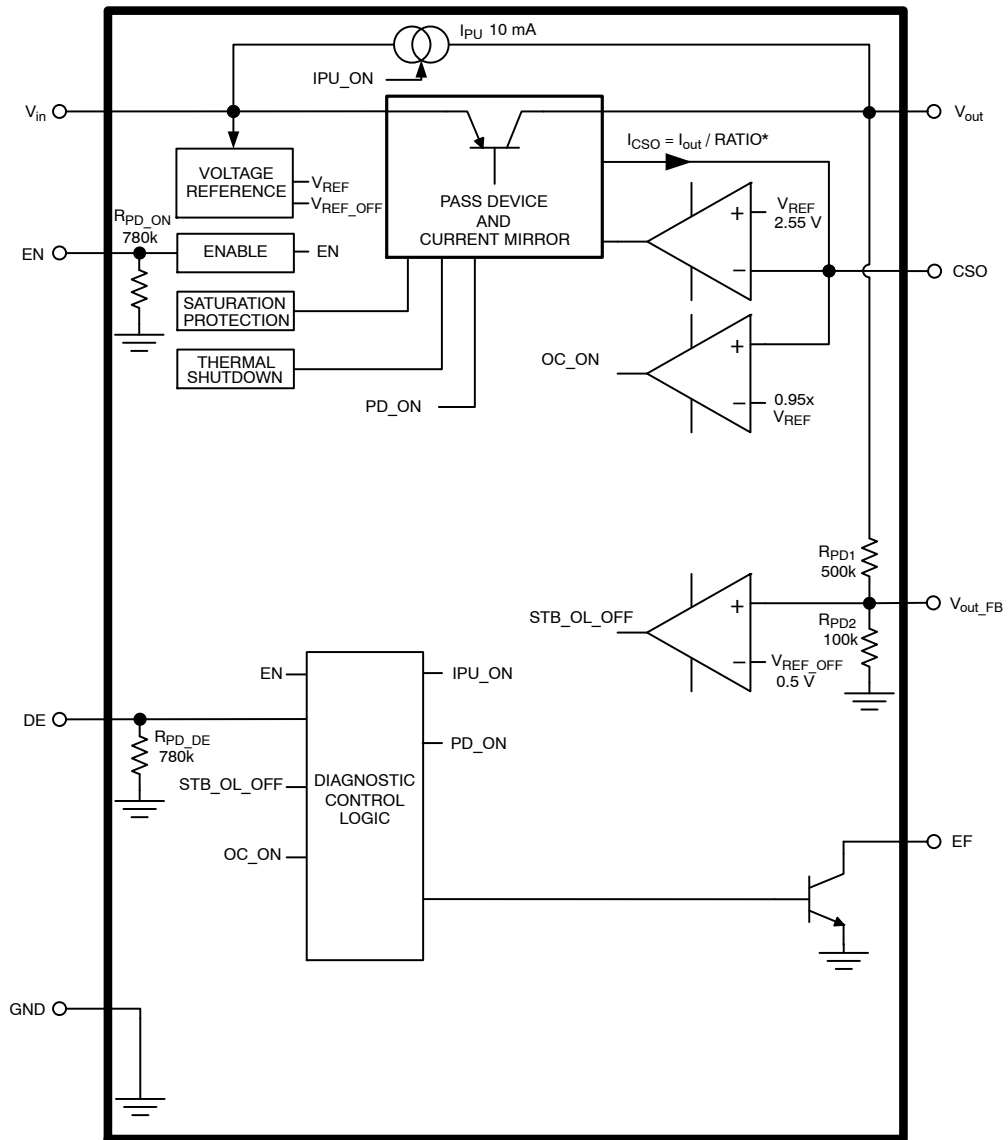
47722 = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

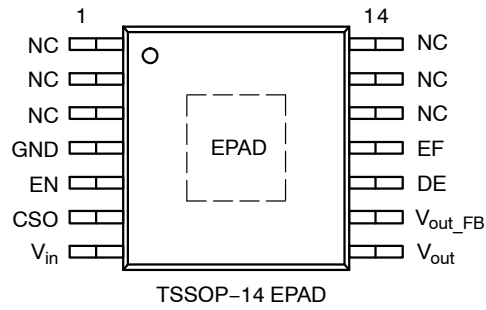
# NCV47722



\*) for current value of RATIO see into Electrical Characteristic Table

**Figure 2. Simplified Block Diagram**

# NCV47722



**Figure 3. Pin Connections (Top Views)**

**Table 1. PIN FUNCTION DESCRIPTION**

Pin No. TSSOP-14 EPAD	Pin Name	Description
1	NC	Not Connected, not internally bonded.
2	NC	Not Connected, not internally bonded.
3	NC	Not Connected, not internally bonded.
4	GND	Power Supply Ground.
5	EN	Enable Input; low level disables regulator. (Used also for OFF state diagnostics control.
6	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
7	V <sub>in</sub>	Power Supply Input.
8	V <sub>out</sub>	Regulated Output Voltage.
9	V <sub>out_FB</sub>	Output Voltage Analog Monitoring. See Application Section for more details.
10	DE	Diagnostic Enable Input.
11	EF	Error Flag (Open Collector) Output. Active Low.
12	NC	Not Connected, not internally bonded.
13	NC	Not Connected, not internally bonded.
14	NC	Not Connected, not internally bonded.
EPAD	EPAD	Exposed Pad is connected to Ground. Connect to GND plane on PCB.

**Table 2. MAXIMUM RATINGS**

Rating	Symbol	Min	Max	Unit
Input Voltage DC	$V_{in}$	-42	45	V
Input Voltage (Note 1) Load Dump – Suppressed	$U_{S*}$	-	60	V
Enable Input Voltage	$V_{EN}$	-42	45	V
Output Voltage Monitoring	$V_{out\_FB}$	-0.3	10	V
CSO Voltage	$V_{CSO}$	-0.3	7	V
DE, CS and EF Voltages	$V_{DE}, V_{CS}, V_{EF}$	-0.3	7	V
Output Voltage	$V_{out}$	-1	40	V
Junction Temperature	$T_J$	-40	150	°C
Storage Temperature	$T_{STG}$	-55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750-1.

**Table 3. ESD CAPABILITY** (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	$ESD_{HBM}$	-2	2	kV

2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (JS-001-2010)  
 Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm<sup>2</sup> due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2014.

**Table 4. LEAD SOLDERING TEMPERATURE AND MSL** (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		-

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**THERMAL CHARACTERISTICS** (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics (single layer PCB) Thermal Resistance, Junction-to-Air (Note 5) Thermal Reference, Junction-to-Lead (Note 5)	$R_{\theta JA}$ $R_{\psi JL}$	62.6 23.7	°C/W
Thermal Characteristics (4 layers PCB) Thermal Resistance, Junction-to-Air (Note 5) Thermal Reference, Junction-to-Lead (Note 5)	$R_{\theta JA}$ $R_{\psi JL}$	44.1 16.8	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm<sup>2</sup> (or 1 in<sup>2</sup>) of 1 oz copper thickness and FR4 PCB substrate. Single layer – according to JEDEC51.3, 4 layers – according to JEDEC51.7

**Table 5. RECOMMENDED OPERATING RANGES**

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	$V_{in}$	4.4	40	V
Output Current Limit (Note 7)	$I_{LIM}$	10	350	mA
Junction Temperature	$T_J$	-40	150	°C
Current Sense Output (CSO) Capacitor	$C_{CSO}$	1	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum  $V_{in} = 4.4 V$  or  $(V_{out} + 0.5 V)$ , whichever is higher.
7. Corresponding  $R_{CSO}$  is in range from 76.5 kΩ down to 2185 Ω.

# NCV47722

**Table 6. ELECTRICAL CHARACTERISTICS**  $V_{in} = 13.5\text{ V}$ ,  $V_{EN} = 3.3\text{ V}$ ,  $R_{CSO} = 0\ \Omega$ ,  $C_{CSO} = 1\ \mu\text{F}$ ,  $C_{in} = 1\ \mu\text{F}$ ,  $C_{out} = 1\ \mu\text{F}$ , Min and Max values are valid for temperature range  $-40^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$  unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to  $T_J = 25^{\circ}\text{C}$  (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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## OUTPUTS

Input to Output Differential Voltage	$V_{in} = 8\text{ V to }18\text{ V}$ $I_{out} = 200\text{ mA}$ $I_{out} = 250\text{ mA}$	$V_{in-out}$	-	200 225	350 400	mV
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## CURRENT LIMIT PROTECTION

Current Limit	$V_{out} = V_{in} - 1\text{ V}$	$I_{LIM}$	350	-	-	mA
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## DISABLE AND QUIESCENT CURRENTS

Disable Current	$V_{EN} = 0\text{ V}$	$I_{DIS}$	-	0.002	10	$\mu\text{A}$
Quiescent Current, $I_q = I_{in} - I_{out}$	$I_{out} = 500\ \mu\text{A}$ , $V_{in} = 8\text{ V to }18\text{ V}$	$I_q$	-	0.5	1.3	mA
Quiescent Current, $I_q = I_{in} - I_{out}$	$I_{out} = 200\text{ mA}$ , $V_{in} = 8\text{ V to }18\text{ V}$	$I_q$	-	8	19	mA
Quiescent Current, $I_q = I_{in} - I_{out}$	$I_{out} = 250\text{ mA}$ , $V_{in} = 8\text{ V to }18\text{ V}$	$I_q$	-	11	25	mA

## ENABLE

Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	$V_{out} \leq 0.1\text{ V}$ $V_{out} \geq V_{in} - 1\text{ V}$	$V_{th(EN)}$	0.99 -	1.8 1.9	- 2.31	V
Enable Input Current	$V_{EN} = 3.3\text{ V}$	$I_{EN}$	2	9	20	$\mu\text{A}$
Turn On Time from Enable ON to $V_{out} = V_{in} - 1\text{ V}$	$I_{out} = 100\text{ mA}$	$t_{on}$	-	25	-	$\mu\text{s}$

## OUTPUT CURRENT SENSE

CSO Voltage Level at Current Limit	$V_{out} = V_{in} - 1\text{ V}$ $R_{CSO} = 3.3\text{ k}\Omega$	$V_{CSO\_Ilim}$	2.448 (-4%)	2.55	2.652 (+4%)	V
CSO Transient Voltage Level	$C_{CSO} = 4.7\ \mu\text{F}$ , $R_{CSO} = 3.3\text{ k}\Omega$ $I_{out}$ pulse from 10 mA to 350 mA, $t_r = 1\ \mu\text{s}$	$V_{CSO}$	-	-	3.3	V
Output Current to CSO Current Ratio	$V_{CSO} = 2\text{ V}$ , $I_{out} = 10\text{ mA to }50\text{ mA}$ $V_{in} = 8\text{ V to }18\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$	$I_{out}/I_{CSO}$	- (-15%)	265	- (+15%)	-
Output Current to CSO Current Ratio	$V_{CSO} = 2\text{ V}$ , $I_{out} = 50\text{ mA to }350\text{ mA}$ $V_{in} = 8\text{ V to }18\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$	$I_{out}/I_{CSO}$	- (-5%)	285	- (+5%)	-
CSO Current at no Load Current	$V_{CSO} = 0\text{ V}$ , $I_{out} = 0\text{ mA}$	$I_{CSO\_off}$	-	-	15	$\mu\text{A}$

## DIAGNOSTICS

Overcurrent Voltage Level Threshold	$V_{out} = V_{in} - 1\text{ V}$ $R_{CSO} = 3.3\text{ k}\Omega$	$V_{OC}$	92	95	98	% of $V_{CSO\_Ilim}$
Short To Battery (STB) Voltage Threshold in OFF state	$V_{in} = 4.4\text{ V to }18\text{ V}$ , $I_{out} = 0\text{ mA}$	$V_{STB}$	2	3	4	V
Open Load (OL) Current Threshold in OFF state	$V_{in} = 4.4\text{ V to }18\text{ V}$	$I_{OL}$	5	10	25	mA
Output Voltage to Output Feedback Voltage Ratio	$V_{in} = 4.4\text{ V to }18\text{ V}$	$V_{out}/V_{outFB}$	5.7	6	6.3	-
Diagnostics Enable Threshold Voltage Logic Low (OFF) Logic High (ON)		$V_{th(DE)}$	0.99 -	1.8 1.9	- 2.31	V
Error Flag Low Voltage	$I_{EF} = -1\text{ mA}$	$V_{EF\_Low}$	-	0.04	0.4	V

## THERMAL SHUTDOWN

Thermal Shutdown Temperature (Note 9)	$I_{out} = 90\text{ mA}$	$T_{SD}$	150	175	195	$^{\circ}\text{C}$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_A \approx T_J$ . Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
- Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

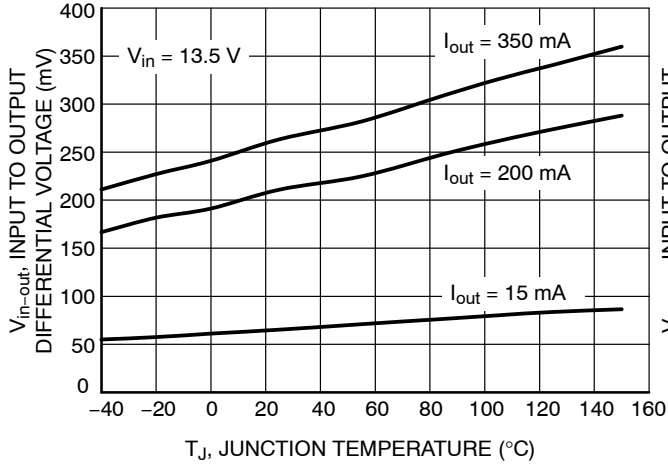


Figure 4. Input to Output Differential Voltage vs. Temperature

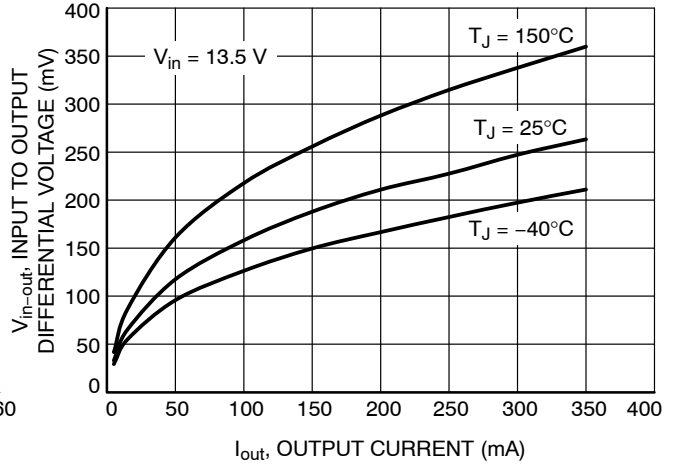


Figure 5. Input to Output Differential Voltage vs. Output Current

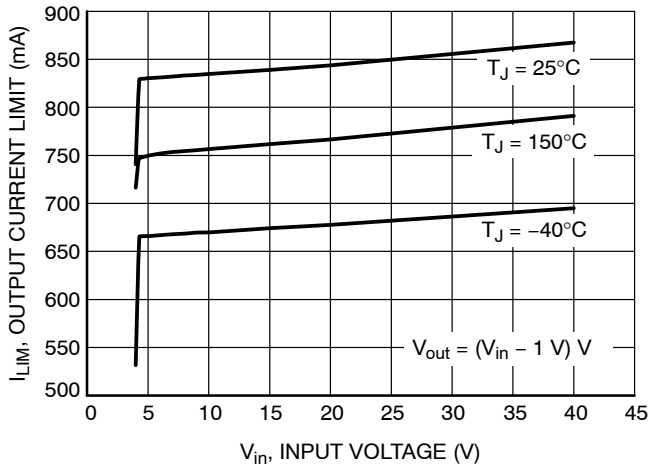


Figure 6. Output Current Limit vs. Input Voltage

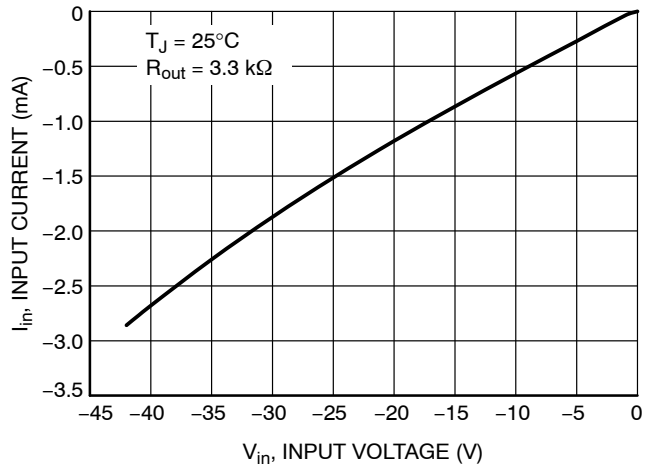


Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

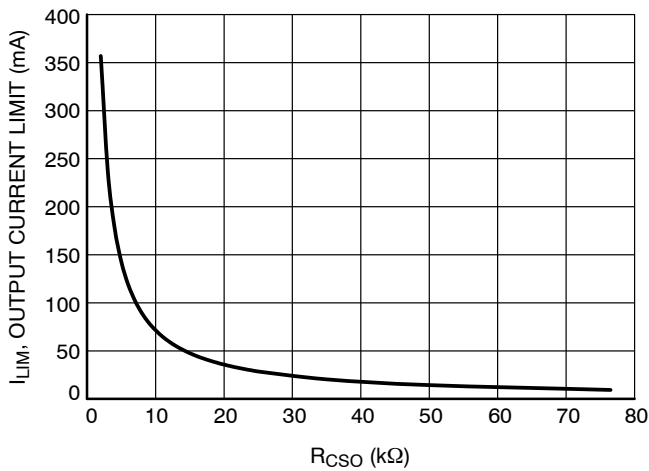


Figure 8. Output Current Limit vs. R<sub>CSO</sub>

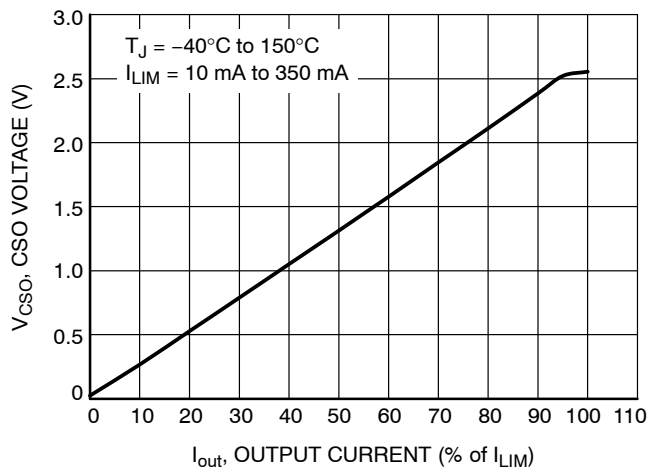


Figure 9. CSO Voltage vs. Output Current (% of I<sub>LIM</sub>)

TYPICAL CHARACTERISTICS

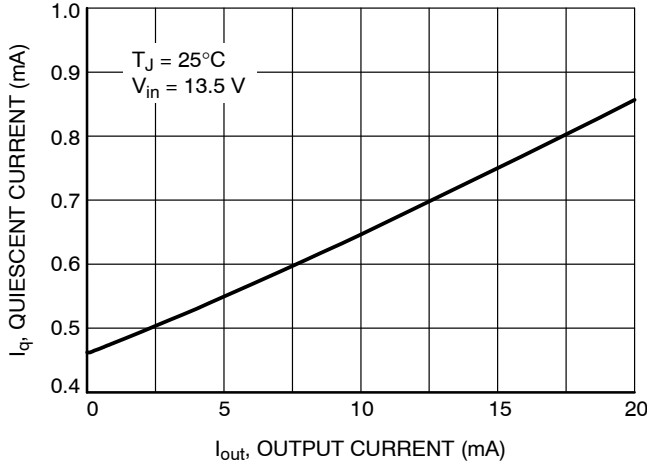


Figure 10. Quiescent Current vs. Output Current (Low Load)

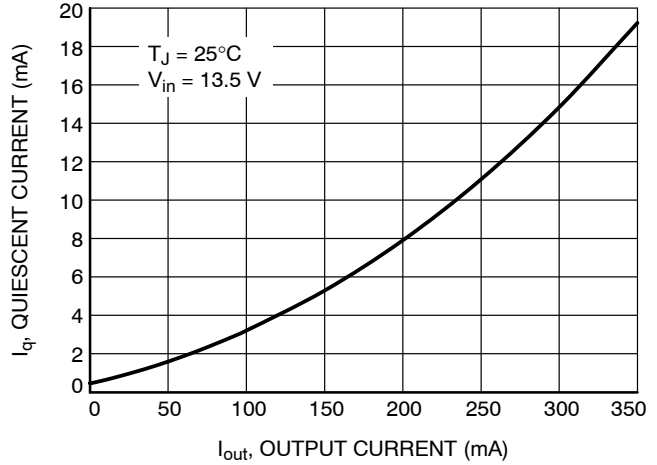


Figure 11. Quiescent Current vs. Output Current (High Load)

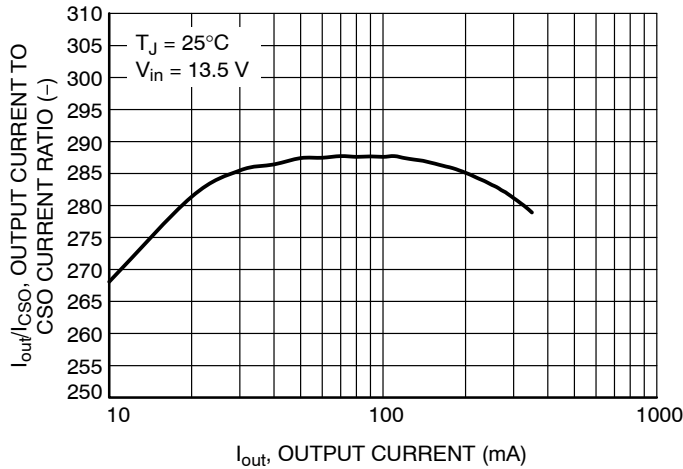


Figure 12. Output Current to CSO Current Ratio vs. Output Current

DEFINITIONS

**General**

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

**Input to Output Differential Voltage**

The Input to Output Differential Voltage parameter is defined for specific output current values and specified over Temperature range.

**Quiescent and Disable Currents**

Quiescent Current ( $I_q$ ) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current ( $I_{DIS}$ ).

**Current Limit**

Current Limit is value of output current by which output voltage drops 1 V below input supply voltage level.

**Thermal Protection**

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

**Maximum Package Power Dissipation**

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

**Circuit Description**

The NCV47722 is an integrated High Side Switch (HSS) with output current capability up to 250 mA to output. It is enabled with an input to the enable pin. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The HSS is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

**Enable Input**

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.99 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

**Setting the Output Current Limit**

The output current limit can be set up to 350 mA by external resistor R<sub>CSO</sub> (see Figure 1). Capacitor C<sub>CSO</sub> of 1 μF in parallel with R<sub>CSO</sub> is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO} = I_{out} \left( R_{CSO} \times \frac{1}{RATIO} \right) \quad (eq. 1)$$

$$I_{LIM} = RATIO \times \frac{2.55}{R_{CSO}} \quad (eq. 2)$$

$$R_{CSO} = RATIO \times \frac{2.55}{I_{LIM}} \quad (eq. 3)$$

where

- R<sub>CSO</sub> – current limit setting resistor
- V<sub>CSO</sub> - voltage at CSO pin proportional to I<sub>out</sub>
- I<sub>LIM</sub> – current limit value
- I<sub>out</sub> – output current actual value
- RATIO – typical value of Output Current to CSO Current Ratio for particular output current range

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 1.

Once output current reaches its limit value (I<sub>LIM</sub>) set by external resistor R<sub>CSO</sub> than voltage at CSO pin is typically 2.55 V. Calculations of I<sub>LIM</sub> or R<sub>CSO</sub> values can be done using Equation 2 and Equation 3, respectively. Minimum and maximum value of Output Current Limit can be calculated according to Equations 4 and 5.

$$I_{LIM\_min} = RATIO_{min} \times \frac{V_{CSO\_min}}{R_{CSO\_max}} \quad (eq. 4)$$

$$I_{LIM\_max} = RATIO_{max} \times \frac{V_{CSO\_max}}{R_{CSO\_min}} \quad (eq. 5)$$

where

RATIO<sub>min</sub> – minimum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

RATIO<sub>max</sub> – maximum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

V<sub>CSO\_min</sub> - minimum value of CSO Voltage Level at Current Limit from electrical characteristics table

V<sub>CSO\_max</sub> - maximum value of CSO Voltage Level at Current Limit from electrical characteristics table

R<sub>CSO\_min</sub> – minimum value of R<sub>CSO</sub> with respect its accuracy

R<sub>CSO\_max</sub> – maximum value of R<sub>CSO</sub> with respect its accuracy

Designers should consider the tolerance of R<sub>CSO</sub> during the design phase.

**Diagnostic in OFF State**

The NCV47722 contains also circuitry for OFF state diagnostics for Short to Battery (STB) and Open Load (OL). There are internal current source and Pull Down resistors which provide additional cost savings for overall application by excluding external components and their assembly cost and saving PCB space and safe control IOs of a Microcontroller Unit (MCU).

Simplified functional schematic and truth table is shown in Figure 13 and related flowchart in Figure 14.



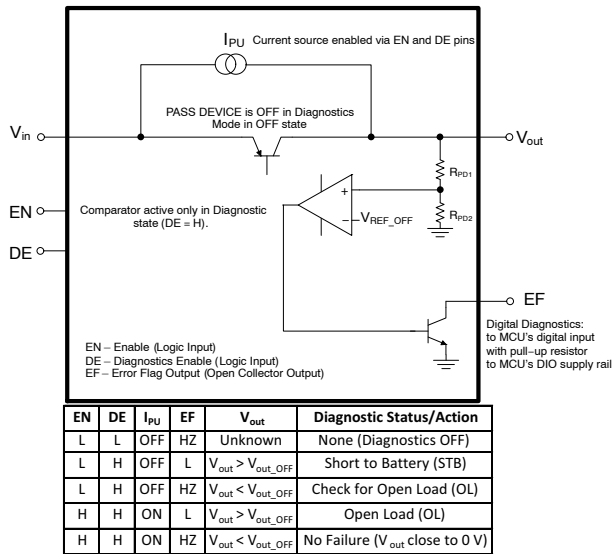


Figure 13. Simplified Functional Diagram of OFF State Diagnostics (STB and OL)

For diagnostics in OFF state the input DE pin has to be put logic high. Logic level on EN pin determines which failure (STB or OL) is diagnosed. For detailed information see Diagnostic Truth Table 7.

**Diagnostic in ON State**

Diagnostic in ON State provides information about Overcurrent or Short to Ground failures, during which the EF output is in logic low state. For detailed information see Diagnostic Features Truth Table 7.

Table 7. DIAGNOSTIC FEATURES TRUTH TABLE

Operational Status	EN	DE	Output Voltage (V <sub>out</sub> )	Diagnostic Output (CSO)	Error Flag (EF)
Disabled	L	L	Low (~0 V)	Low (~0 V)	HZ
Short to Battery	L	H	High (V <sub>out</sub> ~ V <sub>in</sub> )	Low (~0 V)	L (Note 10)
Open Load (OFF)	H	H	High (V <sub>out</sub> ~ V <sub>in</sub> )	Low (~0 V)	L (Note 11)
Normal (OFF)	H	H	Low (~0 V)	Low (~0 V)	HZ (Note 11)
Open Load (ON)	H	L	High (V <sub>out</sub> ~ V <sub>in</sub> )	Low (~0 V)	HZ
Normal (ON)	H	L	High (V <sub>out</sub> ~ V <sub>in</sub> )	Proportional to I <sub>out</sub> (±5%) (Note 12)	HZ
Over Current	H	L	V <sub>in</sub> - 1 V	High (~2.55 V)	L
Short to Ground	H	L	Low (~0 V)	High (~2.55 V)	L

10. Internal current source disabled (between V<sub>out</sub> and V<sub>in</sub>).

11. Internal current source enabled (between V<sub>out</sub> and V<sub>in</sub>).

12. Valid for I<sub>out</sub> = 50 mA to 350 mA. For I<sub>out</sub> = 10 mA to 50 mA range proportional to I<sub>out</sub> (±15%).

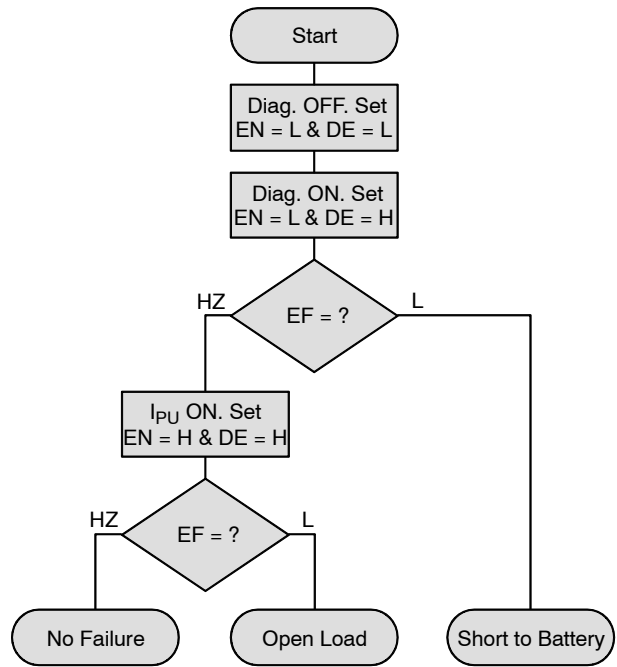


Figure 14. Flowchart for Diagnostics in OFF State

**Thermal Considerations**

As power in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the device can handle is given by:

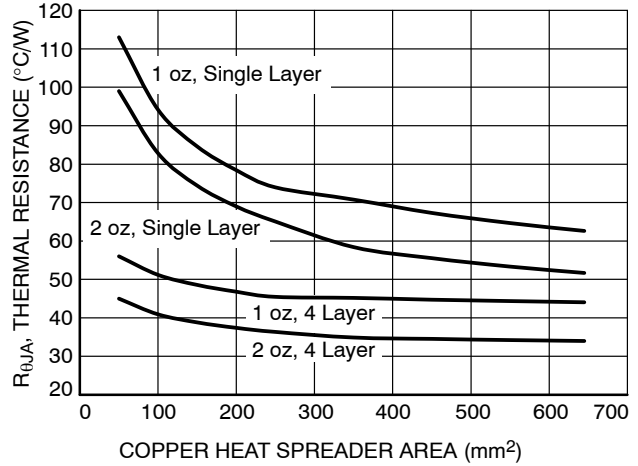
$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 6})$$

Since  $T_J$  is not recommended to exceed  $150^{\circ}\text{C}$ , then the device soldered on  $645 \text{ mm}^2$ , 1 oz copper area, FR4 can dissipate up to 2 W when the ambient temperature ( $T_A$ ) is  $25^{\circ}\text{C}$ . See Figure 15 for  $R_{\theta JA}$  versus PCB area. The power dissipated by the device can be calculated from the following equations:

$$P_D \approx V_{in}(I_q @ I_{out}) + I_{out}(V_{in} - V_{out}) \quad (\text{eq. 7})$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + (V_{out} \times I_{out})}{I_{out} + I_q} \quad (\text{eq. 8})$$



**Figure 15. Thermal Resistance vs. PCB Copper Area**

**Hints**

$V_{in}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

**ORDERING INFORMATION**

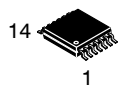
Device	Marking	Package	Shipping†
NCV47722PAAJR2G	Line1: NCV4 Line2: 7722	TSSOP-14 Exposed Pad (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

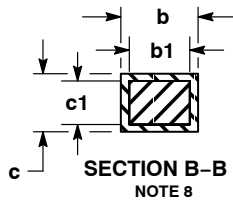
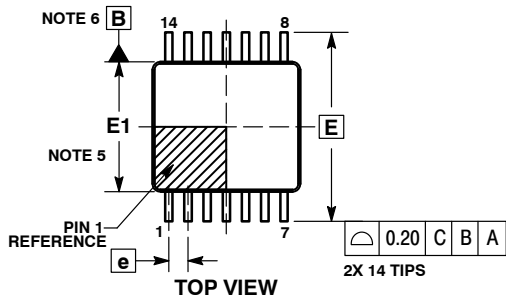
ON Semiconductor®



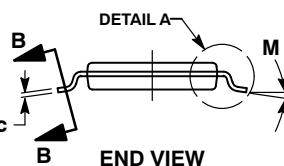
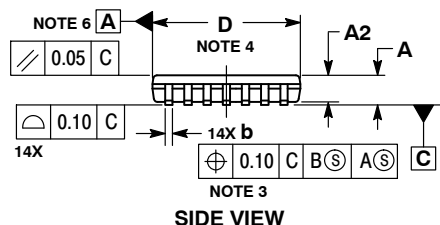
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### TSSOP-14 EP CASE 948AW ISSUE C

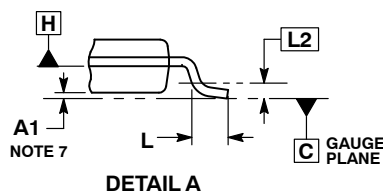
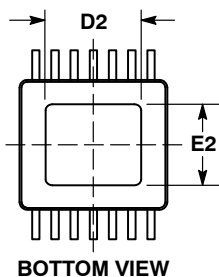
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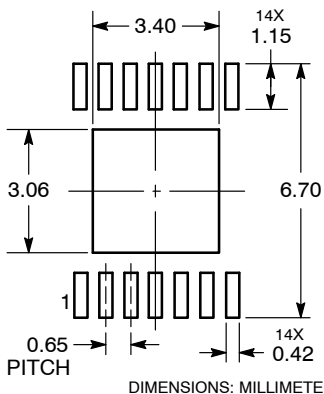
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
  4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
  5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
  6. DATUMS A AND B ARE DETERMINED AT DATUM H.
  7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
  8. SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.



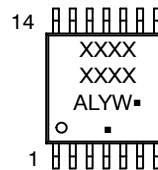
MILLIMETERS		
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0°	8°



### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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