Linear Voltage Regulator - Bias Rail, Low Noise, Very Low Dropout, Programmable Soft-Start
3 A

NCV59745

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Description

The NCV59745 is very low dropout low noise dual−rail voltage regulator that is capable of providing an output current in excess of 3.0 A with a dropout voltage of 115 mV typ. at full load current. This series contains fixed output voltage devices. The high output current capability with high accuracy, broad bandwidth high PSRR and low noise makes this VLDOs ideal for powering noise sensitive high speed communication devices, high end FPGAs and microprocessors.

The NCV59745 is offered in QFNW20 4.0 mm x 4.0 mm package.

Features

- Output Current in Excess of 3.0 A
- 0.25% Typical Accuracy Over Line and Load
- V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range: 2.2 V to 5.5 V
- Output Voltage Range: 0.8 V to 3.6 V
- Dropout Voltage: 105 mV typ. at 3 A
- Programmable Soft Start
- Open Drain Power Good Output
- Low Noise, 6 μV_{RMS} Typically
- Excellent Transient Response
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices, Wettable Flank for AOI

Applications

- High Speed Analog VCO, DAC, ADC
- FPGAs, DSPs, SerDes
- Imaging Sensors and ASICs
- Automotive, Telecom and Industrial Equipment Point of Load Regulation

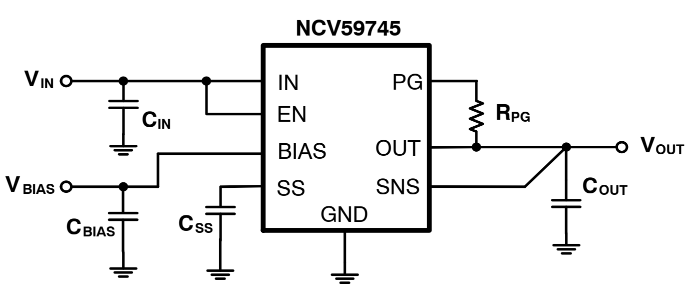
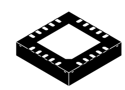
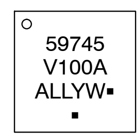


Figure 1. Typical Application Schematic



QFNW20
MW SUFFIX
CASE 484AP

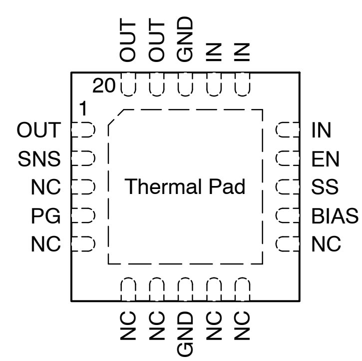
MARKING DIAGRAM



A	=	Assembly Location
LL	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

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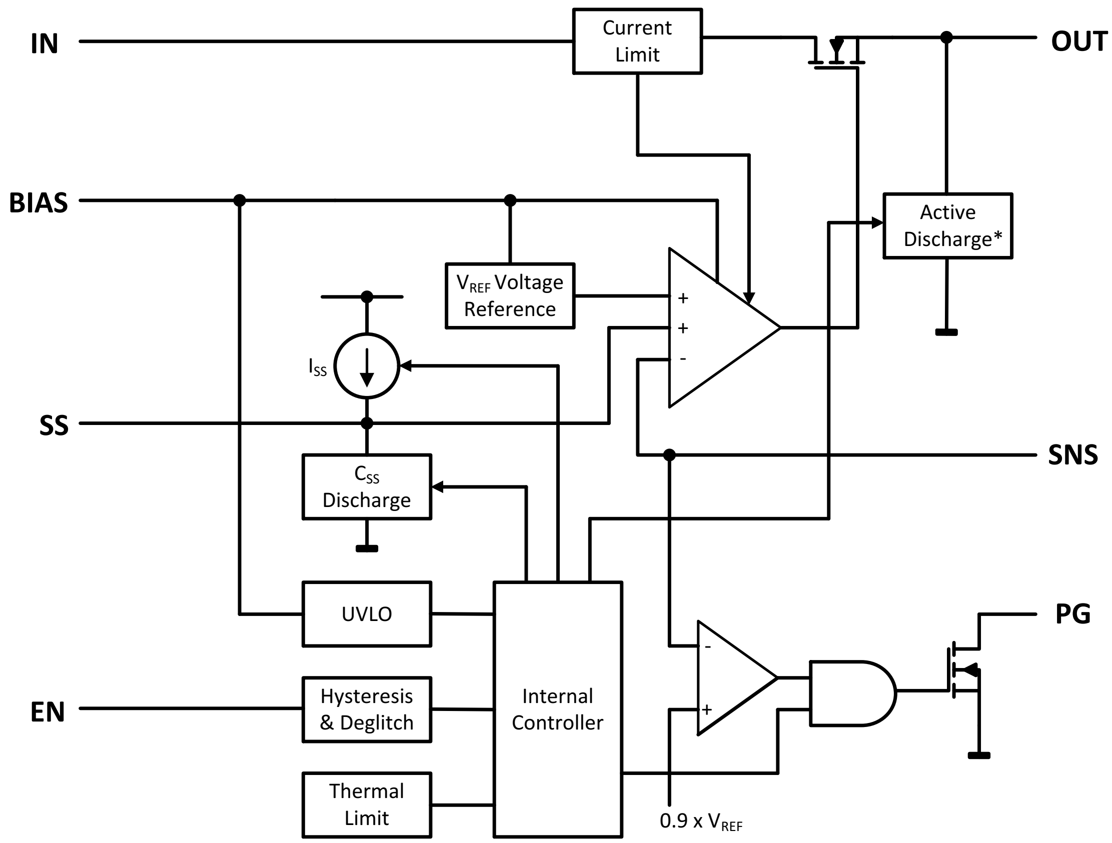


*Active output discharge function is present only in NCV59745A option devices.

Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Name	QFNW20	Description
IN	15–17	Unregulated voltage input to the device.
EN	14	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	13	Soft–Start pin. A capacitor connected on this pin to ground sets the Soft – Start time.
BIAS	12	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	4	Power–Good (PG) is an open–drain, active–high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high–impedance state. When V_{OUT} is below this threshold the pin is driven to a low–impedance state. A pull–up resistor from 10 kΩ to 100 kΩ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SNS	2	Output voltage sense input pin. This pin must not be left floating.
OUT	1, 19, 20	Regulated output voltage. It is recommended that the output capacitor ≥ 10 μF (effective value).
NC	3, 5–7, 9–11	No connection. Each one pin is “true NC” and can be left floating or connected to GND to allow better thermal contact to the PCB top–side plane.
GND	8, 18	Ground pins. Both these pins must be connected to ground.
PAD/TAB		Should be soldered to the ground plane for increased thermal performance

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Voltage Range	V_{IN}	−0.3 to +6	V
Bias Voltage Range	V_{BIAS}	−0.3 to +6	V
Enable Voltage Range	V_{EN}	−0.3 to +6	V
Power−Good Voltage Range	V_{PG}	−0.3 to +6	V
PG Sink Current	I_{PG}	0 to +1.5	mA
SS Pin Voltage Range	V_{SS}	−0.3 to (V_{BIAS} + 0.3) ≤ 6	V
Output Sense Pin Voltage Range	V_{SNS}	−0.3 to +6	V
Output Voltage Range	V_{OUT}	−0.3 to (V_{IN} + 0.3) ≤ 6	V
Maximum Output Current	I_{OUT}	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	P_D	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Junction Temperature Range	T_{STG}	−55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002
   ESD Charged Device Model tested per AEC−Q100−011
   Latch−up Current Maximum Rating ±100 mA per AEC−Q100−004.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFNW20, 4.0x4.0, 0.5P package			
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction−to−Board (Note 6)	$R_{\theta JB}$	3.6	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	27	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 7)	$R_{\theta JC(bot)}$	3.6	°C/W
Characterisation Parameter, Junction−to−Top	Ψ_{JT}	1.0	°C/W
Characterisation Parameter, Junction−to−Board	Ψ_{JB}	3.5	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Thermal data are derived by thermal simulations based on methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:
   These data were generated with only a single device at the center of a high−K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines. Top and Bottom layer 2 oz. copper, inner planes 1 oz. copper.
   The exposed pad is connected to the PCB ground inner layer through a 3 x 3 thermal via array. Vias are 0.3 mm diameter, plated.
5. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
6. The junction−to−board thermal resistance is simulated in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51−8.
7. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 8)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	V_{OUT} + V_{DO}	5.5	V
Bias Voltage	V_{BIAS}	V_{OUT} + 1.6	5.5	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS (At V_{EN} = 1.1 V, V_{IN} = $V_{OUT(NOM)}$ + 0.25 V, C_{BIAS} = 1 μF, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		V_{OUT} +V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		V_{OUT} + 1.4		5.5	V
UVLO	Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	1.2 –	1.5 0.45	2.0 –	V
V_{OUT}	Accuracy	2.4 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.6 V ≤ V_{BIAS} 50 mA ≤ I_{OUT} ≤ 3.0 A	−1.0	±0.3	+1.0	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT(NOM)}$ + 0.25 ≤ V_{IN} ≤ 5.5 V		0.0006		%/V
V_{OUT}/I_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.005		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.01		%/A
V_{DO}	V_{IN} dropout voltage (Note 9)	I_{OUT} = 3.0 A, V_{BIAS} – $V_{OUT(NOM)}$ = 1.6 V		105	195	mV
	V_{BIAS} dropout voltage (Note 9)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}		1.2	1.4	V
I_{CL}	Current limit	V_{OUT} = 80% x $V_{OUT(NOM)}$	3.5	4.3	7	A
I_{BIAS}	Bias pin current	0 mA ≤ I_{OUT} ≤ 3.0 A		1.3	2	mA
I_{BSHDN}	V_{BIAS} shutdown current	V_{EN} ≤ 0.4 V		1	15	μA
I_{INSHDN}	V_{IN} shutdown current	V_{EN} ≤ 0.4 V, V_{OUT} = 0 V		1	15	μA
I_{SNS}	Sense pin current	0 mA ≤ I_{OUT} ≤ 3.0 A	−250	95	250	nA
PSRR	Power−supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		75		dB
		3 MHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		18		
	Power−supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		75		dB
		3 MHz, I_{OUT} = 2 A, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		18		
Noise	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 2 A		6		μVrms
t_{STRT}	Minimum startup time	I_{OUT} = 3 A, C_{SS} = open (Note 10)		350		μs
I_{SS}	Soft−start charging current	V_{SS} = 0.4 V		$6.2 \times \frac{V_{OUT(NOM)}}{0.8\ V}$		μA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,HYS}$	Enable pin hysteresis			100		mV
$V_{EN,DG}$	Enable pin deglitch time			20		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.3	1	μA
V_{IT-}	PG trip threshold	V_{OUT} decreasing	82	88	93	%V_{OUT}
V_{IT+}	PG trip threshold	V_{OUT} increasing	83	91	96	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	μA
R_{AD}	Output Active Discharge Resistance (NCV59745A option only)	V_{BIAS} = 5.0 V, V_{EN} = 0 V, V_{IN} = 1.25 V, V_{OUT} = 1.0 V		600		Ω
TSD	Thermal shutdown temperature	Shutdown, temperature increasing Reset, temperature decreasing		+165 +140		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 3% below nominal.
10. Time from EN rising edge to 98% of $V_{OUT(NOM)}$

TYPICAL CHARACTERISTICS

At T_J = +25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.25 V, $V_{BIAS} = V_{OUT(NOM)}$ + 1.6 V, V_{EN} = 1.1 V, $V_{OUT(NOM)}$ = 1.0 V, C_{IN} = 10 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance value), unless otherwise noted.

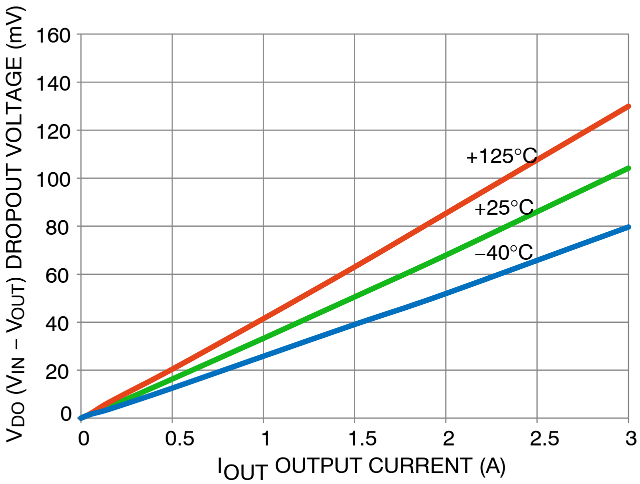


Figure 3. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

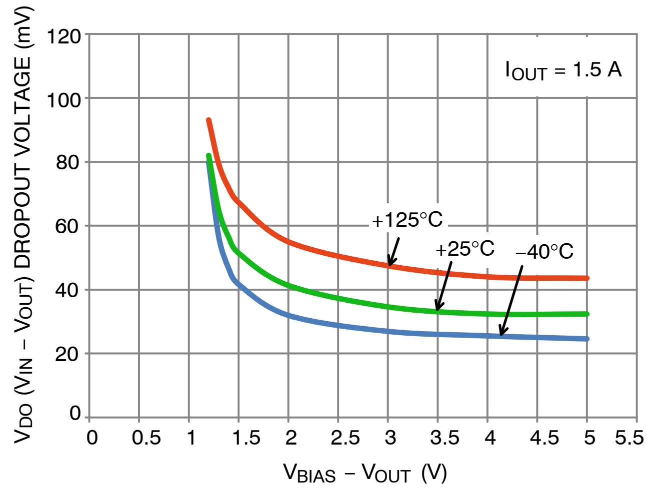


Figure 4. V_{IN} Dropout Voltage vs. (V_{BIAS} − V_{OUT}) and Temperature T_J

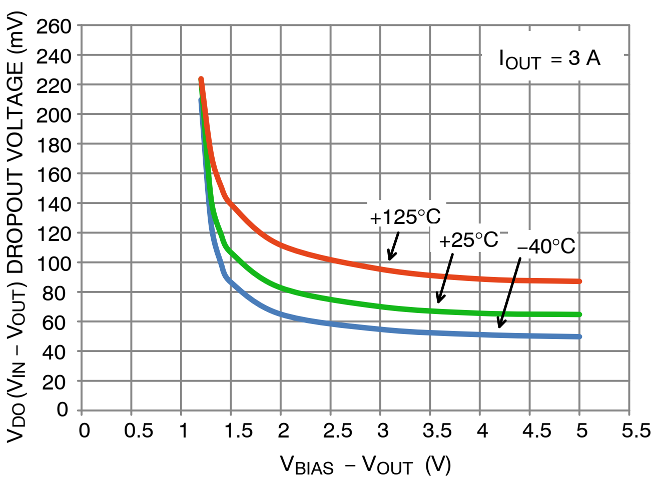


Figure 5. V_{IN} Dropout Voltage vs. (V_{BIAS} − V_{OUT}) and Temperature T_J

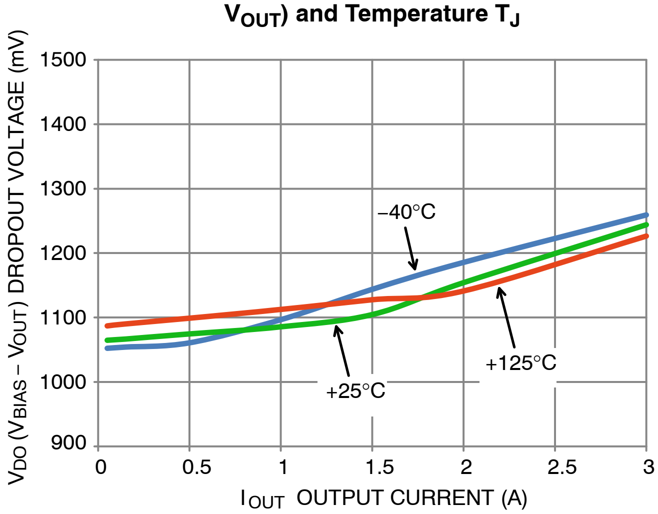


Figure 6. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_J

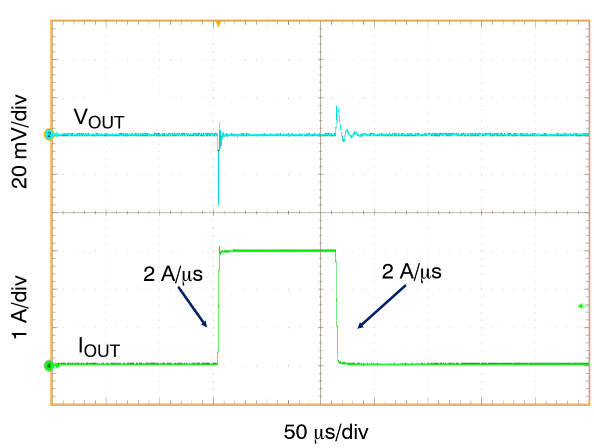


Figure 7. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 10 μF MLCC

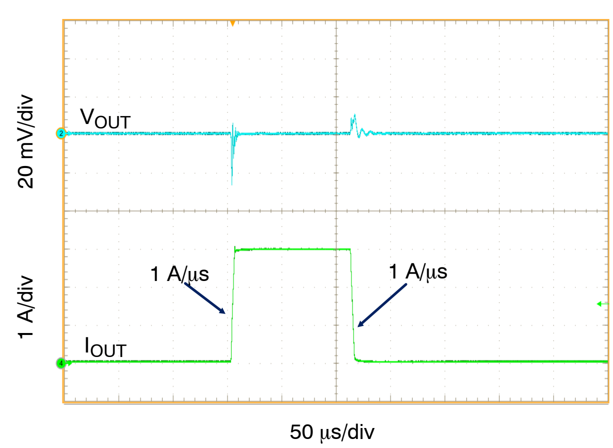


Figure 8. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 10 μF MLCC

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.25 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.6 V, V_{EN} = 1.1 V, $V_{OUT(NOM)}$ = 1.0 V, C_{IN} = 10 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance value), unless otherwise noted.

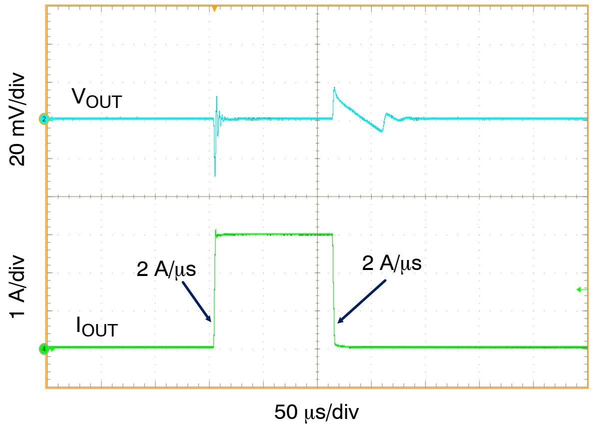


Figure 9. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 47 μF MLCC

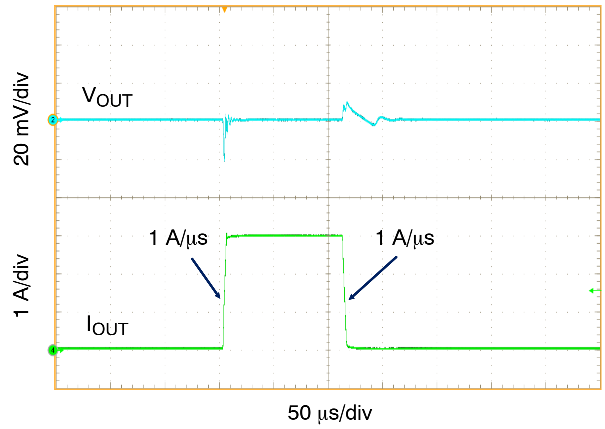


Figure 10. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 47 μF MLCC

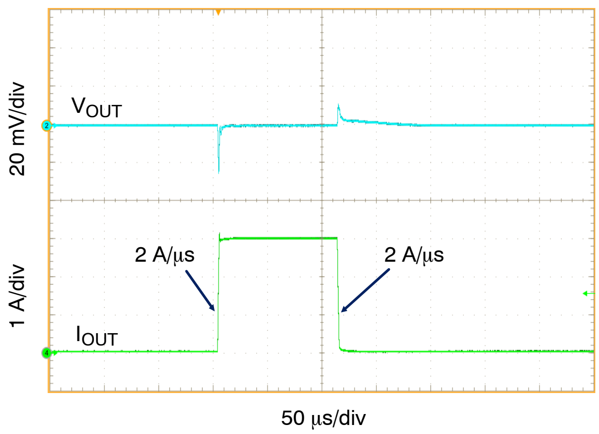


Figure 11. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 330 μF Tantalum Polymer Cap + 3x 10 μF MLCC

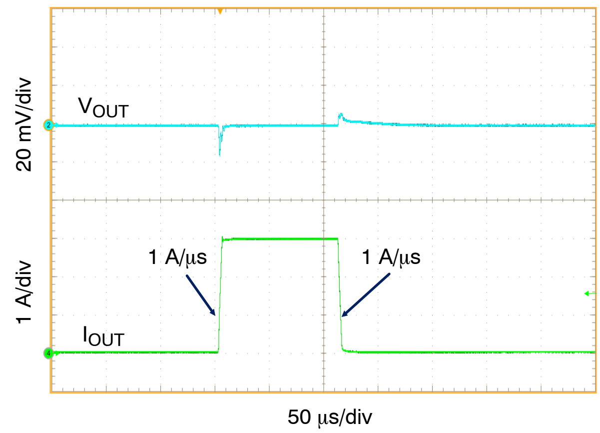


Figure 12. Load Transient Response, I_{OUT} = 10 mA to 3 A, C_{OUT} = 330 μF Tantalum Polymer Cap + 3x 10 μF MLCC

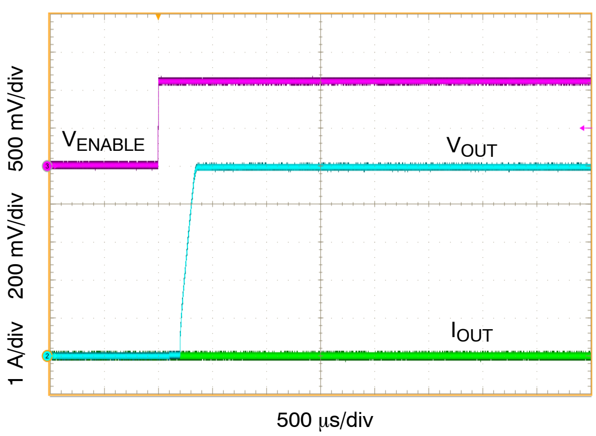


Figure 13. Enable Transient Response, I_{OUT} = 0 A, C_{OUT} = 10 μF MLCC, C_{SS} = 0 nF

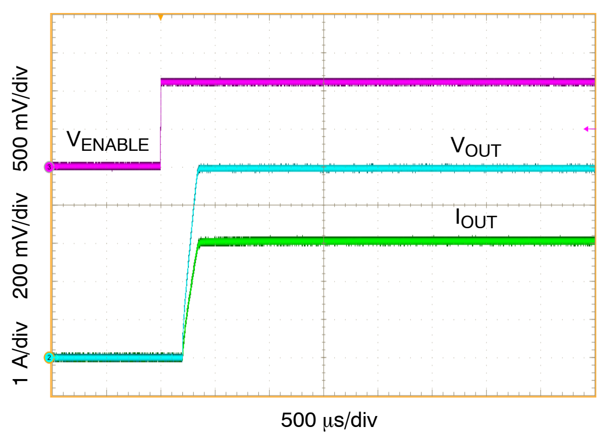


Figure 14. Enable Transient Response, I_{OUT} = 3 A, C_{OUT} = 10 μF MLCC, C_{SS} = 0 nF

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.25 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.6 V, V_{EN} = 1.1 V, $V_{OUT(NOM)}$ = 1.0 V, C_{IN} = 10 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance value), unless otherwise noted.

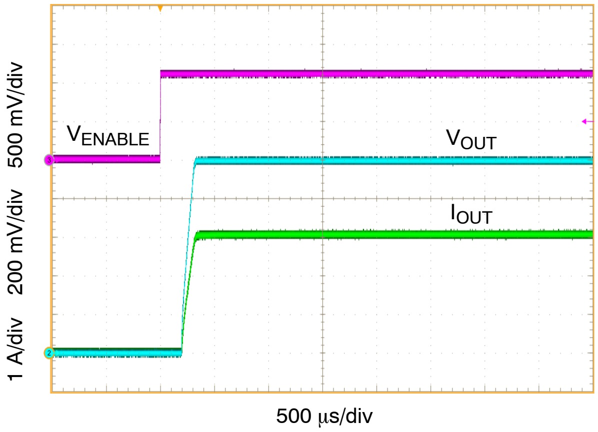


Figure 15. Enable Transient Response, I_{OUT} = 3 A, C_{OUT} = 47 μF MLCC, C_{SS} = 0 nF

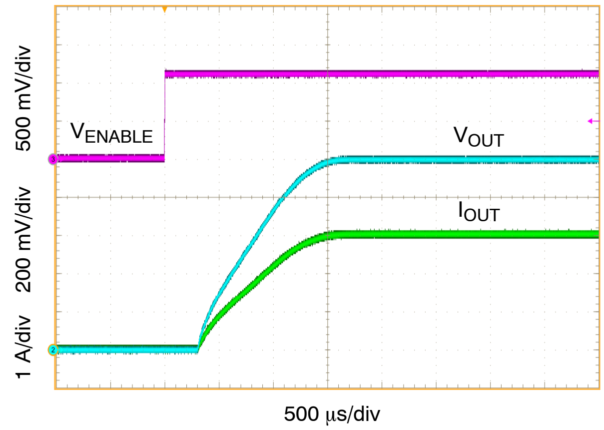


Figure 16. Enable Transient Response, I_{OUT} = 3 A, C_{OUT} = 330 μF Tantalum Polymer Cap + 3x 10 μF MLCC, C_{SS} = 10 nF

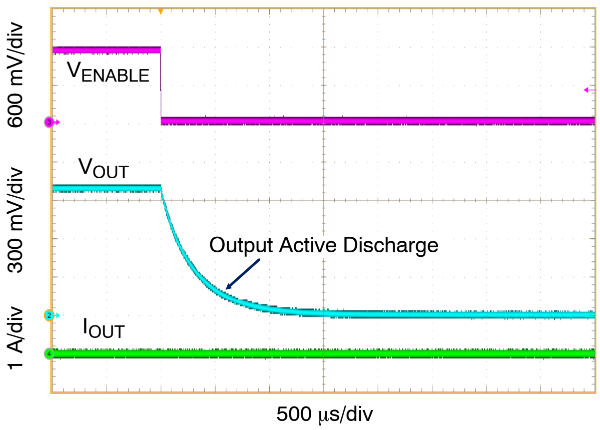


Figure 17. Enable Transient Response, I_{OUT} = 0 A, C_{OUT} = 47 μF MLCC, C_{SS} = 0 nF

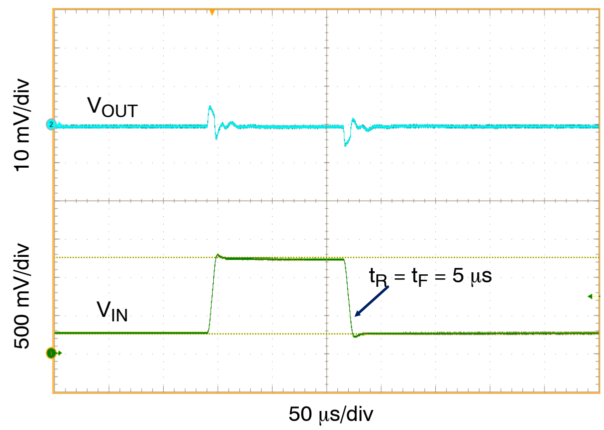


Figure 18. V_{IN} Line Transient Response, V_{IN} = 1.25 V to 2.25 V, I_{OUT} = 0 mA, C_{IN} = 0, C_{OUT} = 10 μF MLCC

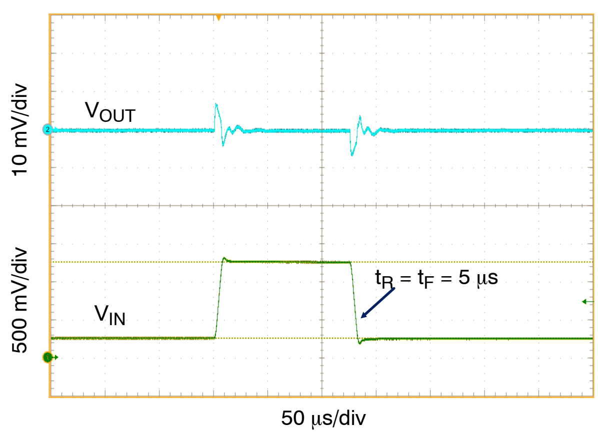


Figure 19. V_{IN} Line Transient Response, V_{IN} = 1.25 V to 2.25 V, I_{OUT} = 3 A, C_{IN} = 0, C_{OUT} = 10 μF MLCC

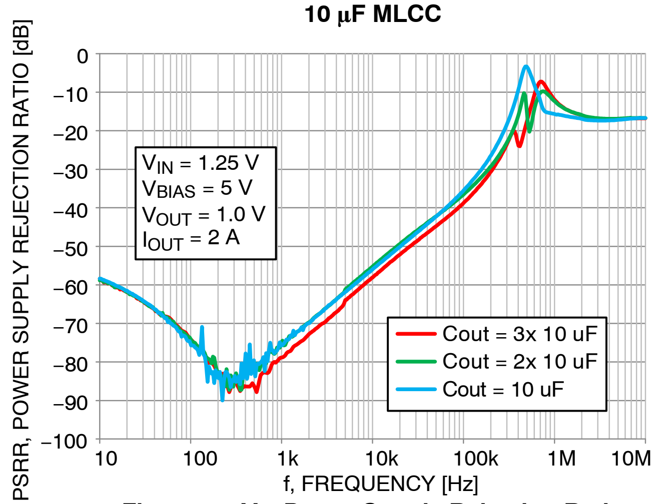


Figure 20. V_{IN} Power Supply Rejection Ratio vs. Frequency

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.25 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.6 V, V_{EN} = 1.1 V, $V_{OUT(NOM)}$ = 1.0 V, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (effective capacitance value), unless otherwise noted.

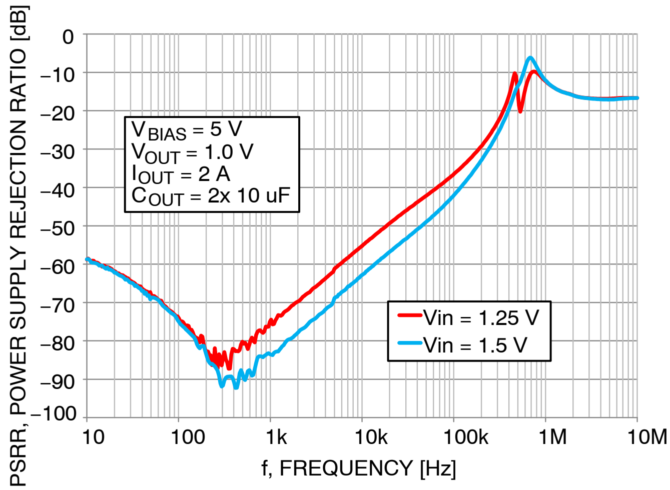


Figure 21. V_{IN} Power Supply Rejection Ratio vs. Frequency

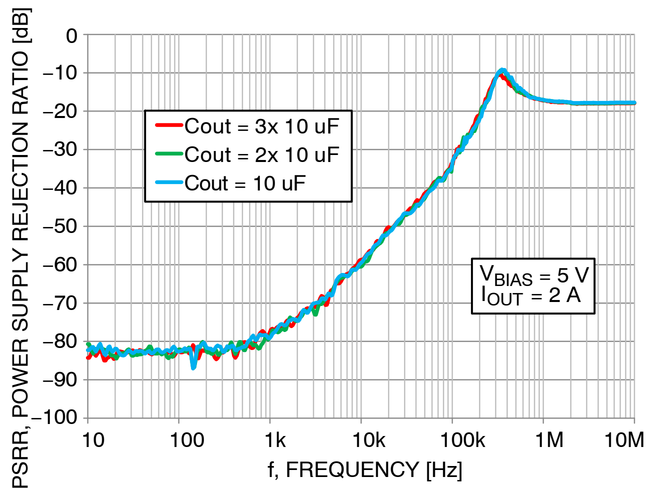


Figure 22. V_{BIAS} Power Supply Rejection Ratio vs. Frequency

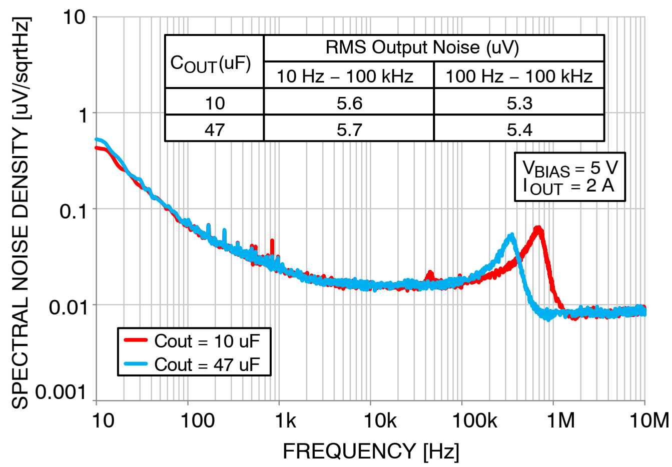


Figure 23. Output Voltage Noise Spectral Density

APPLICATIONS INFORMATION

The NCV59745 very low dropout low noise dual−rail voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal controll circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

The NCV59745 offers programmable smooth monotonic start−up. The controlled voltage rising limits the inrush current what is advantageous in applications with large capacitive loads. The Voltage Controlled Soft Start time is programmable by external C_{SS} capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter.

Open Drain type Power Good (PG) output is available for Vout monitoring and sequencing of other devices.

NCV59745 is a Fixed Voltage linear regulator.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} – V_{OUT}$) when V_{OUT} starts to decrease by percents specified in the Electrical Characteristics table. V_{BIAS} is high enough, specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} – V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with effective capacitance in the range from 10 μF up to 1000 μF. The device is also stable with multiple capacitors in parallel.

In applications where no low input supply impedance is available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as an example) the recommended $C_{BIAS} \geq 1$ μF and $C_{IN} \geq 4.7$ μF of effective capacitance value. For the best performance all capacitors should be connected to the NCV59745 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. To get the full functionality of Soft Start, it is recommended to turn on the V_{IN} and V_{BIAS} supply voltages first and activate the Enable pin no sooner than V_{IN} and V_{BIAS} are on their nominal levels. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

Programmable Soft−Start

The Soft−Start time is programmable by external C_{SS} capacitor value. If C_{SS} capacitor not used, the device is starting with Minimum Start−up time specified in the Electrical Characteristics table.

The output voltage ramping time during Soft−Start depends on the Soft−Start charging current I_{SS} and Soft−Start capacitor value C_{SS}.

The Soft–Start time can be calculated using following equation:

$t_{SS} = C_{SS} \times 0.13$

where

t_{SS} = Soft−Start time in miliseconds

C_{SS} = Soft−Start capacitor value in nano Farads

Soft−Start time vs C_{SS} capacitor value examples can be found in the Table 6. The maximal recommended value of C_{SS} capacitor is 1 μF.

Unlike other LDO devices with external Noise Reduction / Soft−Start capacitor, the C_{SS} capacitor value has no connection with NCV59745 noise performance. After the Soft−Start phase the SS pin voltage persists in ramping up to the V_{BIAS} supply level.

Table 6. CAPACITOR VALUES FOR PROGRAMMING THE SOFT−START TIME

Css	Soft−Start Time
Open	0.35 ms
4.7 nF	0.6 ms
10 nF	1.3 ms
47 nF	6 ms
100 nF	13 ms

Output Noise

Internal Noise Reduction filter is implemented to reduce the output voltage noise. Unlike LDO devices with external noise reduction capacitor this solution is not sensitive to the external capacitor quality.

Output Active Discharge

The NCV59745A option devices are equipped with Output Active Discharge feature. When EN input level is Low and/or Thermal Shutdown is active, the Output Active Discharge transistor is On and the output voltage node V_{OUT} is pulled down to GND through a 600 Ω resistor. The C_{OUT} output capacitor is discharged what is advantageous for applications requiring next V_{OUT} Start−Up ramping from 0 V.

Power Good

Power−Good (PG) is an open−drain, logic active−high output that indicates the status of the Output Voltage V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state. When V_{OUT} is below this threshold the pin is driven to a low−impedance state pulling the PG pin to GND. An external pull−up resistor from 10 kΩ to 100 kΩ should be connected from this pin to a supply up to 5.5 V. The supply voltage can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

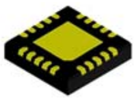
Power Dissipation

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

Table 7. ORDERING INFORMATION

Device	Output Current	Output Voltage	Option	Marking	Wettable Flank	Package	Shipping†
NCV59745AMW100TAG	3.0 A	1.00 V	Output Active Discharge	59745 V100A	SLP Step cut	QFNW20 (Pb−Free)	3000 / Tape & Reel
NCV59745AMW1015TAG	3.0 A	1.015 V	Output Active Discharge	59745 V1015A	SLP Step cut	QFNW20 (Pb−Free)	3000 / Tape & Reel
NCV59745AMW180TAG	3.0 A	1.80 V	Output Active Discharge	59745 V180A	SLP Step cut	QFNW20 (Pb−Free)	3000 / Tape & Reel
NCV59745AMW250TAG	3.0 A	2.50 V	Output Active Discharge	59745 V250A	SLP Step cut	QFNW20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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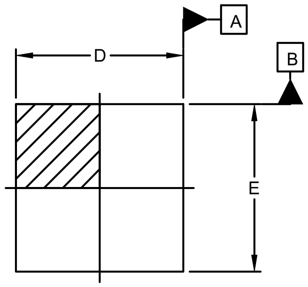
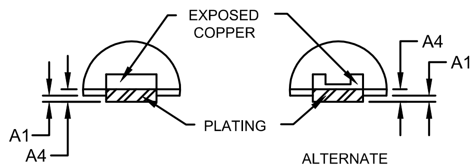
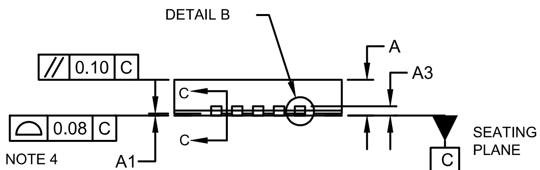


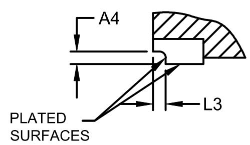
TOP VIEW



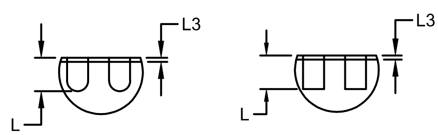
DETAIL B



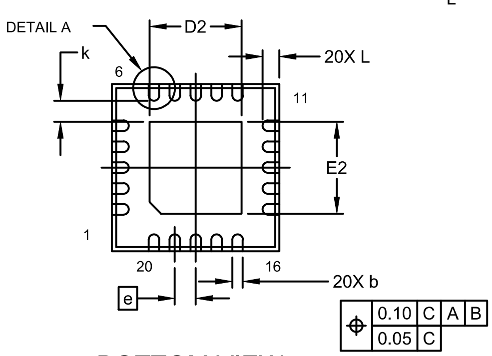
SIDE VIEW



SECTION C-C



DETAIL A

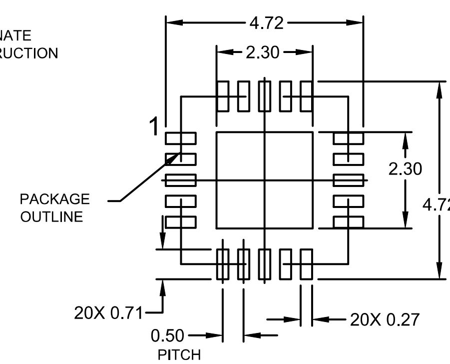


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.10	2.20	2.30
E	3.90	4.00	4.10
E2	2.10	2.20	2.30
e	0.50 BSC		
k	0.50 REF		
L	0.30	0.40	0.50
L3	0.05 REF		



RECOMMENDED MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
ALLYW▪
▪

XXXXXX = Specific Device Code
A = Assembly Location
LL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

(Note: Microdot may be in either location)

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DESCRIPTION:	**QFNW20 4x4, 0.5P**	**PAGE 1 OF 1**

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