NCV70501

Micro-Stepping Motor Driver

ON Semiconductor®

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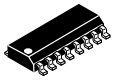
Introduction

NCV70501 is a micro−stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. The NCV70501 contains a current−translation table and takes the next micro−step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (= direction) register or input pin. The chip provides an error message if stall, an electrical error or an elevated junction temperature is detected. It is using a proprietary PWM algorithm for reliable current control.

NCV70501 is fully compatible with the automotive voltage requirements and is ideally suited for general−purpose low current range stepper motor applications in the automotive, industrial, medical, and marine environment.

Features

- Dual H−Bridge for 2−Phase Stepper Motors
- Programmable Peak−Current Up to 300 mA
- On−Chip Current Translator
- SPI Interface With Daisy Chain Capability
- 6 Step Modes from Full−Step up to 16 Micro−Steps
- Fully Integrated Current−Sensing and Current−Regulation
- On Chip Stall Detection
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Fixed PWM Frequency
- Active Fly−Back Diodes
- Full Output Protection and Diagnosis
- Thermal (Warning and) Shutdown
- Compatible with 3.3 V Microcontrollers, 5 V Tolerant Inputs, 5 V Tolerant Open Drain Outputs
- Reset Function
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

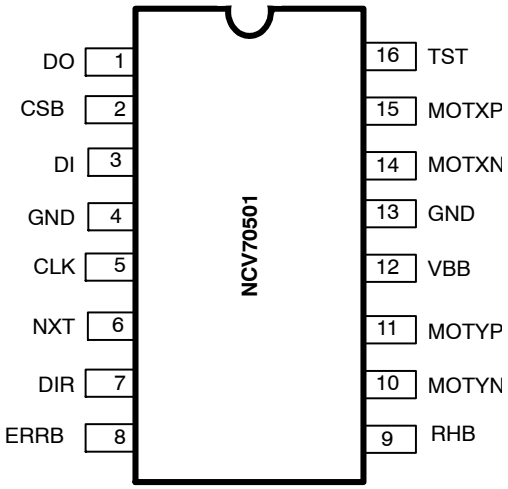


SOIC−16
CASE 751B

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

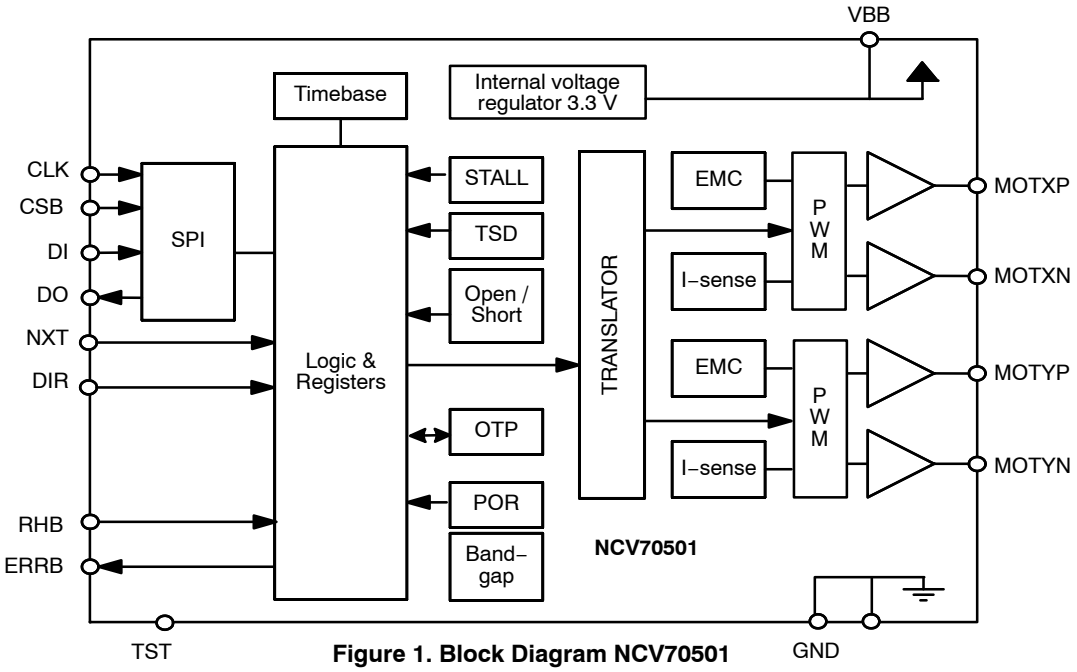


Figure 1. Block Diagram NCV70501

Table 1. PIN LIST AND DESCRIPTION

Name	Pin	Description
DO	1	SPI data output
CSB	2	SPI chip select input
DI	3	SPI data input
GND	4	Ground
CLK	5	SPI clock input
NXT	6	Next micro−step input
DIR	7	Direction input
ERRB	8	Error Output
RHB	9	Run/Hold Current selection input
MOTYN	10	Negative end of phase Y coil output
MOTYP	11	Positive end of phase Y coil output
VBB	12	Voltage supply Input
GND	13	Ground
MOTXN	14	Negative end of phase X coil output
MOTXP	15	Positive end of phase X coil output
TST	16	Test pin input (to be tied to ground in normal operation)

DEVICE ORDERING INFORMATION

Part Number	Temperature Range	Package Type	Peak Current	Shipping†
NCV70501DW002G*	−40°C – 125°C	SOIC−16, 150 mil (Pb−Free)	300 mA	Tube
NCV70501DW002R2G*	−40°C – 125°C	SOIC−16, 150 mil (Pb−Free)	300 mA	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Qualified for automotive applications.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply voltage (Note 1)	−0.3	+36	V
V_{ESD}	Electrostatic discharges on component level (Note 2)	−2	+2	kV
T_{strg}	Storage Temperature	−55	+160	°C
T_J	Junction Temperature (Note 3)	−50	+175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. For limited time < 0.5 s.
2. Human body model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B).
3. Circuit functionality not guaranteed.

Table 3. THERMAL RESISTANCE

Package	Junction−to−Ambient			Unit
	1S0P Board	2S0P Board	2S2P Board	
SOIC−16	96	81	72	K/W

EQUIVALENT SCHEMATICS

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

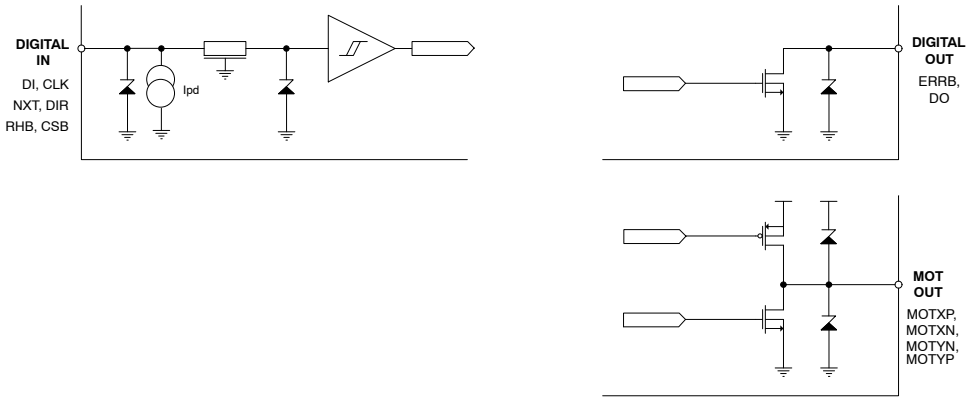


Figure 2. Input and Output Equivalent Diagram

ELECTRICAL SPECIFICATION

Recommended Operating Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 5) is a substantial part of the operation conditions, hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply	+6	+29	V
T_J	Junction temperature	−40	+145 (Note 4)	°C
V_{DIGIO}	Digital I/Os Voltage	0	5.5	V

4. Operating above thermal warning level is limited in time.
5. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.

Table 5. DC PARAMETERS

The DC parameters are given for V_{BB} and T_J in the recommended operating ranges unless otherwise specified.
Convention: Currents flowing into the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Supply Inputs							
V_{BB}	V_{BB}	Nominal operating supply range		6		29	V
I_{BB}		Total current consumption (Note 9)	Unloaded outputs			15	mA
I_{BBs}		Sleep current (Note 10)			90	150	μA
Motordriver							
I_{MDmax} (Peak)	MOTXP MOTXN MOTYP MOTYN	Max peak current through motor coil in normal operation			300		mA
I_{MDabs}		Absolute error on coil current	At I_{MDmax}, Peak = 300 mA	−12		12	%
I_{MDrel}		Error on current ratio I_{coilx} / I_{coily}	At I_{MDmax}, Peak = 300 mA	−9		9	%
R_{ls}		On resistance LOW SIDE driver, high current range, ambient temperature (Note 11)	V_{BB} = 12 V, T_J = 27°C		1.3		Ω
		On resistance low side driver, high current range, high temperature	V_{BB} = 12 V, T_J = 150°C		2.7	3.8	Ω
R_{hs}		On resistance HIGH SIDE driver, high current range, ambient temperature (Note 11)	V_{BB} = 12 V, T_J = 27°C		2.0		Ω
		On resistance high side driver, high current range, high temperature	V_{BB} = 12 V, T_J = 150°C		4.1	5.8	Ω
R_{mpd}		Motor pin pulldown resistance	HiZ Mode		70		kΩ
Logic Inputs							
V_{inL}	DI, CLK NXT, DIR RHB	Logic low input level, max	Tested at 1 MHz frequency			0.8	V
V_{inH}		Logic high input level, min	Tested at 1 MHz frequency	2.4			V
I_{inL}		Logic low input level, max	Tested at 1 MHz frequency	−1			μA
I_{inH}		Logic high input level, max	Tested at 1 MHz frequency			4	μA
V_{inL}	CSB	Logic low input level, max	Tested at 1 MHz frequency			0.8	V
V_{inH}		Logic high input level, min	Tested at 1 MHz frequency	2.4			V
I_{inL}		Logic low input level, max (Note 8)	Tested at 1 MHz frequency		−50		μA
I_{inH}		Logic high input level, max (Note 8)	Tested at 1 MHz frequency			1	μA
R_{pd}	TST0	Internal pulldown resistor		3		9	kΩ
Logic Outputs							
V_{OLmax}	DO	Output voltage when sinking 8 mA				0.4	V
V_{OHmax}		Maximum drain voltage	Pin in open drain state			5.5	V
I_{OLmax}		Maximum allowed drain current				8	mA
V_{OLmax}	ERRB	Output voltage when sinking 8 mA				0.4	V
V_{OHmax}		Maximum drain voltage	Pin in open drain state			5.5	V
I_{OLmax}		Maximum allowed drain current				8	mA
Thermal Warning and Shutdown							
T_{tw}		Thermal warning			145		°C
T_{tsd} (Notes 6, 7)		Thermal shutdown			T_{tw} + 20		°C

6. No more than 100 cumulated hours in life time above T_{tw}.
7. Thermal shutdown is derived from thermal warning.
8. CSB has an internal weak pullup resistor of 100 kΩ.
9. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs, TST input tied to GND.
10. All analog cells in powerdown. Logic powered, no clocks running. All outputs unloaded, no floating inputs.
11. Characterization value, not measured in production.

Table 6. AC PARAMETERS

The AC parameters are given for V_{BB} and temperature in their operating ranges.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Internal Oscillator							
f_{osc}		Frequency of internal oscillator		7	8	9	MHz
Motordriver							
f_{PWM}	MOTxx	PWM frequency	Derived from internal oscillator	19.9	22.8	25.7	kHz
T_{OCdet}	MOTxx	Open coil detection with PWM = 100%	Derived from internal oscillator		50		ms
T_{brise}	MOTxx	Turn−on transient time, 10% to 90%, I_{MD} = 200 mA	SPI bit EMC[1,0] = 00		130		ns
			SPI bit EMC[1,0] = 01		180		
			SPI bit EMC[1,0] = 10		270		
T_{bfall}	MOTxx	Turn−off transient time, 90% to 10%, I_{MD} = 200 mA	SPI bit EMC[1,0] = 00		110		ns
			SPI bit EMC[1,0] = 01		150		
			SPI bit EMC[1,0] = 10		230		
Digital Outputs							
T_{H2L}	DO ERRB	Output fall−time (90% to 10%) from V_{inH} to V_{inL}	Capacitive load 200pF and pullup resistor of 1.5 kΩ			50	ns
Hard Reset Function							
t_{hr_trig}	DIR	Hard reset trigger time	See hard reset function	5		200	μs
t_{hr_dr}	DIR	Hard reset DIR pulse width		2.5		T_{hr_trig}−2.5	μs
t_{hr_set}	RHB	RHB setup time		5			ms
t_{hrerr}	ERRB	Hard reset error indication			1		ms
t_{CSB_with}	CSB	CSB wake−up low pulse width		1		150	μs
t_{wu}	CSB	Wake−up time	See Sleep Mode	250			μs
NXT/DIR Inputs							
t_{NXT_HI}	NXT	NXT minimum, high pulse width (Note 12)		2			μs
t_{NXT_LO}	NXT	NXT minimum, low pulse width (Note 12)		2			μs
t_{DIR_SET}	NXT, DIR	NXT hold time, following change of DIR (Note 12)		500			μs
t_{DIR_HOLD}	NXT, DIR	NXT hold time, before change of DIR (Note 12)		500			μs

12. Characterization value, not measured in production.

Table 7. BEMF MEASUREMENT − 5 bits ADC

Symbol	Pins	Parameter	Remark/Test Condition	Min	Typ	Max	Unit
$BEMF_{DIFF\_R}$	MOTxx	BEMF input range differential		−3.75		3.75	V
$BEMF_{LSB}$	MOTxx	BEMF equivalent LSB value			125		mV
$BEMF_{FULL\_SC}$	MOTxx	BEMF measurement full scale		3.48	3.875	4.26	V

Table 8. SPI TIMING PARAMETERS

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLK}	SPI clock period	1			μs
t_{HI_CLK}	SPI clock high time	200			ns
$t_{CLKRISE}$	SPI clock rise time			1	μs
$t_{CLKFALL}$	SPI clock fall time			1	μs
t_{LO_CLK}	SPI clock low time	200			ns
t_{SET_DI}	DI set up time, valid data before rising edge of CLK	50			ns
t_{HOLD_DI}	DI hold time, hold data after rising edge of CLK	50			ns
t_{HI_CSB}	CSB high time	2.5			μs
$t_{SET\_CSB\_LO}$	CSB set up time, CSB low before rising edge of CLK (Note 13)	1			μs
$t_{CLK\_CSB\_HI}$	CSB set up time, CSB high after rising edge of CLK	200			ns
$t_{DEL\_CSB\_DO}$	DO delay time, DO settling time after CSB low (Note 14)			250	ns
$t_{DEL\_CLK\_DO}$	DO delay time, DO settling time after CLK low (Note 14)			100	ns

13. After leaving sleep mode an additional wait time of 250 μs is needed before pulling CSB low.
14. Specified for a capacitive load 10 pF and a pullup resistor of 1.5 kΩ.

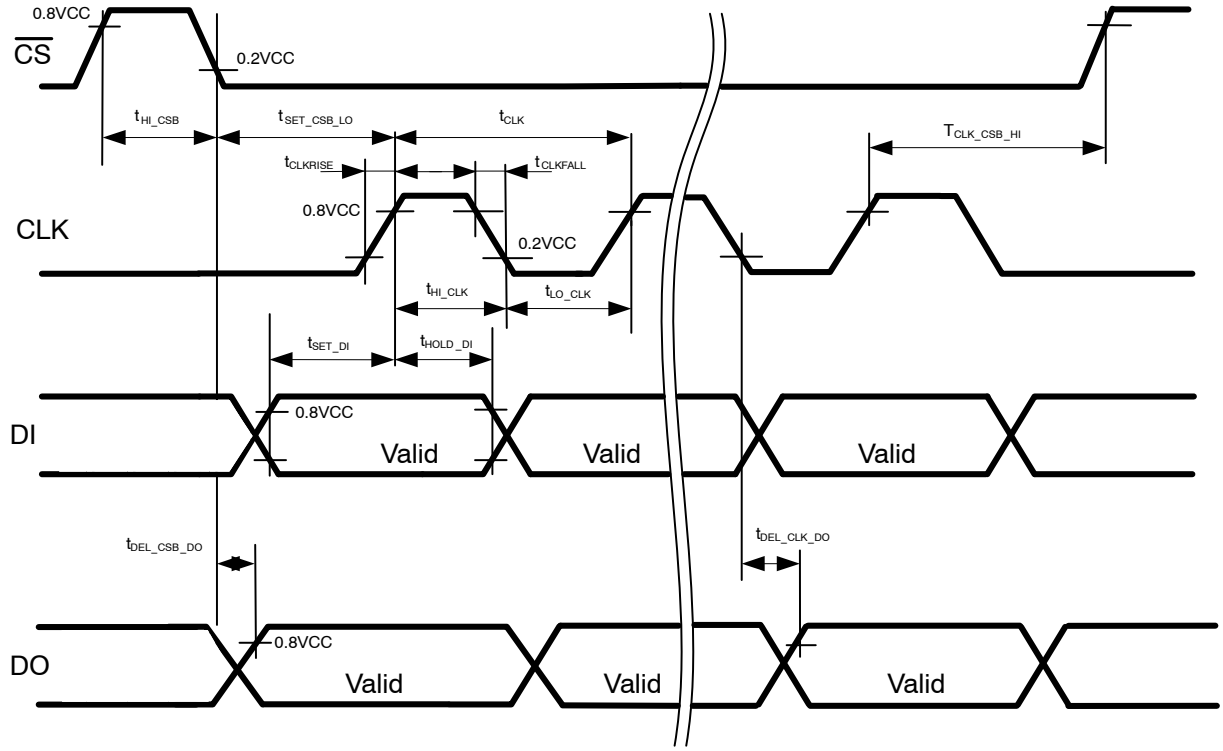


Figure 3. SPI Timing

TYPICAL APPLICATION SCHEMATIC

The application schematic below shows typical connections for applications with low axis counts and/or with software SPI implementation. For applications with many stepper motor drivers, some “minimal wiring” examples are shown at the last sections of this datasheet.

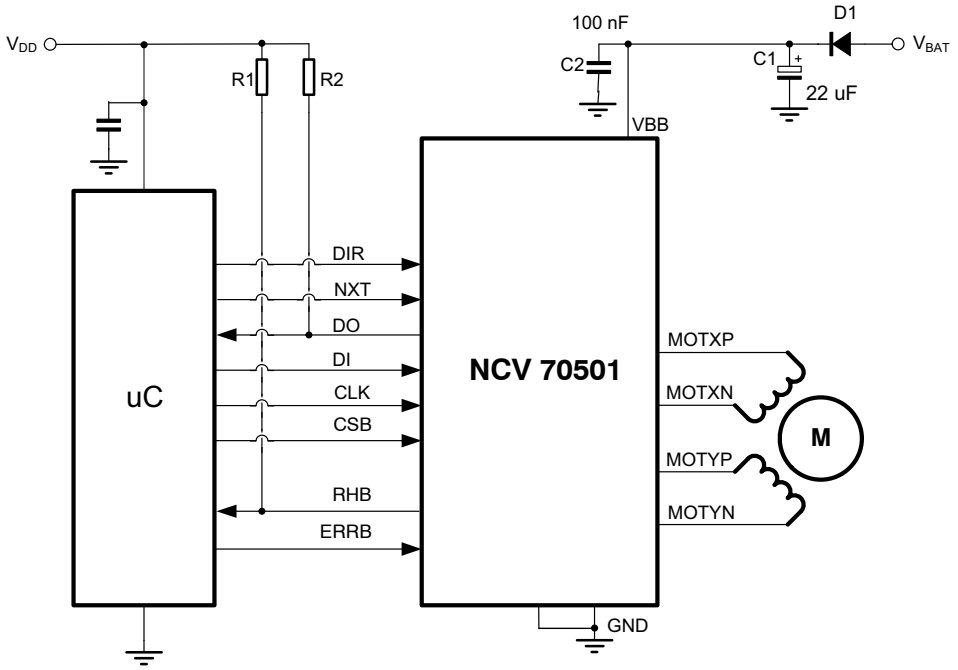


Figure 4. Typical Application Schematic NCV70501

Table 9. EXTERNAL COMPONENTS LIST AND DESCRIPTION

Component	Function	Typical Value	Tolerance	Unit
C1	V_{BB} buffer capacitor (Note 15)	22	−20 +80%	μF
C2	V_{BB} decoupling capacitor	100	−20 +80%	nF
R1, R2	Pullup resistor	1...5	±10%	kΩ
D1	Optional reverse protection diode	E.G. SS16		

15. Low ESR < 4 Ω, mounted as close as possible to the NCV70501. The total decoupling capacitance value has to be chosen properly to reduce the supply voltage ripple and to avoid EM emission.

FUNCTIONAL DESCRIPTION

H−Bridge Drivers with PWM Control

Two H−bridges are integrated to drive a bipolar stepper motor. Each H−bridge consists of two low−side N−type MOSFET switches and two high−side P−type MOSFET switches. One PWM current control loop with on−chip current sensing is implemented for each H−bridge. Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted to maintain current−sense accuracy. A comparator compares continuously the actual winding current with the requested current and feeds back the information to generate a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock. For each output bridge the PWM duty cycle is measured and stored in two appropriate status registers of the motor controller.

The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency. In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. Two bits in SPI control register 3 allow adjustment of the voltage slopes.

A protection against shorts on motor lines is implemented. When excessive voltage is sensed across a MOSFET for a time longer than the required transition time, then the MOSFET is switched−off.

Motor Enable−Disable

The H−bridges and PWM control can be disabled (high−impedance state) by means of a bit <MOTEN> in the SPI control registers. <MOTEN>=0 will only disable the drivers and will not impact the functions of NXT, DIR, RHB, SPI bus, etc. The H−bridges will resume normal PWM operation by writing <MOTEN>=1 in the SPI register. PWM current control is then enabled again and will regulate current in both coils corresponding with the position given by the current translator.

Automatic Forward and Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. For transition to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

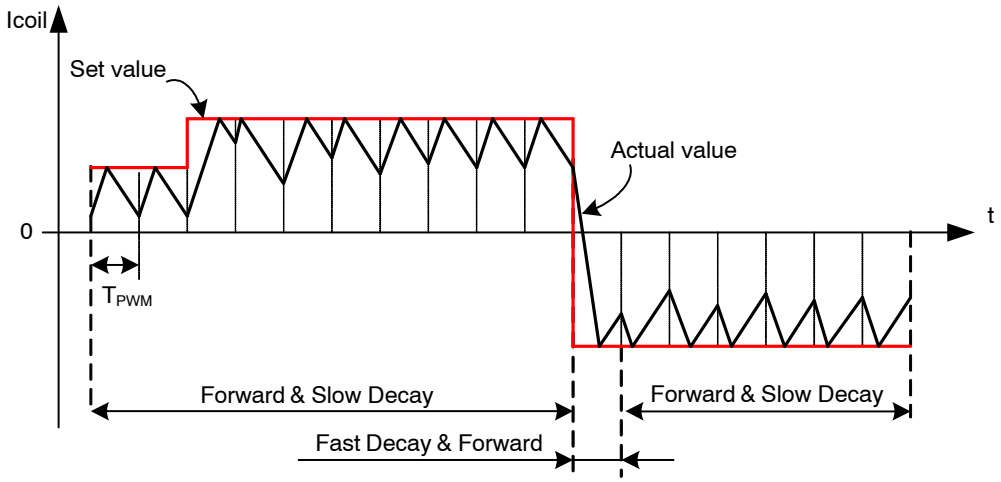


Figure 5. Forward and Slow/Fast Decay PWM

PWM Duty Cycle Measurement

For both motor windings the actual PWM duty cycle is measured and stored in two status registers. The duty cycle values are a representation of the applied average voltage to the motor windings to achieve and maintain the actual set point current. Figure 6 gives an example of the duty cycle representation.

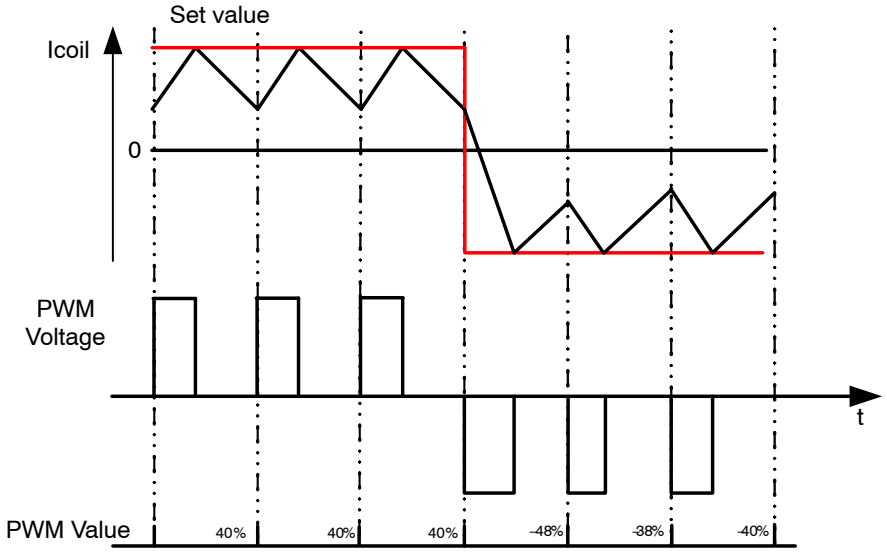


Figure 6. PWM Duty Cycle Measurement

Automatic Duty Cycle Adaptation

If during regulation the set point current is not reached before 75% of T_{pwm}, the duty cycle of the PWM is adapted automatically to > 50% (top regulation) to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The state of the duty cycle adaptation mode is represented in the T/B bits of the appropriate status registers for both motor windings X and Y. Figure 7 gives a representation of the duty cycle adaptation.

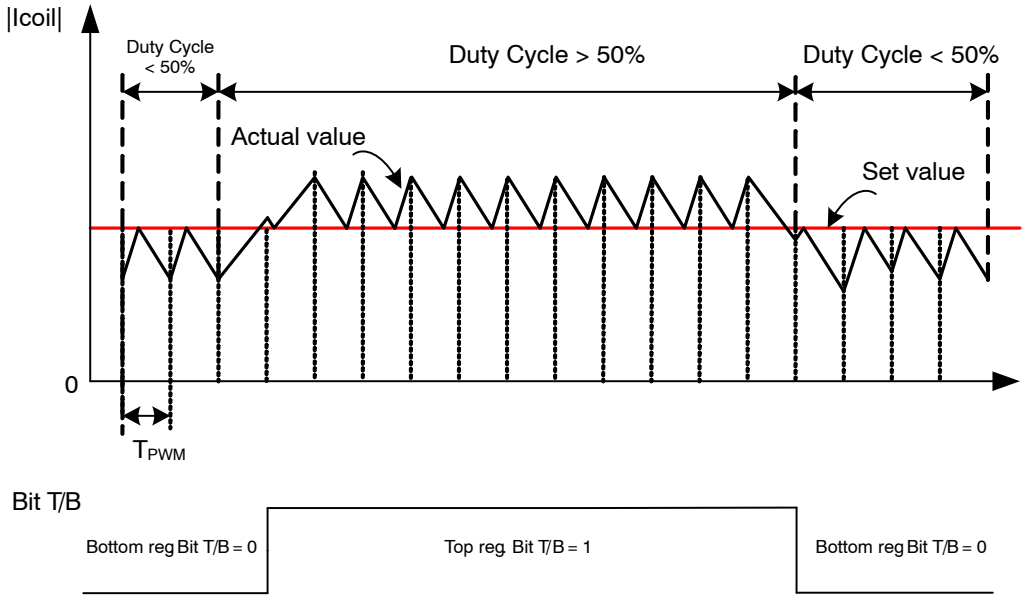


Figure 7. Automatic Duty Cycle Adaptation

Step Translator

Step Mode

The step translator provides the control of the motor by means of SPI register step mode: SM[2:0], SPI bits DIRP, RHBP and input pins DIR (direction of rotation), RHB (run/hold of motor) and NXT (next pulse). It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of six possible stepping modes can be selected through SPI−bits SM[2:0]. After power−on or hard reset, the coil−current translator is set to the default to 1/16 micro−stepping at position **‘8*’**. When remaining in the default step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 10 lists the output current versus the translator position.

When the micro−step resolution is reduced, then the corresponding least−significant bits of the translator position are set to “0”. This means that the position in the current table moves to the right. If there is no adjacent allowed step on the same line, then the position pointer will also move upwards or downwards (depending on the DIR state) in the table to arrive at the corresponding position after one following NXT pulse when DIR is ‘1’ or after two following next pulses when DIR = ‘0’.

When the micro−step resolution is increased, then the corresponding least−significant bits of the translator position are added as “0”: the micro−step position moves to the left on the same row.

Table 10. CIRCULAR TRANSLATOR TABLE

	Step Mode (SM[2:0])				% of I_{max}			Step Mode (SM[2:0])				% of I_{max}	
	000	001	010	011				000	001	010	011		
MSP[5:0]	1/16	1/8	1/4	1/2	Coil y	Coil x	MSP[5:0]	1/16	1/8	1/4	1/2	Coil y	Coil x
000 000	0	0	0	0	0,0	100,0	**100 000**	32	16	8	4	0,0	−100,0
000 001	1	–	–	–	9,8	99,5	**100 001**	33	–	–	–	−9,8	−99,5
000 010	2	1	–	–	19,5	98,1	**100 010**	34	17	–	–	−19,5	−98,1
000 011	3	–	–	–	29,0	95,7	**100 011**	35	–	–	–	−29,0	−95,7
000 100	4	2	1	–	38,3	92,4	**100 100**	36	18	9	–	−38,3	−92,4
000 101	5	–	–	–	47,1	88,2	**100 101**	37	–	–	–	−47,1	−88,2
000 110	6	3	–	–	55,6	83,1	**100 110**	38	19	–	–	−55,6	−83,1
000 111	7	–	–	–	63,4	77,3	**100 111**	39	–	–	–	−63,4	−77,3
001 000	8(*)	4	2	1	70,7	70,7	**101 000**	40	20	10	5	−70,7	−70,7
001 001	9	–	–	–	77,3	63,4	**101 001**	41	–	–	–	−77,3	−63,4
001 010	10	5	–	–	83,1	55,6	**101 010**	42	21	–	–	−83,1	−55,6
001 011	11	–	–	–	88,2	47,1	**101 011**	43	–	–	–	−88,2	−47,1
001 100	12	6	3	–	92,4	38,3	**101 100**	44	22	11	–	−92,4	−38,3
001 101	13	–	–	–	95,7	29,0	**101 101**	45	–	–	–	−95,7	−29,0
001 110	14	7	–	–	98,1	19,5	**101 110**	46	23	–	–	−98,1	−19,5
001 111	15	–	–	–	99,5	9,8	**101 111**	47	–	–	–	−99,5	−9,8
010 000	16	8	4	2	100,0	0,0	**110 000**	48	24	12	6	−100,0	0,0
010 001	17	–	–	–	99,5	−9,8	**110 001**	49	–	–	–	−99,5	9,8
010 010	18	9	–	–	98,1	−19,5	**110 010**	50	25	–	–	−98,1	19,5
010 011	19	–	–	–	95,7	−29,0	**110 011**	51	–	–	–	−95,7	29,0
010 100	20	10	5	–	92,4	−38,3	**110 100**	52	26	13	–	−92,4	38,3
010 101	21	–	–	–	88,2	−47,1	**110 101**	53	–	–	–	−88,2	47,1
010 110	22	11	–	–	83,1	−55,6	**110 110**	54	27	–	–	−83,1	55,6
010 111	23	–	–	–	77,3	−63,4	**110 111**	55	–	–	–	−77,3	63,4
011 000	24	12	6	3	70,7	−70,7	**111 000**	56	28	14	7	−70,7	70,7
011 001	25	–	–	–	63,4	−77,3	**111 001**	57	–	–	–	−63,4	77,3
011 010	26	13	–	–	55,6	−83,1	**111 010**	58	29	–	–	−55,6	83,1
011 011	27	–	–	–	47,1	−88,2	**111 011**	59	–	–	–	−47,1	88,2
011 100	28	14	7	–	38,3	−92,4	**111 100**	60	30	15	–	−38,3	92,4
011 101	29	–	–	–	29,0	−95,7	**111 101**	61	–	–	–	−29,0	95,7
011 110	30	15	–	–	19,5	−98,1	**111 110**	62	31	–	–	−19,5	98,1
011 111	31	–	–	–	9,8	−99,5	**111 111**	63	–	–	–	−9,8	99,5

*Default position after reset of the translator position.

Besides the micro−step modes listed above, also two full step modes are implemented. Full step mode 1 activates always only one coil at a time, whereas mode 2 always keeps 2 coils active. The table below lists the output current versus the translator positions for these cases and Figure 8 shows the projection on a square.

Changing between micro−step mode and full step modes follows a similar scheme as changes between micro−step modes. Changing from one full step mode to another full step mode will always result in a “45deg step−back or forward” depending on the DIR bit. For example: in the table below, when changing full step mode (positioner is on a particular row and full step column), then the new full step location will be one row above or below in the adjacent “full step column”. The step−back and forward is executed after the NXT pulse.

Example change FS1−>FS2−>FS1 (CW Direction): MSP=”100 000”(FS1) => new MSP=”011 000”(FS2) => new MSP=“010 000”(FS1)

Table 11. SQUARE TRANSLATOR TABLE FOR FULL STEP

	Step Mode (SM[2:0])		% of Imax	
	101	111		
MSP[5:0]	Full Step1	Full Step2	Coil x	Coil y
000 000	0	–	100	0
001 000	–	0	71	71
010 000	1	–	0	100
011 000	–	1	−71	71
100 000	2	–	−100	0
101 000	–	2	−71	−71
110 000	3	–	0	−100
111 000	–	3	71	−71

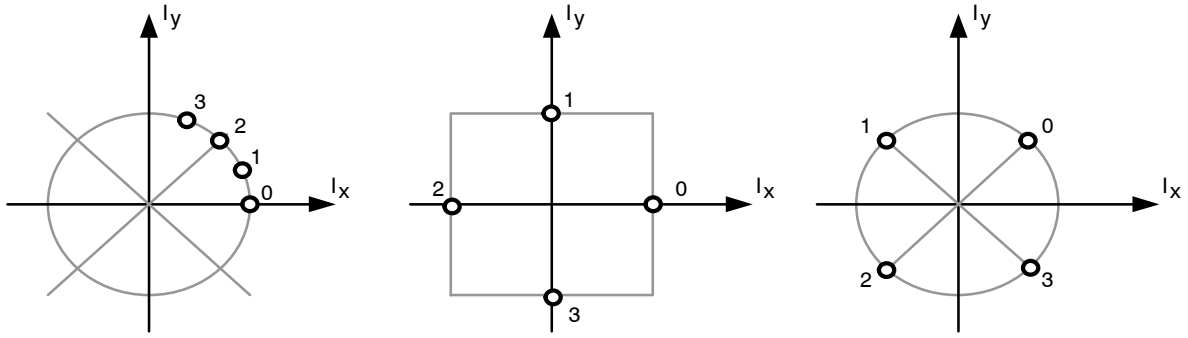


Figure 8. Translator Table: Circular and Square

Translator Position

The translator position can be read in the SPI register <MSP[5:0]>. This is a 6−bit number equivalent to the 1/16th micro−step from Table 10: Circular Translator Table. The translator position is updated immediately following a next micro−step trigger (see Figure 9).

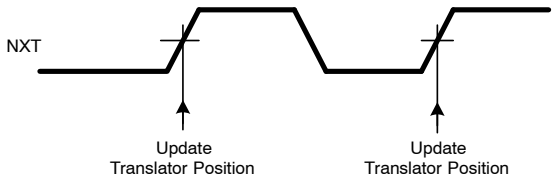


Figure 9. Translator Position Timing Diagram

Direction

The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP> (SPI register). The polarity bit <DIRP> allows changing the direction of rotation by means of only SPI commands instead of the dedicated input pin.

Direction = DIR−pin EXOR <DIRP>

Positive direction of rotation means counter−clockwise rotation of electrical vector Ix + Iy. Also when the motor is disabled (<MOTEN>=0), both the DIR pin and <DIRP> will have an effect on the positioner. The logic state of the DIR pin is visible as a flag in SPI status register.

Next Micro−Step Trigger

Positive edges on the NXT input − or activation of the “NXT pushbutton” <NXTP> in the SPI input register − will move the motor current one step up/down in the translator table. The <NXTP> bit in SPI is used to move positioner one (micro−)step by means of only SPI commands. If the bit is set to “1”, it is reset automatically to “0” after having advanced the positioner with one micro−step.

Trigger “Next micro−step” = (positive edge on NXT−pin) OR (<NXTP>=1)

- Also when the motor is disabled (<MOTEN>=0), NXT/DIR/RHB functions will move the positioner according to the logic.
- In order to be sure that both the NXT pin and the <NXTP> SPI command are individually attended, the following non overlapping zone has to be respected. In this case it is guaranteed that both triggers will have effect (2 steps are taken).

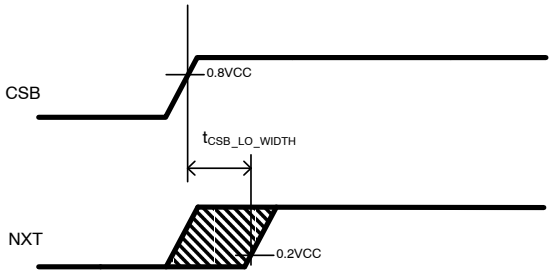


Figure 10. NXT Input Nonoverlapping Zone with the <NXTP> SPI Command

For control by means of I/O’s, the NXT− and DIR pin operation should be in a non−overlapped way. See also the timing diagram below (refer to the AC table for the timing values). On the other hand, both SPI bits <DIRP> and <NXTP> can change state at the same time in the same SPI command: the next micro−step will be applied in the new direction.

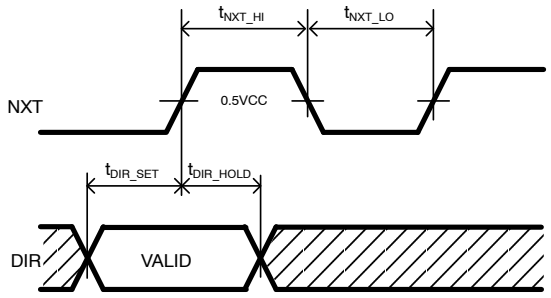


Figure 11. NXT−Input Timing Diagram

IRUN, IHOLD and “Run / Not Hold” Mode

The RHB input pin and it’s “polarity bit” <RHBP> (SPI register) allow to switch the driver between “Run Mode” and “Hold Mode”.

“Run Mode” = NOT(“Hold Mode”) = RHB pin EXOR <RHBP>

- In “Run mode”, the current translator table is stepped through based on the “NXT & DIR” commands. The amplitude of the motor current (=Imax) is set by SPI control register ”IRUN[3:0]”.
- In “Hold mode”, NXT & DIR will have no effect and the position in the current translator table is maintained. The motor current amplitude is set by SPI control register ”IHOLD[3:0]”.

The run and hold current settings correspond to the following current levels:

Table 12. IRUN AND IHOLD REFERENCE VALUES (4−BIT)

Register Value	Peak Motor Current IRUN (mA)	Peak Motor Current IHOLD (mA)
0	15	0*
1	27	15
2	48	27
3	87	48
4	100	87
5	115	100
6	132	115
7	152	132
8	174	152
9	200	174
A	230	200
B	300	230

*During hold with a hold current of 0 mA the stall and motion detection and the open coil detection are disabled. The PWM duty cycle registers will present 0% duty cycle.

Whenever IRUN[3:0] or IHOLD[3:0] is changed, the new coil currents will be updated immediately at the next PWM period.

In case the motor is disabled (<MOTEN>=0), the logic is functional and both RHB pin and <RHBP> bit will have effect on NXT/DIR operation (not on the H−bridges). When the chip is in sleep mode, the logic is not functional and as a result, the RHB pin will have no effect.

The logic state of the RHB pin is visible as a flag in SPI status register.

Note: The hard−reset function is embedded in the "Hold mode" by means of a special sequence on the DIR pin, see also (Hard Reset).

Stall and Motion Detection

Motion detection is based on the Back Electromotive Force (BEMF or back emf) generated into the stepper driver H−bridge. When the motor is blocked, e.g. when it hits the end−position, the velocity and as a result also the generated back emf, is disturbed. The NCV70501 measures the differential back emf during the current zero crossing phase and makes it available in the SPI status register 3. The measurement samples are taken every PWM period and will be converted into a 5−bits coded word, with the following formula:

$$BEMF\_code(dec) = V\_MOT\_XorY\_diff\ (V) * \left(\frac{5}{8}\right) * \frac{2^5}{2.41}$$

For further reference, please see SPI map and Table 7 − BEMF. At the end of the current zero crossing the internal circuitry compares the last sampled value with a threshold <StThr[3:0]> for the stall detection.

For slow speed or when a motion ends at a full step position, the end of the zero crossing is taking too long or is non−existing. Therefore, the comparison of Bemf with the threshold will be done − in the absence of a NXT trigger − the latest at "stall time−out". This time−out is set in SPI by means of <StTo[7:0]> and is expressed in counts of $4/f_{pwm}$ (See AC Table), roughly in steps of 0.2 ms. If <StTo[7:0]> = 0 then this time−out is not active.

If <StThr[3:0]> = 0 then stall detection is disabled. If the Bemf signal is measured to be below the StThr level for 2 succeeding coil current zero−crossings, then the stall bit in SPI is set, the current translator table goes 135degrees in opposite direction and the ERRB pin is pulled low, Irun is maintained. The stall bit in SPI register is cleared upon read of the microcontroller, also the ERRB pin is inactive again. After the stall bit has been cleared, the chip will react on "Next Micro−step Triggers" only when the direction changed state at least once.

An additional feature of the NCV70501 is the detection of uncontrolled motion during Hold. If the stall detection is enabled and the hold position is at full steps (full step mode1, 0°, 90°, 180°, 270°) with only excitation of one coil, the NCV70501 is checking upon back emf voltages higher then the <StThr[3:0] > threshold. If this higher voltage is detected it indicates there is a motor movement. The stall bit in the SPI register is set and the ERRB pin will be activated. The motion detection during hold does not work for IHold is 0A.

Table 13. STALL THRESHOLD SETTINGS (4−BIT)

StThr[3:0] Index	StThr Level (V)
0	Disable
1	0.125
2	0.250
3	0.375
4	0.50
5	0.625
6	0.75
7	1.0
8	1.25
9	1.5
A	1.75
B	2.0
C	2.25
D	2.50
E	2.75
F	3.00

Warning, Error Detection and Diagnostics Feedback

Thermal Warning and Shutdown

When junction temperature is above T_{TW}, the thermal warning bit <TW> is set (SPI Register) and the ERRB pin is pulled low*. If junction temperature increases above thermal shutdown level, then also the <TSD> flag is set, the ERRB pin is pulled low, the motor is disabled (<MOTEN> = 0) and the hardware reset is disabled. If $T_J < T_{tw}$ level and after reading of <TSD> the status of <TSD> is cleared and the ERRB pin is released.

Only if the <TSD>=<TW>=0 the motor can be enabled again by writing <MOTEN>=1 in the control register 1.

During the over temperature condition the hardware reset will not work until $T_J < T_{tw}$ and the <TSD> readout is done.

In this way it is guaranteed that after a <TSD>=1 event, the die−temperature decreases back to the level of T_{TW}.

*__Remark__: During the <TW> situation the motor is not disabled while the ERRB is pulled low. To be informed about other error situations it is recommended to poll the status registers on a regular base (time base driven by application software in the millisecond domain).

Over−Current Detection

The over−current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over−current detection threshold, then the over−current flag <SHORT> is set and the drivers are

switched off to protect the integrated circuit. Each driver stage has an individual detection bit for the N side and the P side.

During a short situation the Motor Enable bit becomes low. The positioner, the NXT, RHB and DIR stay operational.

The flag <SHORT> (result of OR−ing the latched flags : <SHRTXPT> OR <SHRTXPB> OR <SHRTXNT> OR <SHRTYXNB> OR <SHRTYPT> OR <SHRTYPB> OR <SHRTYNT> OR <SHRTYNB>) is reset when the microcontroller reads&resets the short circuit status flags in status registers 6 and 7.

To enable the motor after a cleared short flag, <MOTEN> =1 has to be written. Depending on the <DIAGEN> bit in SPI control register 3 the motor driver performs an automatic diagnostics procedure after enabling the motor (refer to the Automatic Diagnostics section).

Notes:

1. Successive reading of the <SHRTij> flags and enabling the motor in case of a short circuit condition, may lead to damage of the drivers.
2. Example: SHRTXPT means: Short at X coil, Positive output pin, Top transistor.

Open Coil Detection

There are two open coil detection methods used:

After Power up: During the power up reset state, the electronics automatically performs diagnostics for open coils and short circuit conditions. If an error situation is detected the <OPENX> or <OPENY> with the <OPEN> and <SHORT> bits are set in the SPI status registers. These bits remain active during the entered sleep mode after power−up (refer to the Sleep Mode Section).

During operation: Open coil detection is based on the observation of 100 percent duty cycle of the PWM regulator. If in a coil 100 percent duty cycle is detected for longer than T_{OCdet} then the related driver transistors are disabled (high−impedance) and the appropriate bit (<OPENX> or <OPENY>) together with <OPEN> in the SPI status register are set. During the stated situation the positioner and the not open coil stay functioning, as well as the Motor Enable bit. After reading the status of the open coil bit, the output stage concerned will become active again.

Remark: In order to detect an open coil, it needs to be driven without interruption during minimum T_{OCdet}. This is typically the case during hold condition or very slow motions.

SPI Framing Error

The SPI transmission is continuously monitored for correct amounts of incoming data bits. If within one frame of data the number of SPI CLK high transitions is not equal to a multiple of 16 (16,32,48,...), then the SPI error bit in the status register is set and the ERRB pin goes low to indicate this error to the micro controller. During this fault condition the incoming data is not loaded into the internal registers and the transmit shift register is not loaded with the requested data.

The status of the SPI framing error is reset by an errorless received frame requesting for the motor controller status register 0. This request will reset the SPI error bit and releases the ERRB pin (high).

Error Output

This is an open drain output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = (<SPI> OR <SHORT> OR <OPENX> OR <OPENY> OR <TSD> OR <TW> OR <STALL> OR (*)reset state)

AND not(**)sleep mode

* Reset State: After a power−on or a hard−reset, the ERRB is pulled low during Threrr (Table 8: AC Parameters).

** Sleep Mode: In sleep mode the ERRB is always inactive (high).

Automatic Diagnostics

Via the diagnostics enable bit <DIAGEN> in SPI control register 3 an automatic diagnostics mode can be enabled. The diagnostic routine is the same as the routine in powerup situation. When automatic diagnostics is enabled, every time when the user changes the Motor Enable state from ‘0’ to ‘1’, the diagnostics are performed. The dead time for this diagnostics routine is 1 ms*.

*For a controlled start of the diagnostics the user has to place the motor driver in high impedance state by setting the MOTEN bit to ‘0’. After changing this bit, there is need for an additional delay time. This is needed for recirculation of the motor current. An average time of approximately 2ms is needed. This time has to be taken into account by the user.

Sleep Mode

The motor driver can be put in a low−power consumption mode (sleep mode). The sleep mode is entered automatically after a power−on or hard reset and can also be activated by means of SPI bit <SLP>. In sleep−mode, all analog circuits are suspended in low−power and all digital clocks are stopped: SPI communication is impossible. The motor driver is disabled (even if <MOTEN>=1), the content of all logic registers is maintained (including <MOTEN>, <TSD> and <TW>), all logic output pins are disabled (ERRB has no function) and none of the input pins are functional with the exception of pin CSB. Only this pin can wake−up the chip to normal mode (i.e. clear bit <SLP>) by means of a “high−to−low voltage” transition. After wake−up, some time T_{wu}, (see AC Table) is needed to restore analog and digital clocks and to bring SPI communication within specification.

Notes:

- The hard−reset function is disabled in sleep mode.

- The thermal shutdown function will be “frozen” during sleep mode and re−activated at wake−up. This is important in case bit <TSD>=1 was cleared already by the micro and <TW> was not “0” yet.
- The CSB low pulse width has to be within T_{CSB_with}, (see AC Table) to guarantee a correct wake−up

Power−on Reset, Hard−Reset Function

After a power−on a flag <HR> in the SPI status register is set and the ERRB is pulled low. The ERRB stays low during this reset state. The maximum power−on reset time is given by Threrr (Table 6: AC Parameters). After the reset state the device enters sleep mode and the ERRB pin goes high to indicate the motor controller is ready for operation.

By means of a specific pattern on the DIR pin during the “Hold Mode”, the complete digital can be reset without a power−cycle. This so called hard−reset function is activated when during “Hold Mode”, the input pin DIR changes logic state “0−>1−>0−>1” within T_{hr_trig} (Table 6: AC Parameters).

The operation of all analog circuits is suspended during the reset state of the digital. Similar as for a normal power−on, the flag <HR> is set in the SPI register after a hard−reset and the ERRB pin is pulled low during Threrr (Table 8: AC Parameters).

To enable the motor controller to perform a proper self diagnosis, it is recommended that the motor is in “Hold Mode” before the hard reset is generated. The minimum time (Thr_set) between the beginning of “Hold Mode” and the first rising edge of the DIR pin is given in Table 6: AC Parameters.

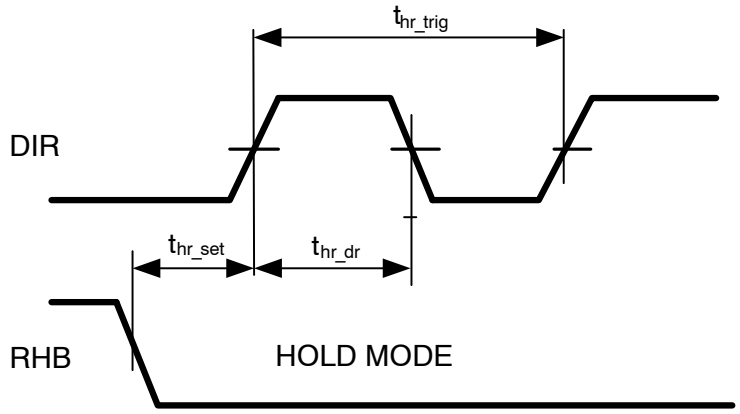


Figure 12. Hard Reset Timing Diagram

SPI INTERFACE

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV70501 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The implemented SPI allows connection to multiple slaves by means of both time−multiplexing (CSB per slave) and daisy−chain (CSB per group of slaves). Multi−axis connections schemes are discussed in a separate chapter below.

SPI Transfer Format and Pin Signals

All SPI commands (to DI pin of NCV70501) from the micro controller consist of one “address byte” and one “data byte”. The address byte contains up to two addresses of each 4 bit long. These addresses are pointing to a command or requested action in a SPI slave. Three command−types can be distinguished: “Write to a control register”, “Read from a control register” and “Read from a status register”.

- Writing to a control register is accomplished only if the address of the target register appears in the first half of the address byte. The contents of the data−byte will be copied in the control register. The contents of the addressed control register will be sent back by the NCV70501 in the next SPI access.
- Reading from a control register is accomplished by putting its address in the second half of the address byte. The data byte has no function for this command.
- Reading from a status register is accomplished by putting its address either in the first or in the second half of the address byte. The data byte has no function for this command.

The response (from DO pin of NCV70501) on these commands is always 2 bytes long. The possible combinations of DI/DO and their use are summarized in the following Table 14. Figure 13 gives examples of the data streaming:

Table 14. SPI COMMAND ADDRESS, DATA AND RESPONSE STRUCTURE

DI ADDR[7:4]	DI ADDR[3:0]	DI DATA[7:0]	DO BYTE1	DO BYTE2	Comment on Use
ACR1	ACR2	DICR1	DOCR1	DOCR2	Control and Status of CR
ACR1	ASR1	DICR1	DOCR1	DOSR1	Control and Status of SR
ACR1	Nop	DICR1	DOCR1	00h	Control and no Status
ASR1	ACR1	XXh	DOSR1	DOCR1	Status of SR and CR
ASR1	ASR2	XXh	DOSR1	DOSR2	Status of SR and SR
ASR1	Nop	XXh	DOSR1	00h	Status of SR
Nop	ACR1	XXh	00h	DOCR1	Status of CR
Nop	ASR1	XXh	00h	DOSR1	Status of SR
Nop	Nop	XXh	00h	00h	Dummy/Placeholder

With:

- ACRx = Address of control register x
- ASRx = Address of status register x
- DICRx = Data input of Control Register x
- DOxy = Data output of corresponding register contents transmitted in the next SPI access
- Nop = Register address outside range : 0h, Ch, Dh, Eh or Fh
- XXh = any byte

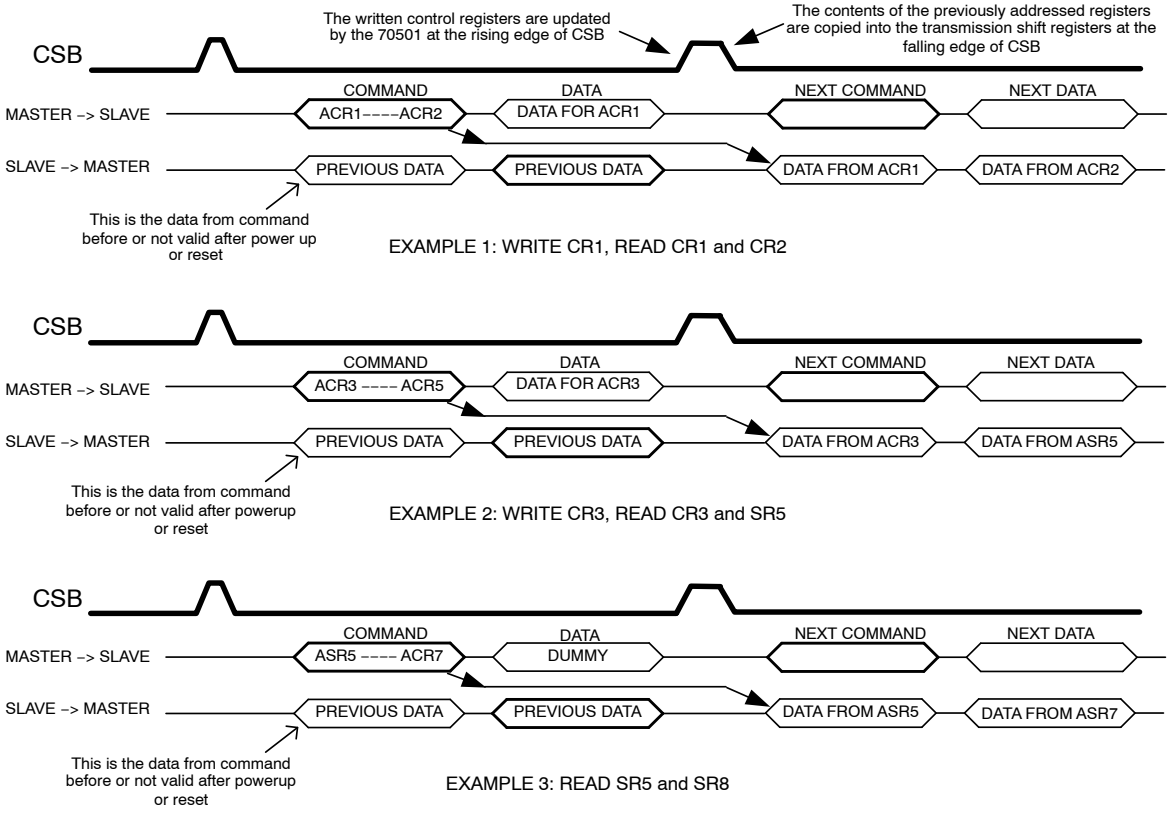


Figure 13. Command and Data Streaming of SPI

Table 15. SPI CONTROL REGISTERS

4−bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default After Reset
1h (CR1)	DIRP	RHBP	NXTP	MOTEN	StTrh[3]	StTrh[2]	StTrh[1]	StTrh[0]	0000 0000
2h (CR2)	Ihold[3]	Ihold[2]	Ihold[1]	Ihold[0]	Irun[3]	Irun[2]	Irun[1]	Irun[0]	0000 0000
3h (CR3)	Reserved	DIAGEN	EMC[1]	EMC[0]	SLP	SM[2]	SM[1]	SM[0]	0010 0000
4h (CR4)	StTo[7]	StTo[6]	StTo[5]	StTo[4]	StTo[3]	StTo[2]	StTo[1]	StTo[0]	0001 0000

All SPI CONTROL registers have Read/Write access. The NCV70501 responds on every incoming byte by shifting out the data stored on the last address sent via the bus. After power on reset (POR) the initial address is unknown, so in that case the first data shifted out is undefined. Note: all “reserved” bits cannot be written to one and will always be read out as zeroes.

BITS DEFINITION

Symbol	MAP position	Description
DIRP	Bit 7 – ADDR_0x01 (CR1)	Direction control polarity (inverts the logic polarity of the related DIR pin)
RHBP	Bit 6 – ADDR_0x01 (CR1)	Polarity of RHB pin; RHBP = 1 inverts RHB pin (Hold = NOT(RHB XOR RHBP))
NXTP	Bit 5 – ADDR_0x01 (CR1)	Push button pin, generating next step in position table
MOTEN	Bit 4 – ADDR_0x01 (CR1)	Enables the X Y H-bridges (motor activated, either in RUN or in HOLD).
StThr[3:0]	Bits [3:0] – ADDR_0x01 (CR1)	Threshold level for internal stall detection algorithm; disabled when “0”.
Ihold[3:0]	Bits [7:4] – ADDR_0x02 (CR2)	Current amplitude in HOLD mode.
Irun[3:0]	Bits [3:0] – ADDR_0x02 (CR2)	Current amplitude in RUN mode.
DiagEN	Bit 6 – ADDR_0x03 (CR3)	Enables automatic diagnostics at the rising edge of MOTEN bit.
EMC[2:0]	Bits [5:4] – ADDR_0x03(CR3)	Voltage slope defining bits for motor driver switching. Three combinations are available up to “10”
SLP	Bit 3 – ADDR_0x03 (CR3)	Places the device in sleep mode with low current consumption (when written as “1”). Note that this bit cannot read back for verification as by doing so the device will awake.
SM[2:0]	Bits [2:0] – ADDR_0x03(CR3)	Step mode selection (see related tables).
StTo[7:0]	Bits [7:0] – ADDR_0x04(CR4)	Max programmed difference between two successive full step next pulse periods (timeout): after this time the BEMF sample is taken to verify stall.

Table 16. SPI STATUS REGISTER (SR) ALL SPI STATUS REGISTERS HAVE READ ONLY ACCESS, WITH THE EVEN PARITY ON BIT7

4−bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comment	Default After Reset
5h (SR1)	PAR	SPI,L	SHORT,R	OPEN,R	TSD,L	TW,R	STALL,L	HR,L	Errors	x0xx xx01
6h (SR2)	PAR	RHBpin,R	MSP5,R	MSP4,R	MSP3,R	MSP2,R	MSP1,R	MSP0,R	Micro−step position	xx00 1000
7h (SR3)	PAR	DIRpin, R	Bemfs, R	Bemf4, R	Bemf3, R	Bemf2, R	Bemf1, R	Bemf0, R	Input pins and Bemf	xx00 0000
8h (SR4)	PAR	T/BX,R	SignX,R	PWMX4,R	PWMX3,R	PWMX2,R	PWMX1,R	PWMX0,R	PWMX	0000 0000
9h (SR5)	PAR	T/BY,R	SignY,R	PWMY4,R	PWMY3,R	PWMY2,R	PWMY1,R	PWMY0,R	PWMY	0000 0000
Ah (SR6)	PAR	OPENX,L	Reserved	Reserved	SHRTXPB,L	SHRTXNB,L	SHRTXPT,L	SHRTXNT,L	ShortsX	xx00 xxxx
Bh (SR7)	PAR	OPENY,L	Reserved	Reserved	SHRTYPB,L	SHRTYNB,L	SHRTYPT,L	SHRTYNT,L	ShortsY	xx00 xxxx

Flags have “,L” for latched information or “,R” for real time information. All latched flags are “cleared upon read”.

All SPI STATUS registers have Read access. Flags have “,L” for latched information or “,R” for real time information. All latched flags are “cleared upon read”. Note: all “reserved” bits will always be read out as zeroes. All status registers data is protected by even parity.

BITS DEFINITION

Symbol	Bit position	Reg	Description
Par	Bit 7 – ADDR_0x05	SR1	Parity bit for SR1.
SPI	Bit 6 – ADDR_0x05	SR1	SPI error: no multiple of 16 rising clock edges between falling and rising edge of CSB line.
SHORT	Bit 5 – ADDR_0x05	SR1	An over current detected (common : reads if one of the SHORTij individual bits are set)
OPEN	Bit 4 – ADDR_0x05	SR1	Open Coil X or Y detected (common : reads if one of the two specific X / Y open coil bits is set)
TSD	Bit 3 – ADDR_0x05	SR1	Thermal shutdown flag. This situation should always be avoided in the final application by proper thermal design.
TW	Bit 2 – ADDR_0x05	SR1	Thermal warning flag. The controller unit should take action before the TSD is reached (shutdown).
STALL	Bit 1 – ADDR_0x05	SR1	Stall detected by the internal algorithm (BEMF < StThr). The feature can be disabled (see prev. table)
HR	Bit 0 – ADDR_0x05	SR1	Reset flag: “1” indicates that any reset has occurred (all registers content will go to POR default).
Par	Bit 7 – ADDR_0x06	SR2	Parity bit for SR2.
RHBpin	Bit 6 – ADDR_0x06	SR2	Read out of RHB pin logic status.
MSP[5:0]	Bits[5:0] – ADDR_0x06	SR2	Current translator micro-step position (see related table for details).
Par	Bit 7 – ADDR_0x07	SR3	Parity bit for SR3.
DIRpin	Bit 6 – ADDR_0x07	SR3	Read out of DIR pin logic status.
Bemfs	Bit 5 – ADDR_0x07	SR3	Last BEMF measured voltage has expected polarity (Yes = 0, No = 1 means opposite sign).
Bemf[4:0]	Bits [4:0] – ADDR_0x07	SR3	BEMF measured value code. See formula in STALL DETECTION section for details.
Par	Bit 7 – ADDR_0x08	SR4	Parity bit for SR4.
T/BX	Bit 6 – ADDR_0x08	SR4	PWM Regulation mode on X coil (regulation on Top = 1 or Bottom = 0)
SignX	Bit 5 – ADDR_0x08	SR4	PWM sign for X coil regulation (“0” = positive, “1” = negative)
PWMX[4:0]	Bits [4:0] – ADDR_0x08	SR4	PWM duty cycle value for coil X (proportional: 100% corresponds to 31dec)
Par	Bit 7 – ADDR_0x09	SR5	Parity bit for SR5.
T/BY	Bit 6 – ADDR_0x09	SR5	PWM Regulation mode on Y coil (regulation on Top = 1 or Bottom = 0)
SignY	Bit 5 – ADDR_0x09	SR5	PWM sign for Y coil regulation (“0” = positive, “1” = negative)
PWMY[4:0]	Bits [4:0] – ADDR_0x09	SR5	PWM duty cycle value related to coil Y (proportional: 100% corresponds to 31dec)
Par	Bit 7 – ADDR_0x0A	SR6	Parity bit for SR6.
OPENX	Bit 6 – ADDR_0x0A	SR6	Open Coil X detected.
Reserved	Bits [5:4] – ADDR_0x0A	SR6	Reserved, will be read as zeroes.
SHRTXPB	Bit 3 – ADDR_0x0A	SR6	Short circuit detected at XP pin towards ground (bottom).
SHRTXNB	Bit 2 – ADDR_0x0A	SR6	Short circuit detected at XN pin towards ground (bottom).
SHRTXPT	Bit 1 – ADDR_0x0A	SR6	Short circuit detected at XP pin towards supply (top).
SHRTXNT	Bit 0 – ADDR_0x0A	SR6	Short circuit detected at XN pin towards supply (top).
Par	Bit 7 – ADDR_0x0B	SR7	Parity bit for SR7.
OPENY	Bit 6 – ADDR_0x0B	SR7	Open Coil Y detected.
SHRTYPB	Bit 3 – ADDR_0x0B	SR7	Short circuit detected at YP pin towards ground (bottom).
SHRTYNB	Bit 2 – ADDR_0x0B	SR7	Short circuit detected at YN pin towards ground (bottom).
SHRTYPT	Bit 1 – ADDR_0x0B	SR7	Short circuit detected at YP pin towards supply (top).
SHRTYNT	Bit 0 – ADDR_0x0B	SR7	Short circuit detected at YN pin towards supply (top).

APPLICATION EXAMPLES FOR MULTI−AXIS CONTROL

The wiring diagrams below show possible connections of multiple slaves to one microcontroller. In these examples, all movements of the motors are synchronized by means of a common NXT wire. The direction and Run/Hold activation is controlled by means of an SPI bus.

Further I/O reduction is accomplished in case the ERRB is not connected. This would mean that the microcontroller operates while polling the error flags of the slaves. Ultimately, one can operate multiple slaves by means of only 4 SPI connections: even the NXT pin can be avoided if the microcontroller operates the motors by means of the “NXTP” bit.

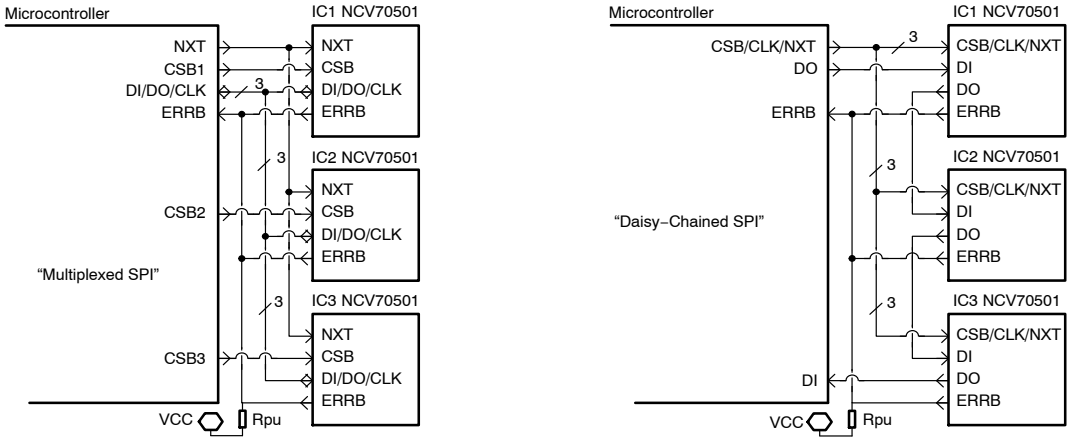


Figure 14. Examples of Wiring Diagrams for Multi−Axis Control*

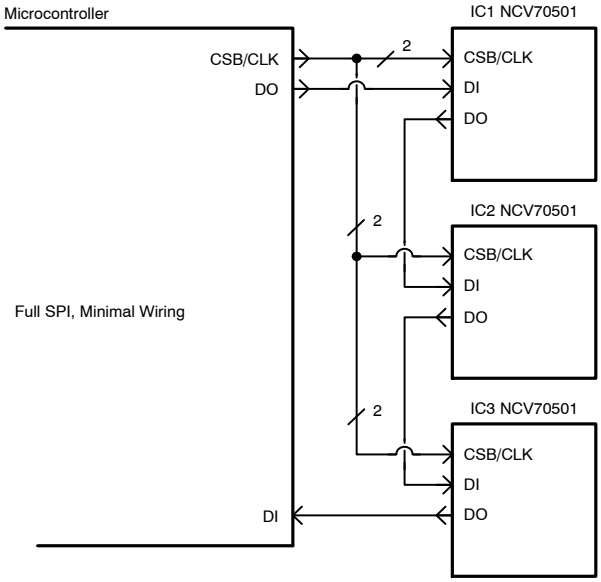


Figure 15. Minimal Wiring Diagram for Multi−Axis Control*

*This drawing does not present the Hard Reset interconnection. For the functionality of the Hard Reset function the RHB and DIR pins have to be connected to the micro controller.

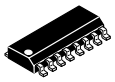
ELECTRO MAGNETIC COMPATIBILITY

The NCV70501 has been developed using state−of−the−art design techniques for EMC. The overall system performance depends on multiple aspects of the system (IC design and lay−out , PCB design and layout ...) of which some are not solely under control of the IC manufacturer. Therefore, meeting system EMC requirements can only happen in collaboration with all involved parties.

Special care has to be taken into account with long wiring to motors and inductors. A modern methodology to regulate the current in inductors and motor windings is based on controlling the motor voltage by PWM. This low frequency switching of the battery voltage is present at the wiring towards the motor or windings. To reduce possible radiated transmission, it is advised to use twisted pair cable and/or shielded cable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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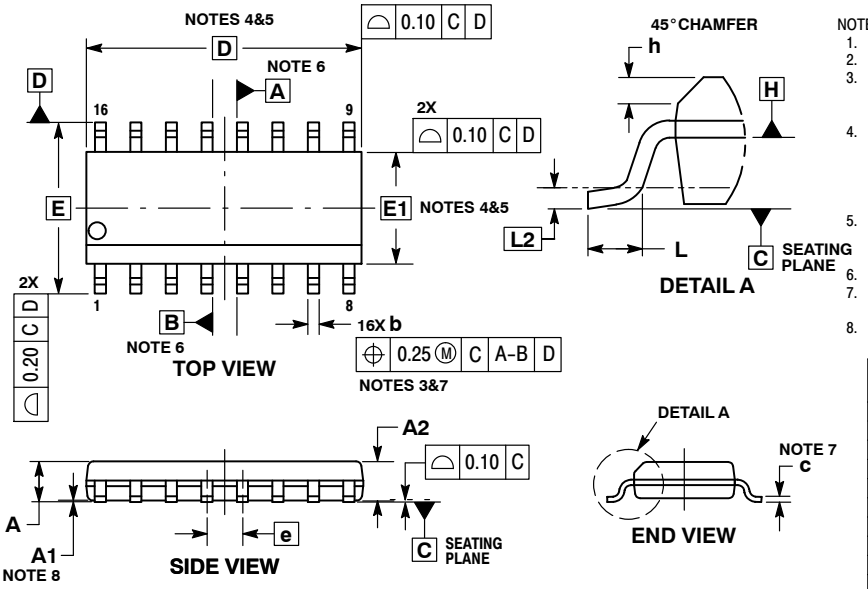
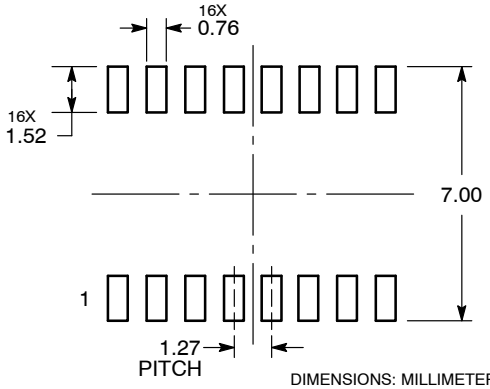
DATE 18 MAY 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

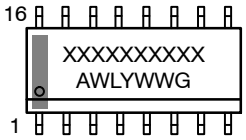
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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