NCV7321

Stand-alone LIN Transceiver

ON Semiconductor®

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Description

The NCV7321 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus. The transceiver is implemented in I3T technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

The NCV7321 LIN device is a member of the in−vehicle networking (IVN) transceiver family.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function. The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

Features

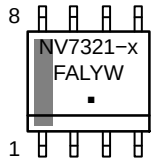
- LIN−Bus Transceiver
  - LIN Compliant to Specification Revision 2.x (Backwards Compatible to Version 1.3) and J2602
  - Bus Voltage ±45 V
  - Transmission Rate 1 kbps to 20 kbps
  - Supports K−Line Bus Architecture
- Protection
  - Thermal Shutdown
  - Indefinite Short−Circuit Protection on Pins LIN and WAKE Towards Supply and Ground
  - Load Dump Protection (45 V)
  - Bus Pins Protected Against Transients in an Automotive Environment
- EMI Compatibility
  - Integrated Slope Control
- Modes
  - Normal Mode: LIN Transceiver Enabled, Communication via the LIN Bus is Possible, INH Switch is On
  - Sleep Mode: LIN Transceiver Disabled, the Consumption from V_{BB} is Minimized, INH Switch is Off
  - Standby Mode: Transition Mode reached either after Power−up or after a Wake−up Event, INH Switch is on
  - Wake−up Bringing the Component from Sleep Mode into Standby Mode is Possible either by LIN Command or a Digital Signal on WAKE Pin (e.g. External Switch)

Quality

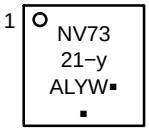
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Require− ments; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS

SOIC−8
CASE 751



DFN8
CASE 506DG

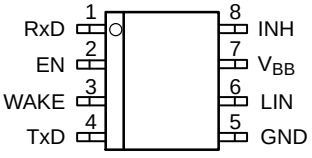


SOIC−8:
x = Specific Device Code
0 = NCV7321D10
1 = NCV7321D11
2 = NCV7321D12

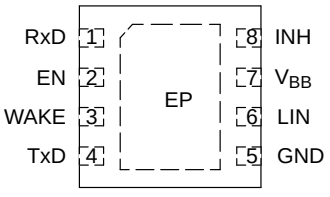
DFN8:
y = Specific Device Code
2 = NCV7321MW2
F = Fab Location Code
(NCV7321D11R2G only)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



SOIC−8 (Top View)



DFN8 (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

RECOMMENDED OPERATING RANGES AND KEY TECHNICAL CHARACTERISTICS

Table 1. RECOMMENDED OPERATING RANGES AND KEY TECHNICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Nominal Battery Operating Voltage (Note 1)	5	12	27	V
	Load Dump Protection			45	
$I_{BB\_}SLP$	Supply Current in Sleep Mode			20	μA
V_{LIN}	LIN Bus Voltage	−45		45	V
V_{WAKE}	Operating DC Voltage on WAKE Pin	0		V_{BB}	V
	Maximum Rating Voltage on WAKE Pin	−35		45	V
V_{INH}	Operating DC Voltage on INH Pin	0		V_{BB}	V
V_Dig_IO	Operating DC Voltage on Digital IO Pins (EN, RxD, TxD)	0		5.5	V
T_{JSD}	Junction Thermal Shutdown Temperature	150	165	185	°C
T_{amb}	Operating Ambient Temperature	−40		+125	°C
V_{ESD}	Electrostatic Discharge Voltage (all pins) Human Body Model (Note 2)	−4		+4	kV
	Version NCV7321D11/D12/MW2; no filter on LIN Electrostatic Discharge Voltage (LIN) System Human Body Model (Note 3)	−10		+10	kV
V_{TRAN}	Version NCV7321D12/MW2; Voltage transients (DCC method), pin LIN According to SAE J2962−1, Class C (Note 4)	−85		+85	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Below 5 V on V_{BB} in normal mode, the bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit. Above 27 V on V_{BB}, LIN communication is operational (LIN pin toggling) but parameters cannot be guaranteed. For higher battery voltage operation above 27 V, LIN pull−up resistor must be selected large enough to avoid clamping of LIN pin by voltage drop over external pull−up resistor and LIN pin min current limitation.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor conform to MIL STD 883 method 3015.7.
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test−house.
4. Direct Capacitor Coupling (DCC) method according to SAE J2962−1 specification, referring to ISO 7637−3 Slow Transient Pulse. Coupling Capacitor 10 nF. Tested with no external protections. Verified by an external test house.

Table 2. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal characteristics, SOIC−8 (Note 5)			
Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 6)	$R_{\theta JA}$	125	°C/W
Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 7)	$R_{\theta JA}$	75	°C/W
Thermal characteristics, DFN8 (Note 5)			
Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 6)	$R_{\theta JA}$	140	°C/W
Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 7)	$R_{\theta JA}$	47	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
7. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

BLOCK DIAGRAM

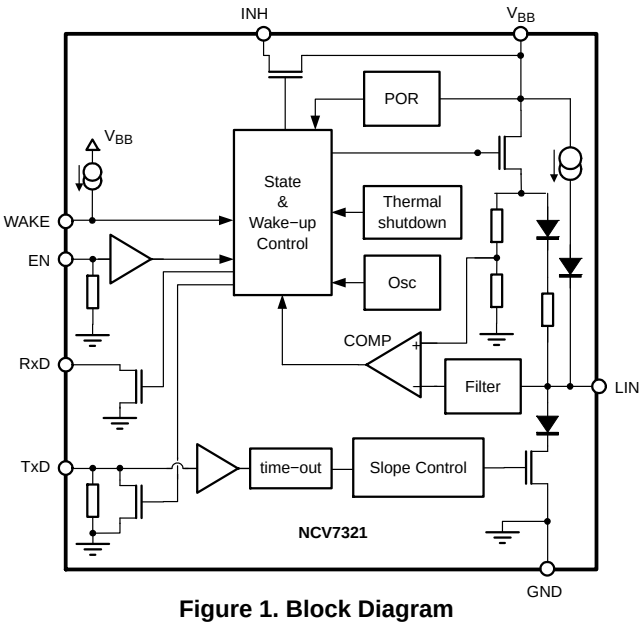


Figure 1. Block Diagram

TYPICAL APPLICATION

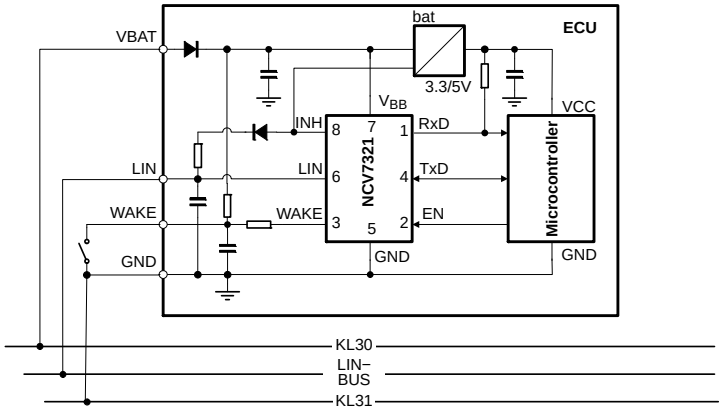


Figure 2. Typical Application Diagram for a Master Node

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	RxD	Receive Data Output; Low in Dominant State; Open−Drain Output
2	EN	Enable Input, Transceiver in Normal Operation Mode when High, Pull−down Resistor to GND
3	WAKE	High Voltage Digital Input Pin to Apply Local Wake−up, Sensitive to Falling Edge, Pull−up Current Source to V_{BB}
4	TxD	Transmit Data Input, Low for Dominant State, Pull−down to GND (Switchable Strength for Wake−up Source Recognition)
5	GND	Ground
6	LIN	LIN Bus Output/Input
7	V_{BB}	Battery Supply Input
8	INH	Inhibit Output, Switch Between INH and V_{BB} can be Used to Control External Regulator or Pull−up Resistor on LIN Bus
−	EP	Exposed Pad. Recommended to connect to GND or left floating in application (DFN8 package only).

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Voltage on Pin V_{BB}	−0.3		+45	V
V_{LIN}	LIN Bus Voltage	−45		+45	V
V_{WAKE}	DC Voltage on WAKE Pin	−35		+45	V
V_{INH}	DC Voltage on INH Pin	−0.3		V_{BB} + 0.3	V
I_{INH}	DC Current from INH Pin			50	mA
V_Dig_IO	DC Input Voltage on Pins (EN, RxD, TxD)	−0.3		+45	V
T_J	Maximum Junction Temperature	−40		+150	°C
V_{ESD}	HBM (All Pins) (Note 8)	−4		+4	kV
	CDM (All Pins) (Note 9)	−750		+750	V
	Version NCV7321D10: HBM (LIN, INH, V_{BB}, WAKE) (Note 10) System HBM (LIN, V_{BB}, WAKE) (Note 11)	 −5 −5		 +5 +5	 kV kV
	Version NCV7321D11/D12/MW2: HBM (LIN, INH, V_{BB}, WAKE) (Note 10) System HBM (V_{BB}, WAKE) (Note 12) System HBM (LIN) (Note 12)	 −8 −6 −10		 +8 +6 +10	 kV kV kV
	Version NCV7321D12/MW2: Powered ESD (LIN), Contact/Air, 330 pF / 2 kΩ (Note 13) Powered ESD (LIN), Air, 150 pF / 2 kΩ (Note 13)	 −15 −25		 +15 +25	 kV kV
V_{TRAN}	Version NCV7321D12/MW2; Voltage transients (DCC method), pin LIN According to SAE J2962−1, Class C (Note 14)	−85		+85	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

8. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor conform to MIL STD 883 method 3015.7.
9. Charged device model test according to ESD STM5.3.1−1999.
10. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor referenced to GND.
11. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. 220 nF filter on LIN pin. System HBM levels are verified by an external test−house.
12. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. No filter on LIN pin. System HBM levels are verified by an external test−house.
13. Powered ESD test method according to SAE J2962−1 specification, referring to ISO 10605. Verified by an external test house.
14. Direct Capacitor Coupling (DCC) method according to SAE J2962−1 specification, referring to ISO 7637−3 Slow Transient Pulse. Coupling Capacitor 10 nF. Tested with no external protections. Verified by an external test house.

FUNCTIONAL DESCRIPTION

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class−A multiplex buses with a single master node and a set of slave nodes.

The NCV7321 contains the LIN transmitter, LIN receiver, power−on−reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for the maximum specified transmission speed of 20 kB with EMC performance due to reduced slew rate of the LIN output.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitter off when temperature exceeds the TSD trigger level.

The NCV7321 has four operating states (unpowered mode, standby mode, normal mode and sleep mode) that are determined by the supply voltage V_{BB}, input signals EN and WAKE and activity on the LIN bus.

OPERATING STATES

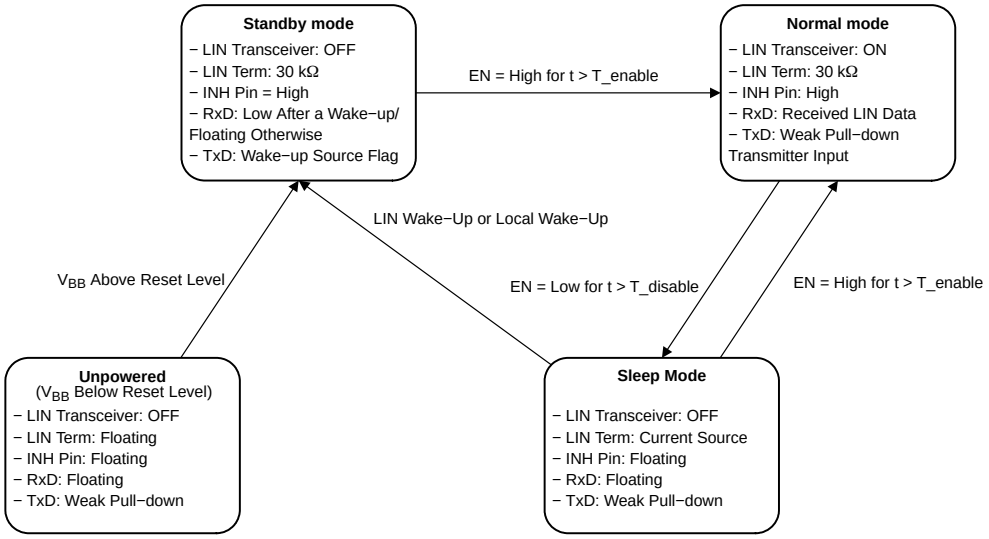


Figure 3. State Diagram

Unpowered Mode

As long as V_{BB} remains below its power−on−reset level, the chip is kept in a safe unpowered state. LIN transmitter is inactive, both LIN and INH pins are left floating and only a weak pull−down is connected on pin TxD. Pin RxD remains floating.

The unpowered state will be entered from any other state when V_{BB} falls below its power−on−reset level.

Standby Mode

Standby mode is a low−power mode, where LIN transceiver remains inactive while INH pin is driven high to activate an external voltage regulator – see Figure 2. Depending on the transition which led to the standby mode, pins RxD and TxD are configured differently during this mode. A 30 kΩ resistor in series with a reverse−protection diode is internally connected between LIN and V_{BB} Pins.

Standby mode is entered in one of the following ways:

- After the voltage level at V_{BB} pin rises above its power−on−reset level. In this case, RxD Pin remains high−impedant and the pull−down applied on pin TxD remains weak.
- After a wake−up event is recognized while the chip was in the sleep mode. Pin RxD is pulled low while pin TxD signals the type of wake−up leading to the standby mode – its pull−up remains weak for LIN wake−up and it is switched to strong pull−down for the case of local wake−up (i.e. wake−up via Pin WAKE).

While in the standby mode, the configuration of Pins RxD and TxD remains unchanged, regardless the activity on WAKE and LIN Pins – i.e. if additional wake−ups occur during the standby mode, they have no influence on the chip configuration.

Normal Mode

In normal mode, the full functionality of the LIN transceiver is available. Data according the state of TxD input are sent to the LIN bus while pin RxD reflects the logical symbol received on the LIN bus – high−impedant for recessive and Low for dominant. A 30 kΩ resistor in series

with a reverse−protection diode is internally connected between LIN and V_{BB} pins.

To avoid that, due to a failure of the application (e.g. software error), the LIN bus is permanently driven dominant and thus blocking all subsequent communication, signal on pin TxD passes through a timer, which releases the bus in case TxD remains low for longer than T_TxD_timeout. The transmission can continue once the TxD returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold, e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases LIN bus to recessive. Once the junction temperature decreases back below the thermal shutdown release level, the transmission can be enabled again – however, to avoid thermal oscillations, first a High logical level on TxD must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless of the TxD signal). A battery monitoring circuit in NCV7321 de−activates the transmitter in the normal mode if the V_{BB} level drops below MONL_V_{BB}. Transmission is enabled again when V_{BB} reaches MONH_V_{BB}. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power−on−reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power−on−reset level.

Normal mode can be entered from either standby or sleep mode when EN Pin is High for longer than T_enable. When the transition is made from standby mode, TxD pull−down is set to weak and RxD is put high−impedant immediately after EN becomes High (before the expiration of T_enable filtering time). This excludes signal conflicts between the standby mode pin settings and the signals required to control the chip in the normal mode (e.g. strong pull−down on TxD after local wake−up vs. High logical level on TxD required to send a recessive symbol on LIN).

Sleep Mode

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized. Pin INH is put to high−impedant state to disable the external regulator and, in case of a master node, the LIN termination – see Figure 2. Only a weak pull−up current source is internally connected between LIN and V_{BB} Pins, in order to minimize current consumption even in case of LIN short to GND.

Sleep mode can be entered from normal mode by assigning Low logical level to pin EN for longer than T_disable. The sleep mode can be entered even if a permanent short occurs either on LIN or WAKE Pin.

If a wake−up event occurs during the transition between normal and sleep mode (during the T_disable filtering time), it will be regarded as valid wake−up and the chip will enter standby mode with the appropriate setting of Pins RxD and TxD.

Wake−up

Two types of wake−up events are recognized by NCV7321:

- Local wake−up – when a high−to−low transition on pin WAKE is encountered and WAKE pin remains Low at least during T_WAKE – see Figure 4.
- Remote (or LIN) wake−up – when LIN bus is externally driven dominant during longer than T_LIN_wake and a rising edge on LIN occurs afterwards – see Figure 5.

Wake−up events can be exclusively detected in sleep mode or during the transition from normal mode to sleep mode. Due to timing tolerances, valid wake−up events beginning shortly before normal−to−sleep mode transition can be also sometimes regarded as valid wake−ups.

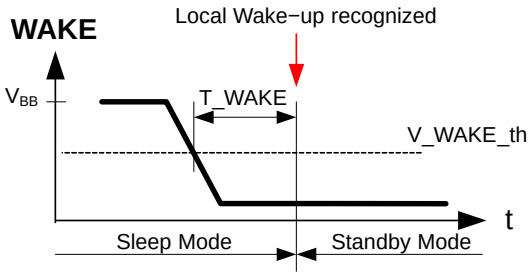


Figure 4. Local Wake−up Detection

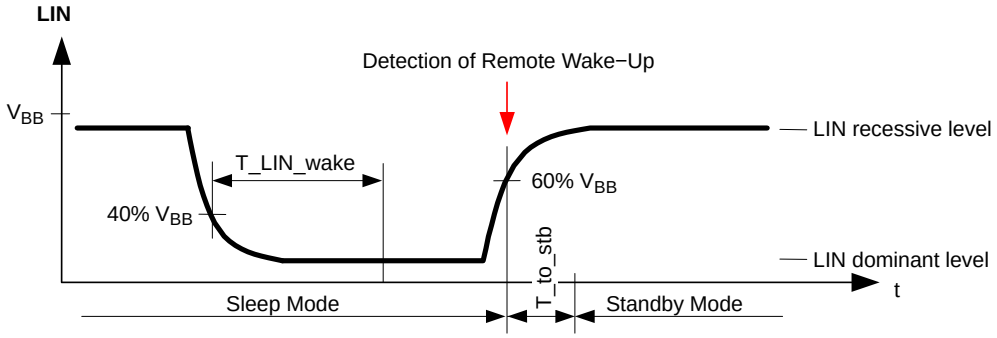


Figure 5. Remote (LIN) Wake−up Detection

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 5). Positive currents flow into the IC.

Table 5. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified. Typical values are given at V_{BB} = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BB} CURRENT CONSUMPTION						
I_{BB}_ON_rec	V_{BB} Consumption	Normal Mode; LIN Recessive $V_{LIN} = V_{BB} = V_{INH} = V_{WAKE}$			1.6	mA
I_{BB}_ON_dom	V_{BB} Consumption	Normal Mode; LIN Dominant $V_{BB} = V_{INH} = V_{WAKE}$			8	mA
I_{BB}_STB	V_{BB} Consumption	Standby Mode $V_{LIN} = V_{BB} = V_{INH} = V_{WAKE}$			350	μA
I_{BB}_SLP	V_{BB} Consumption	Sleep Mode $V_{LIN} = V_{BB} = V_{INH} = V_{WAKE}$			30	μA
I_{BB}_SLP_18V	V_{BB} Consumption	Sleep Mode, V_{BB} < 18 V $V_{LIN} = V_{BB} = V_{INH} = V_{WAKE}$ (Note 15)			20	μA
I_{BB}_SLP_12V	V_{BB} Consumption	Sleep Mode, V_{BB} = 12 V, T_J < 85°C $V_{LIN} = V_{BB} = V_{INH} = V_{WAKE}$ (Note 15)			10	μA
POR AND V_{BB} MONITOR						
PORH_V_{BB}	Power−on Reset High Level on V_{BB}	V_{BB} Rising	2		4.5	V
PORL_V_{BB}	Power−on Reset Low Level on V_{BB}	V_{BB} Falling	1.7		4	V
MONH_V_{BB}	Battery Monitoring High Level	V_{BB} Rising			4.5	V
MONL_V_{BB}	Battery Monitoring Low Level	V_{BB} Falling	3			V
LIN TRANSMITTER						
VLIN_dom_LoSup	LIN Dominant Output Voltage	TxD = Low; V_{BB} = 7.3 V			1.2	V

15. Values based on design and characterization. Not tested in production.
16. The voltage drop in Normal mode between LIN and VBB pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 5. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified. Typical values are given at V_{BB} = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
VLIN_dom_HiSup	LIN Dominant Output Voltage	TxD = Low; V_{BB} = 18 V			2.0	V
VLIN_REC	LIN Recessive Output Voltage (Note 16)	TxD = High; I_{LIN} = 10 μA	V_{BB} − 1.5		V_{BB}	V
ILIN_lim	Short Circuit Current Limitation	V_{LIN} = V_{BB}_max	40		200	mA
R_{slave}	Internal Pull−up Resistance		20	33	47	kΩ
CLIN	Capacitance on Pin LIN (Note 15)			20	30	pF
LIN RECEIVER						
Vbus_dom	Bus Voltage for Dominant State				0.4	V_{BB}
Vbus_rec	Bus Voltage for Recessive State		0.6			V_{BB}
Vrec_dom	Receiver Threshold	LIN Bus Recessive − Dominant	0.4		0.6	V_{BB}
Vrec_rec	Receiver Threshold	LIN Bus Dominant − Recessive	0.4		0.6	V_{BB}
Vrec_cnt	Receiver Centre Voltage	(Vrec_dom + Vrec_rec)/2	0.475		0.525	V_{BB}
Vrec_hys	Receiver Hysteresis	(Vrec_rec − Vrec_dom)	0.05		0.175	V_{BB}
ILIN_off_dom	LIN Output Current, Bus in Dominant State	Normal Mode, Driver Off; V_{BB} = 12 V, V_{LIN} = 0 V	−1			mA
ILIN_off_dom_slp	LIN Output Current, Bus in Dominant State	Sleep Mode, Driver Off; V_{BB} = 12 V, V_{LIN} = 0 V	−20	−15	−2	μA
ILIN_off_rec	LIN Output Current, Bus in Recessive State	Driver Off; V_{BB} < 18 V; V_{BB} < V_{LIN} < 18 V			1	μA
ILIN_no_GND	Communication not Affected	V_{BB} = GND = 12 V; 0 < V_{LIN} < 18 V	−1		1	mA
ILIN_no_V_{BB}	LIN Bus Remains Operational	V_{BB} = GND = 0 V; 0 < V_{LIN} < 18 V			5	μA
PIN EN						
Vil_EN	Low Level Input Voltage		−0.3		0.8	V
Vih_EN	High Level Input Voltage		2.0		5.5	V
Rpd_EN	Pull−down Resistance to Ground		150	350	650	kΩ
PIN TxD						
Vil_TxD	Low Level Input Voltage		−0.3		0.8	V
Vih_TxD	High Level Input Voltage		2.0		5.5	V
Rpd_TxD	Pull−down Resistor on TxD Pin, Corresponding to “Weak Pull−down”	Normal Mode or Sleep Mode or Standby Mode after Power up or Standby Mode after LIN Wake−up	150	350	650	kΩ

15. Values based on design and characterization. Not tested in production.
16. The voltage drop in Normal mode between LIN and VBB pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 5. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified. Typical values are given at V_{BB} = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PIN TxD						
Ipd_TxD_Strong	Pull−down Current on TxD Pin Corresponding to “Strong Pull−down”	Standby Mode after Local Wake−up	1.5			mA
PIN RxD						
Iol_RxD	Low Level Output Current	V_{RxD} = 0.4 V, Normal Mode, V_{LIN} = 0 V	1.5			mA
Ioh_RxD	High Level Output Current	V_{RxD} = 5 V, Normal Mode, V_{LIN} = V_{BB}	−5	0	5	μA
PIN WAKE						
V_wake_th	WAKE Threshold Voltage		V_{BB} − 3.3		V_{BB} − 1.1	V
I_wake_pull−up	Pull−up Current on Pin WAKE	V_{WAKE} = 0 V	−30	−15	−1	μA
I_wake_leak	Leakage of Pin WAKE	V_{WAKE} = V_{BB}	−5	0	5	μA
PIN INH						
Delta_VH	High Level Voltage Drop	I_{INH} = 15 mA, INH Active	0.05	0.35	0.75	V
I_leak	Leakage Current	Sleep Mode; V_{INH} = 0 V	−1	0	1	μA
THERMAL SHUTDOWN						
T_{JSD}	Thermal Shutdown Junction Temperature	Temperature Rising	150	165	185	°C
T_{JSD}_hyst	Thermal Shutdown Hysteresis			5		°C

15. Values based on design and characterization. Not tested in production.
16. The voltage drop in Normal mode between LIN and VBB pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 6. AC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x T_{BIT})	$TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} T_{BIT} = 50 µs V_{BB} = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x T_{BIT})	$TH_{REC(min)}$ = 0.422 x V_{BB} $TH_{DOM(min)}$ = 0.284 x V_{BB} T_{BIT} = 50 µs V_{BB} = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x T_{BIT})	$TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} T_{BIT} = 96 µs V_{BB} = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x T_{BIT})	$TH_{REC(min)}$ = 0.389 x V_{BB} $TH_{DOM(min)}$ = 0.251 x V_{BB} T_{BIT} = 96 µs V_{BB} = 7.6 V to 18 V	0.5		0.590	
Ttx_prop_down	Propagation Delay of TxD to LIN. TxD high to low	(Note 17)			6	µs
Ttx_prop_up	Propagation Delay of TxD to LIN. TxD low to high	(Note 17)			6	µs
T_fall	LIN Falling Edge	Normal Mode; V_{BB} = 12 V			22.5	µs
T_rise	LIN Rising Edge	Normal Mode; V_{BB} = 12 V			22.5	µs
T_sym	LIN Slope Symmetry	Normal Mode; V_{BB} = 12 V	−4	0	4	µs
LIN RECEIVER						
Trec_prop_down	Propagation Delay of Receiver Falling Edge		0.1		6	µs
Trec_prop_up	Propagation Delay of Receiver Rising Edge		0.1		6	µs
Trec_sym	Propagation Delay Symmetry	Trec_prop_down − Trec_prop_up	−2		2	µs
MODE TRANSITIONS AND TIMEOUTS						
T_LIN_wake	Duration of LIN Dominant for Detection of Wake−up via LIN bus	Sleep Mode	30	90	150	µs
T_to_stb	Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake−up	Sleep Mode		10		µs
T_WAKE	Duration of Low Level on WAKE Pin for Local Wake−up Detection	Sleep Mode	7		50	µs
T_enable	Duration of High Level on EN Pin for Tran−sition to Normal Mode	Version NCV7321D10	2	5	10	µs
		Version NCV7321D11/D12/MW2	2	7.5	18.5	µs
T_disable	Duration of Low Level on EN Pin for Tran−sition to Sleep Mode	Version NCV7321D10	2	5	10	µs
		Version NCV7321D11/D12/MW2	2	7.5	18.5	µs
T_TxD_timeout	TxD Dominant Time−Out	Normal Mode, TxD = Low, Guaran−tees Baudrate as Low as 1 kbps	15		50	ms

17. Values based on design and characterization. Not tested in production.

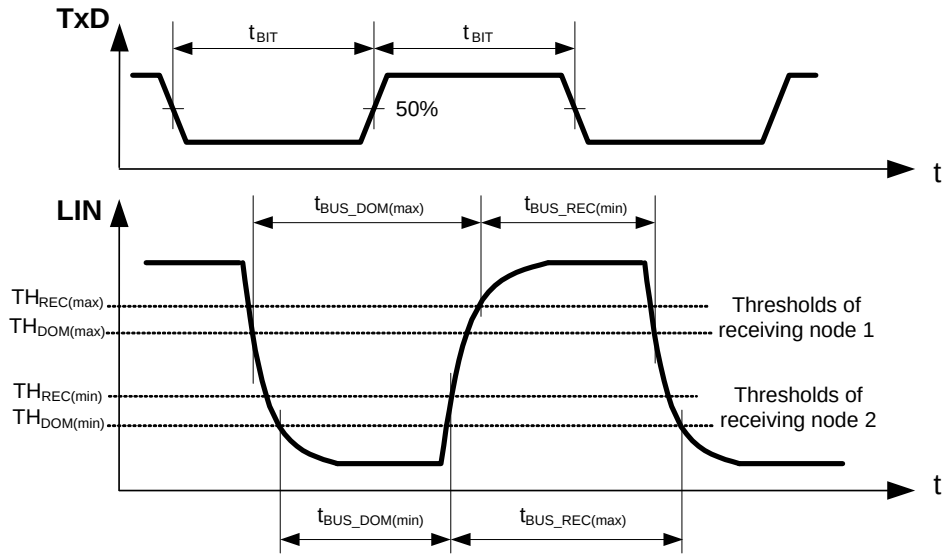


Figure 6. LIN Transmitter Duty Cycle

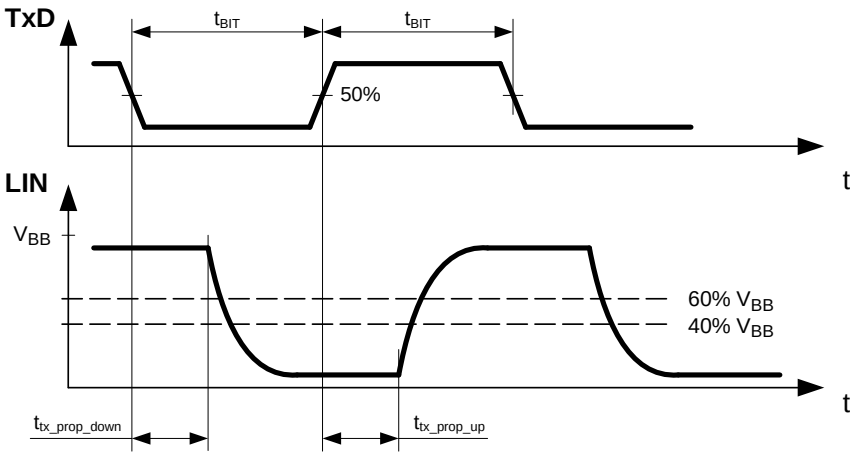


Figure 7. LIN Transmitter Timing

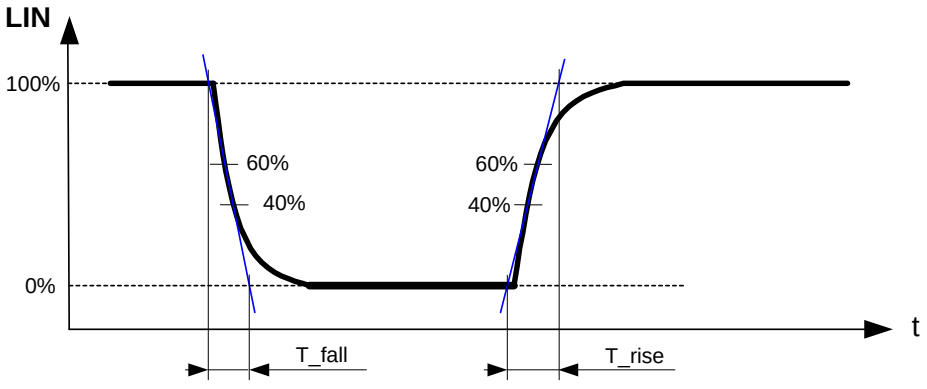


Figure 8. LIN Transmitter Rising and Falling Times

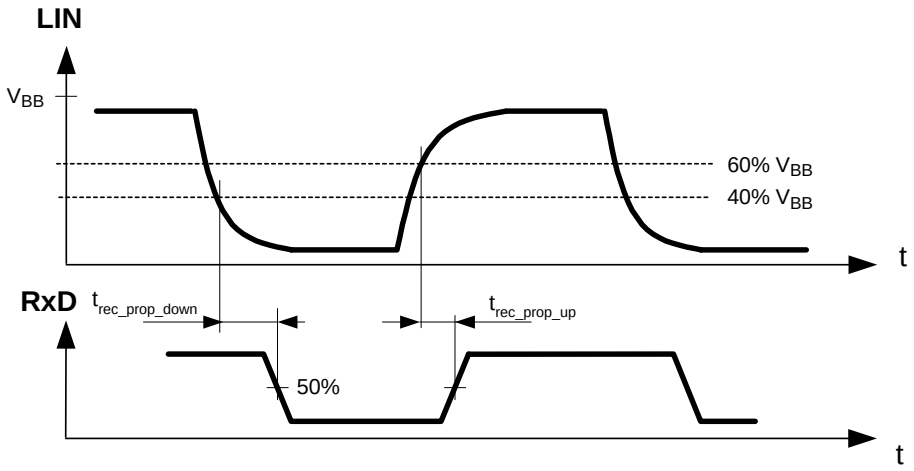


Figure 9. LIN Receiver Timing

DEVICE ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping†
NCV7321D10G	Stand−alone LIN Transceiver	−40°C to +125°C	SOIC−8 (Pb−Free)	96 Tube / Tray
NCV7321D10R2G				3000 / Tape & Reel
NCV7321D11G	Improved Stand−alone LIN Transceiver			96 Tube / Tray
NCV7321D11R2G				3000 / Tape & Reel
NCV7321D12R2G	ESD Improved Stand−alone LIN Transceiver	−40°C to +125°C	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NCV7321MW2R2G			DFN8 Wettable Flank (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

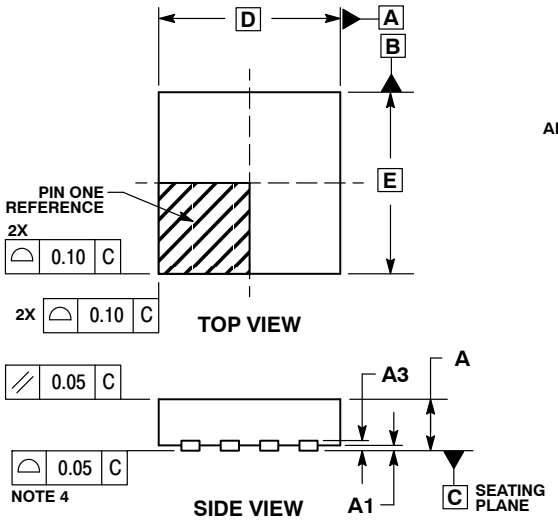
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

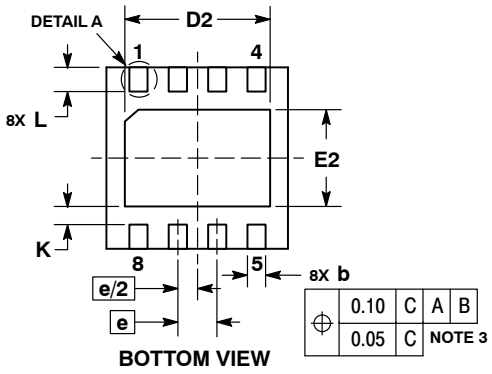
ON Semiconductor®

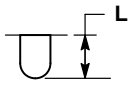
DFN8, 3x3, 0.65P
CASE 506DG
ISSUE A

DATE 28 APR 2016

SCALE 2:1





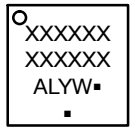


DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.30	2.50
E	3.00 BSC	
E2	1.50	1.70
e	0.65 BSC	
K	0.30 TYP	
L	0.35	0.45

GENERIC MARKING DIAGRAM*

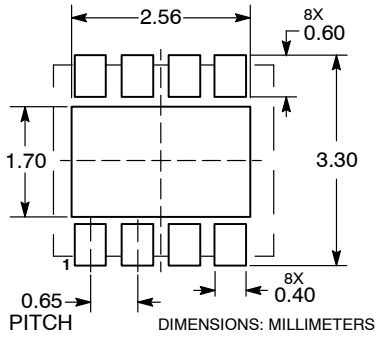


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8 3X3, 0.65P**	**PAGE 1 OF 1**

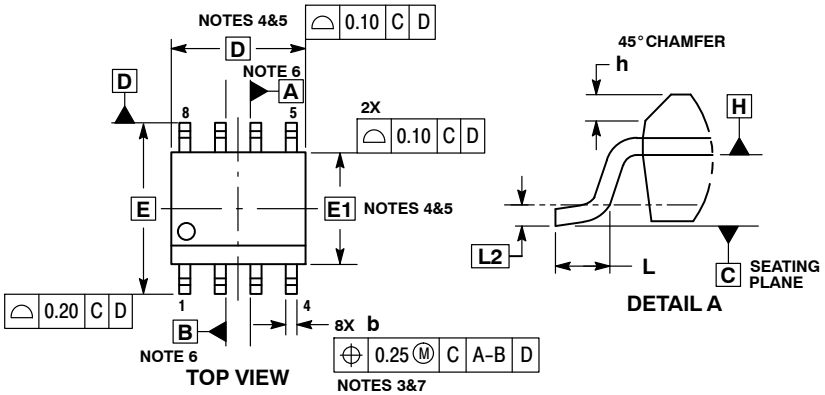
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

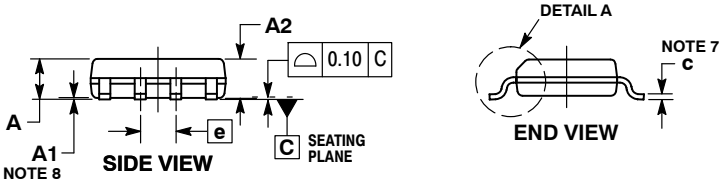
ON Semiconductor®

SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

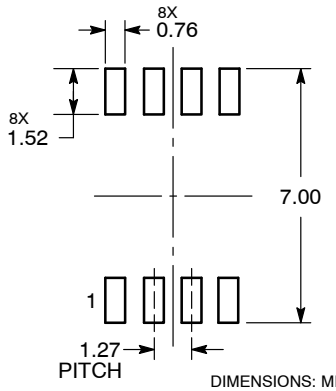




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

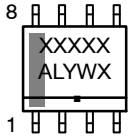
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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L = Wafer Lot
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W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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