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CAN FD Transceiver, Low Power, with INH, WAKE and Error Detection

NCV7343

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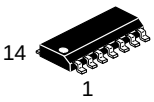
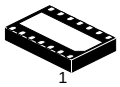


SOIC−14
D2 SUFFIX
CASE 751A−03



DFNW14 4.5x3, 0.65P
MW SUFFIX
CASE 507AC

Description

The NCV7343 CAN FD transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7343 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

The NCV7343 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbit/s to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7343 an excellent choice for all types of HS−CAN networks, in nodes that require a low−power mode with wake−up capability via the CAN bus.

Features

- Compliant with International Standard ISO11898−2:2016
- CAN FD Timing Specified up to 5 Mbit/s
- Extended Bus Load Range
- Standby and Sleep Mode with very Low Current Consumption
- CAN Wake−up with Wake−up Pattern (WUP), Short CAN Activity Filter Time, Long Wake−up Timeout and Normal Bus Biasing.
- Local Wake−up
- V_{IO} Pin Allowing Direct Interfacing with 3 V to 5 V MCUs
- Low Electromagnetic Emission (EME) and High Electromagnetic Susceptibility (EMS)
- High Impedance Bus Lines in Unpowered State
- Transmit Data (TxD) Dominant Timeout Function (Long)
- Bus Error Detection
- Under all Supply Conditions the Chip behaves Predictably
- ESD Robustness of Bus Pins > 8 kV
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected against Transients in an Automotive Environment
- AEC−Q100 Grade 0 Qualified and PPAP Capable
- These are Pb−Free Devices

Quality

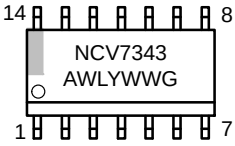
- Wettable Flank Package for Enhanced Optical Inspection

Typical Applications

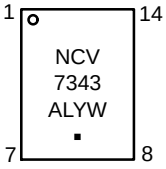
- Automotive
- Industrial Networks

MARKING DIAGRAMS

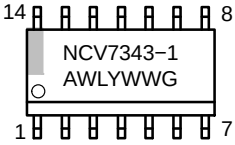
NCV7343D20



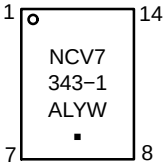
NCV7343MW0



NCV7343D21



NCV7343MW1



SOIC−14 **DFNW14**

A = Assembly Site
(W)L = Wafer Lot
YW(W) = Date Code
G or ▪ = Pb−Free Identification

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

TYPICAL APPLICATION

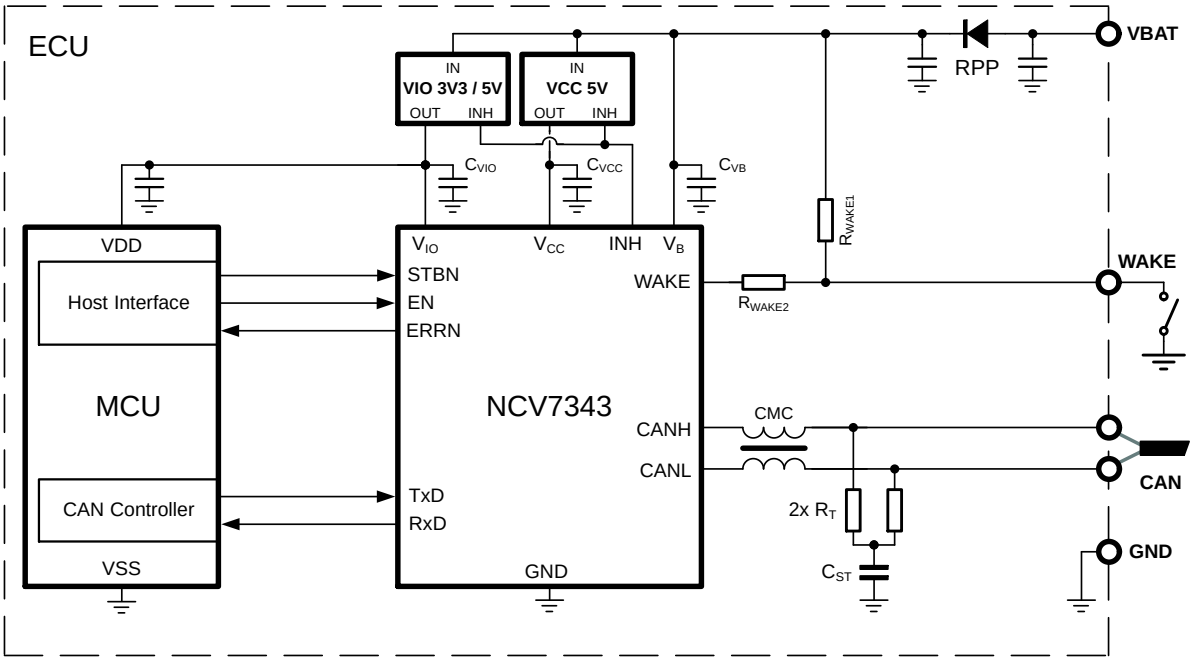


Figure 1. Typical Application Diagram

RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATIONS DIAGRAM

Symbol	Parameter	Value	Unit	Note
C_{VB}	Decoupling Capacitor on V_B Supply Pin, Ceramic	100	nF	
C_{VCC}	Decoupling Capacitor on V_{CC} Supply Pin, Ceramic	1	μF	
C_{VIO}	Decoupling Capacitor on V_{IO} Supply Pin, Ceramic	100	nF	
R_{WAKE1}	WAKE Pin Pull−up Resistor	33	kΩ	
R_{WAKE2}	WAKE Pin Serial Protection Resistor	3.3	kΩ	
CMC	Common Mode Choke	100	μH	(Note 1)
R_{LT}	Terminating Resistors	60	Ω	< 1%, ≥ 0.25 W
C_{ST}	Common−mode Stabilization Capacitor, Ceramic	4.7	nF	< 20%, 50 V

1. Murata DLW32SH101XF2, Murata DLW32SH101XK2, TDK ACT45B−101−2P, TDK ACT1210R−101−2P

BLOCK DIAGRAM

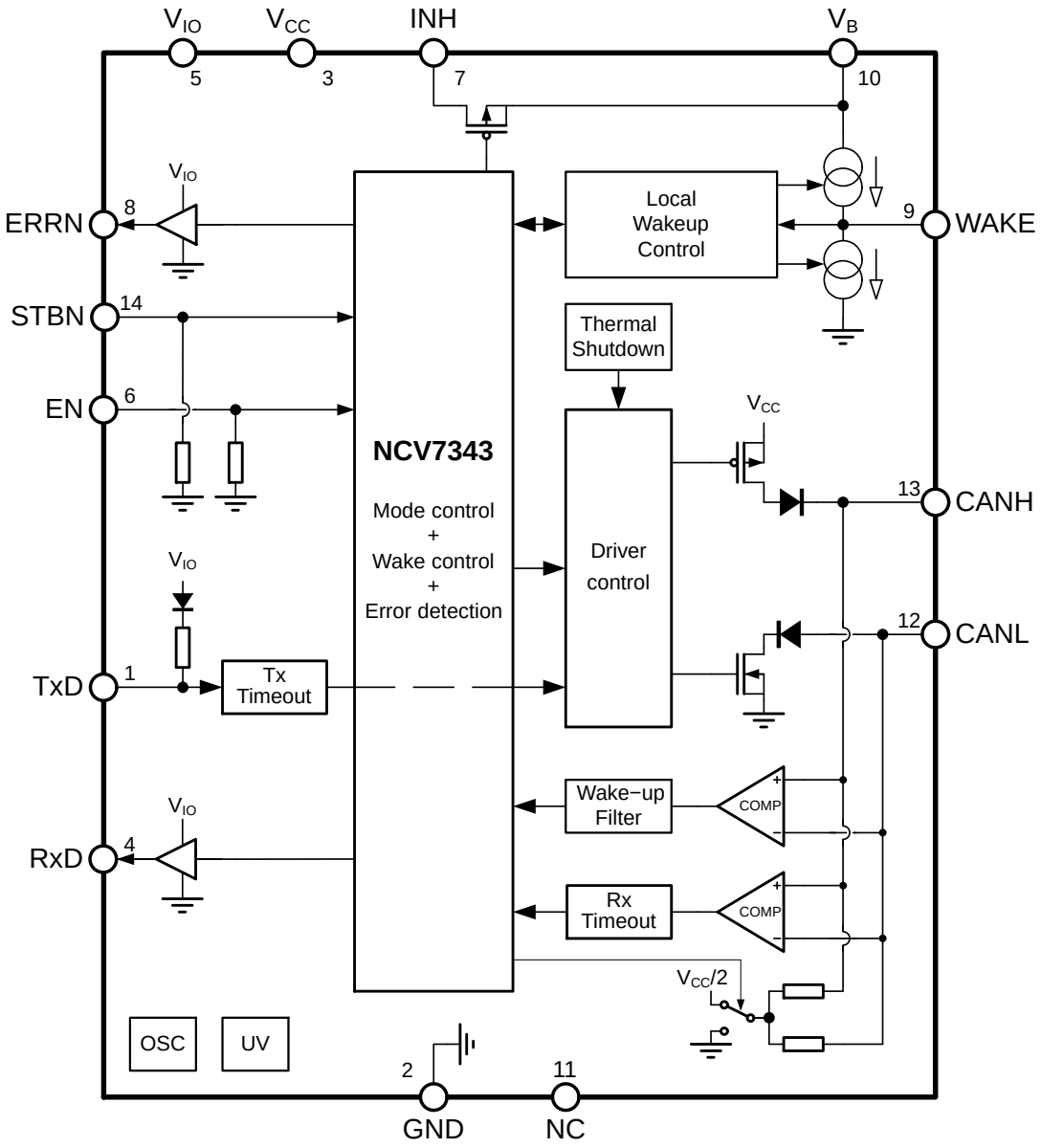
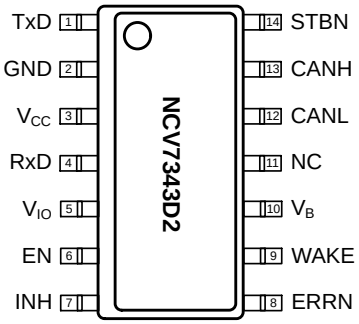


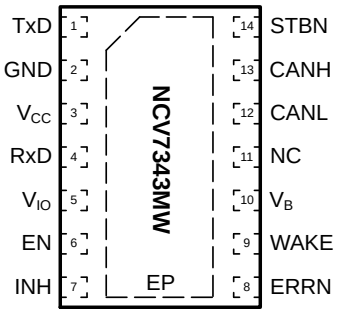
Figure 2. NCV7343 Block Diagram

PIN CONNECTIONS



(Top View)

Figure 3. Pin Connections − SOIC−14



(Top View)

Figure 4. Pin Connections − DFNW14

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull−up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5	V_{IO}	Input / Output pins supply voltage
6	EN	Enable mode control input; internal pull−down current
7	INH	High voltage output for controlling external voltage regulators
8	ERRN	Digital output indicating errors and power−up; active low
9	WAKE	Local wake−up input
10	V_B	Battery supply connection
11	N_C	Not connected
12	CANL	Low−level CAN bus line (low in dominant mode)
13	CANH	High−level CAN bus line (high in dominant mode)
14	STBN	Standby mode control input; internal pull−down current
15	EP	Exposed Pad. Recommended to connect to GND or left floating in application (DFNW14 package only)

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_B	Supply Voltage, Pin V_B	(Note 2)	−0.3	+40	V
V_{SUP}	Supply Voltage, Pin V_{CC}, V_{IO}	(Note 2)	−0.3	+6.0	V
V_{CAN}	DC Voltage at Pins CANH and CANL	$0 < V_{CC} < 5.5$ V	−42	+42	V
V_{DIFF}	DC Voltage between Any Two Pins (Including CANH and CANL)		−42	+42	V
V_{DIG_IN}	DC Voltage at Pin TxD, STBN, EN		−0.3	+40	V
V_{DIG_OUT}	DC Voltage at Pin RxD, ERRN		−0.3	V_{IO} + 0.3	V
V_{INH}	DC Voltage at Pin INH		−0.3	V_B + 0.3	V
I_{INH}	DC Current on INH Pin		−5	0	mA
V_{WAKE}	DC Voltage at Pin WAKE		−42	+42	V
V_{ESD_IEC}	Electrostatic Discharge Voltage at Pins CANH, CANL, V_B and WAKE; System HBM, According to IEC 61000−4−2.	(Note 3)	−8	+8	kV
V_{ESD_HBM}	Electrostatic Discharge Voltage at Pins CANH, CANL, V_B and WAKE; Component HBM, According to JEDEC JESD22−A114.	(Note 4)	−8	+8	kV

MAXIMUM RATINGS (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD_INT}	Electrostatic Discharge Voltage at All Other Pins; Component HBM, According to JEDEC JESD22−A114.	(Note 4)	−4	+4	kV
V_{ESD_CDM}	Electrostatic Discharge Voltage at All Pins; Component CDM, According to JEDEC JESD22−C101.		−750	+750	V
V_{ESD_MM}	Electrostatic Discharge Voltage at All Pins; Component MM, According to JEDEC JESD22−A115.	(Note 5)	−200	+200	V
V_{TRAN}	Voltage Transients, Pins CANH, CANL. Test Pulses According to ISO7637−2, Class C, (Note 6)	Test pulses 1	−100	−	V
		Test pulses 2a	−	+75	V
		Test pulses 3a	−150	−	V
		Test pulses 3b	−	+100	V
	Voltage Transients, Pin V_B, According to ISO7637−2	Test pulse 5 Load dump	−	40	V
Latch−up	Static Latch−up at All Pins, According to JEDEC JESD78		−	150	mA
T_J	Maximum Junction Temperature		−40	+160	°C
T_{STG}	Storage Temperature		−55	+150	°C
MSL	Moisture Sensitivity Level	SOIC−14	2		
		DFNW14	1		
T_{SLD}	Peak Soldering Temperature (Note 7)		−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor, referenced to GND. WAKE pin stressed through an external series resistor 3.3 kΩ and with 10 nF capacitor on the module input. VB pin decoupled with 100 nF during stressing. Results were verified by an external test house.
4. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
5. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
6. Results were verified by an external test house.
7. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−14 (Note 8)			
Thermal Resistance Junction−to−Air, (Note 9)	$R_{\theta JA\_1}$	100	K/W
Thermal Resistance Junction−to−Air, (Note 10)	$R_{\theta JA\_2}$	63	
Thermal Characteristics, DFNW14 (Note 8)			
Thermal Resistance Junction−to−Air, (Note 9)	$R_{\theta JA\_1}$	115	K/W
Thermal Resistance Junction−to−Air, (Note 10)	$R_{\theta JA\_2}$	65	

8. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
9. Test board according to EIA/JEDEC Standard JESD51−3 (1S0P PCB), signal layer with 10% trace coverage.
10. Test board according to EIA/JEDEC Standard JESD51−7 (2S2P PCB), signal layers with 10% trace coverage.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_B	Supply Voltage, Pin V_B		5.0	40	V
V_{CC}	Supply Voltage, Pin V_{CC}		4.5	5.5	V
V_{IO}	Supply Voltage, Pin V_{IO}		2.8	5.5	V
V_{CAN}	DC Voltage at Pins CANH and CANL		−36	36	V
V_{DIG_IN}	DC Voltage at Pins TxD, STBN, and EN		0	5.5	V
V_{DIG_OUT}	DC Voltage at Pins RxD and ERRN		0	V_{IO}	V
V_{INH}	DC Voltage at Pin INH		0	V_B	V
I_{INH}	DC Current on Pin INH		−1	0	mA

RECOMMENDED OPERATING RANGES (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{WAKE}	DC Voltage at Pin WAKE		−42	V_B	V
T_J	Junction Temperature		−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} SUPPLY (Pin V_{CC})						
V_{CC}	Power Supply Voltage		4.5	−	5.5	V
I_{CC}	Supply Current	Normal mode, Dominant, V_{TxD} = 0 V	−	47	61	mA
		Normal mode, Recessive, V_{TxD} = V_{IO}	−	3.2	6.2	mA
		Silent mode, Recessive	−	1.0	3.2	mA
		Normal mode, Dominant, V_{TxD} = 0 V, one of bus wires shorted (Note 11) −3 V ≤ V_{CANH}, V_{CANL} ≤ +18 V	−	−	103	mA
I_{CC_LP}	Supply Current in Low−power Modes (Standby or Sleep Mode)	Standby or Sleep mode, V_{CC} = 5 V V_B > V_{CC}, T_J ≤ 100°C (Note 11)	−	11	20	μA
V_{uv_VCC}	Undervoltage Detection Threshold		3.5	3.8	4.3	V
V_{uvh_VCC}	Undervoltage Threshold Hysteresis		−	120	−	mV
V_{IO} SUPPLY VOLTAGE (Pin V_{IO})						
V_{IO}	Supply Voltage on Pin V_{IO}		2.8	−	5.5	V
I_{IO}	Normal−power Mode Supply Current	Normal or Silent mode; V_{TxD} = 0 V	−	110	300	μA
		Normal or Silent mode, V_{TxD} = V_{IO}	−	1.5	7.0	μA
I_{IO_LP}	Low−power Mode Supply Current	Standby or Sleep mode; V_{TxD} = V_{IO}; T_J ≤ 100°C (Note 11)	−	1.0	4.0	μA
V_{uv_VIO}	Undervoltage Detection Threshold		2.0	2.2	2.8	V
V_{uvh_VIO}	Undervoltage Threshold Hysteresis		−	280	−	mV
V_B SUPPLY VOLTAGE (Pin V_B)						
V_B	Supply Voltage on Pin V_B		5.0	−	40	V
I_B	Normal−power Mode Supply Current	Normal and Silent mode; V_B = 5 V to 38 V	−	3.5	7.0	μA
I_{B_LP}	Low−power Mode Supply Current	Standby mode V_{WAKE} = V_B; V_B = 5 V to 38 V	−	3.5	7.0	μA
		Sleep mode V_{VCC} = V_{VIO} = 0 V, V_{WAKE} = V_B; V_B = 5 V to 38 V T_J ≤ 100°C (Note 11)	−	13	20	μA
$I_{B\_LP\_VB\&VCC}$	Sum of Low−power Mode Supply Current to Battery and V_{CC} Pin	Sleep and Standby Mode V_{VCC} = V_{VIO} = 5 V, V_B = 5 V to 38 V T_J ≤ 100°C (Note 11)	−	14	23	μA

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_B SUPPLY VOLTAGE (Pin V_B)						
V_{uvd_VB}	Undervoltage Detection Threshold	V_B falling	3.7	4.1	4.5	V
V_{uvr_VB}	Undervoltage Recovery Threshold	V_B rising	3.9	4.4	4.9	V
V_{uvh_VB}	Undervoltage Threshold Hysteresis		100	300	400	mV
TRANSMITTER DATA INPUT (PIN TxD)						
V_{IH}	High−level Input Voltage	Output recessive	2.0	−	−	V
V_{IL}	Low−level Input Voltage	Output dominant	−	−	0.8	V
I_{IH}	High−level Input Current	V_{TxD} = V_{IO}	−5.0	0	+5.0	μA
R_{PU}	Pull−up Resistor		10	25	50	kΩ
I_{LEAK}	Leakage Current	V_{TxD} = 5.5 V, V_{IO} = 0 V	−1.0	0	+1.0	μA
C_i	Input Capacitance	(Note 11)	−	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level Output Current	V_{RxD} = V_{IO} − 0.4 V	−8.0	−3.0	−1.0	mA
I_{OL}	Low−level Output Current	V_{RxD} = 0.4 V	1.0	6.0	12	mA
TRANSMITTER MODE SELECT (Pin STBN, EN)						
V_{IH}	High−level Input Voltage	Standby mode	2.0	−	−	V
V_{IL}	Low−level Input Voltage	Normal mode	−	−	0.8	V
R_{PD}	Pull−down Resistor		300	650	1000	kΩ
I_{IL}	Low−level Input Current	V_{STBN} = 0 V	−1.0	0	+1.0	μA
I_{LEAK}	Leakage Current	V_{STBN} = 5.5 V, V_B = V_{CC} = V_{IO} = 0 V	−1.0	0	+1.0	μA
C_i	Input Capacitance	(Note 11)	−	5	10	pF
ERROR SIGNALING (Pin ERRN)						
I_{OH}	High Level Output Current	V_{ERRN} = V_{IO} − 0.4 V	−100	−50	−10	μA
I_{OL}	Low Level Output Current	V_{ERRN} = 0.4 V	0.1	0.5	1.0	mA
LOCAL WAKE−UP INPUT (Pin WAKE)						
V_{IH}	High−level Input Voltage	Standby or Sleep	V_B − 2	−	−	V
V_{IL}	Low−level Input Voltage	Standby or Sleep	−	−	V_B − 4	V
I_{IH}	High−level Input Current	V_{WAKE} = V_B − 2 V; V_{WAKE} = High for t ≥ t_{wake_filt} (Pull−up active)	−11	−	−3.0	μA
I_{IL}	Low−level Input Current	V_{WAKE} = V_B − 4 V; V_{WAKE} = Low for t ≥ t_{wake_filt} (Pull−down active)	3.0	−	11	μA
INHIBIT OUTPUT (Pin INH)						
V_{OH}	High−level Output Voltage	I_{INH} = −1 mA	V_B − 0.6	V_B − 0.27	V_B − 0.1	V
I_{LEAK}	Leakage Current	Sleep or Power−off mode, V_{INH} = 0 V	−5	0	+5	μA
CAN TRANSMITTER (Pins CANH and CANL)						
$V_{o(dom)(CANH)}$	Dominant Output Voltage at Pin CANH	Normal mode; V_{TxD} = Low; t < $t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 65 Ω	2.75	3.65	4.5	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN TRANSMITTER (Pins CANH and CANL)						
$V_{o(dom)(CANL)}$	Dominant Output Voltage at Pin CANL	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 65 Ω	0.5	1.35	2.25	V
$V_{o(rec)}$	Recessive Output Voltage at Pins CANH and CANL	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load	2.0	2.5	3.0	V
$V_{o(off)}$	Recessive Output Voltage at Pins CANH and CANL	Standby or Sleep mode; no load	−0.1	0	+0.1	V
$V_{o(dom)(diff)}$	Differential Dominant Output Voltage ($V_{CANH} - V_{CANL}$)	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 50 Ω ≤ R_{LT} ≤ 65 Ω	1.5	2.3	3.0	V
$V_{o(dom)(diff)\_E}$		Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 70 Ω	1.4	2.3	3.3	V
$V_{o(dom)(diff)\_ARB}$		Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; R_{LT} = 2 240 Ω	1.5	–	5.0	V
$V_{o(rec)(diff)}$	Differential Recessive Output Voltage ($V_{CANH} - V_{CANL}$)	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load	−50	0	+50	mV
$V_{o(off)(diff)}$	Differential Recessive Output Voltage ($V_{CANH} - V_{CANL}$)	Standby or Sleep Mode; no load	−0.2	0	+0.2	V
$V_{o(sym)}$	Driver Output Voltage Symmetry $V_{o(sym)} = V_{CANH} + V_{CANL}$	TxD = square wave up to 1 MHz; C_{ST} = 4.7 nF	0.9	1.0	1.1	V_{CC}
$I_{o(sc)(CANH)}$	Short Circuit Output Current at Pin CANH in Dominant	Normal mode; V_{TxD} = Low, $t < t_{dom(TxD)}$; −3 V ≤ V_{CANH} ≤ +18 V NCV7343xx0 NCV7343xx1	 −100 −100	 −70 −70	 +2.0 +5.0	mA
$I_{o(sc)(CANL)}$	Short Circuit Output Current at Pin CANL in Dominant	Normal mode; V_{TxD} = Low, $t < t_{dom(TxD)}$; −3 V ≤ V_{CANL} ≤ +36 V NCV7343xx0 NCV7343xx1	 −2.0 −2.0	 +70 +70	 +100 +100	mA
$I_{o(sc)(rec)}$	Short Circuit Output Current at Pins CANH and CANL in Recessive	Normal or Silent mode; −27 V < V_{CANH}, V_{CANL} < +32 V NCV7343xx0 NCV7343xx1	 −3.0 −6.0	 – –	 +3.0 +6.0	mA
CAN RECEIVER (Pins CANH and CANL)						
$I_{LEAK(off)}$	Input Leakage Current	0 Ω < R(V_{CC} to GND) < 1 MΩ V_{CANH} = V_{CANL} = 5 V	−5.0	0	+5.0	μA
		V_B = V_{CC} = V_{IO} = 0 V V_{CANH} = V_{CANL} = 5 V	−5.0	0	+5.0	μA
$V_{i(rec)(diff)\_NM}$	Differential Input Voltage Range Recessive State	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	−3.0	–	+0.5	V
$V_{i(rec)(diff)\_LP}$		Standby or Sleep mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	−3.0	–	+0.4	V
$V_{i(dom)(diff)\_NM}$	Differential Input Voltage Range Dominant State	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.9	–	8.0	V
$V_{i(dom)(diff)\_LP}$		Standby or Sleep mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	1.05	–	8.0	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN RECEIVER (Pins CANH and CANL)						
$V_{i(th)(diff)\_NM}$	Differential Receiver Threshold Voltage	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.5	−	0.9	V
$V_{i(th)(diff)\_NM\_E}$		Normal or Silent mode; Extended, −30 V ≤ V_{CANH}, V_{CANL} ≤ +35 V; no load	0.4	−	1.0	V
$V_{i(th)(diff)\_LP}$		Standby or Sleep mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.4	−	1.05	V
$R_{i(cm)}$	Common−mode Input Resistance at Pins CANH and CANL	−2 V ≤ V_{CANH}, V_{CANL} ≤ +7 V	6.0	−	50	kΩ
$R_{i(cm)(m)}$	Matching between Pin CANH and Pin CANL Common Mode Input Resistance	V_{CANH} = V_{CANL} = +5 V	−1	0	+1	%
$R_{i(diff)}$	Differential Input Resistance	$R_{i(diff)}$ = $R_{i(cm)(CANH)}$ + $R_{i(cm)(CANL)}$ −2 V ≤ V_{CANH}, V_{CANL} ≤ +7 V	12	−	100	kΩ
C_i	Input Capacitance at Pins CANH and CANL	V_{TxD} = High; (Note 11)	−	7.5	20	pF
$C_{i(diff)}$	Differential Input Capacitance	V_{TxD} = High; (Note 11)	−	3.75	10	pF
THERMAL SHUTDOWN						
T_{JSD}	Shutdown Junction Temperature	Junction temperature rising	160	180	200	°C
T_{JSD_HYST}	Shutdown Junction Temperature Hysteresis		2.0	3.5	6.0	°C
TIMING CHARACTERISTICS (see Figure 18)						
$t_{d(TxD-BUSon)}$	Propagation Delay TxD to Bus Active	Normal mode (Note 12, Figure 16)	−	75	−	ns
$t_{d(TxD-BUSoff)}$	Propagation Delay TxD to Bus Inactive	Normal mode (Note 12, Figure 16)	−	85	−	ns
$t_{d(BUSon-RxD)}$	Propagation Delay Bus Active to RxD	Normal or Silent mode (Note 12, Figure 16)	−	25	−	ns
$t_{d(BUSoff-RxD)}$	Propagation Delay Bus Inactive to RxD	Normal or Silent mode (Note 12, Figure 16)	−	35	−	ns
t_{pd_dr}	Propagation Delay TxD to RxD Dominant to Recessive Transition	Normal mode (Note 12, Figure 17) $t_{bit(TxD)}$ = 200 ns / 500 ns / 1000 ns	50	100	170	ns
t_{pd_rd}	Propagation Delay TxD to RxD Recessive to Dominant Transition	Normal mode (Note 12, Figure 17) $t_{bit(TxD)}$ = 200 ns / 500 ns / 1000 ns	50	120	170	ns
$t_{dom(TxD)}$	TxD Dominant Timeout	Normal mode; V_{TxD} = Low	1.2	2.4	6.0	ms
$t_{en(TxD)}$	Transmitter Activation Time after Clearing TxD Dominant Timeout Flag Condition	Normal mode	7.0	−	50	μs
$t_{dom(BUS)}$	Bus Dominant Timeout	Normal or Silent mode; bus dominant	1.5	2.8	6.5	ms
$t_{en(RxD)}$	Receiver Activation Time after Clearing Bus Dominant Timeout Flag Condition	Normal or Silent mode	14	−	50	μs
$t_{bit(RxD)}$	Bit Time on RxD Pin	$t_{bit(TxD)}$ = 500 ns (Note 12, Figure 17)	400	−	550	ns
		$t_{bit(TxD)}$ = 200 ns (Note 12, Figure 17)	120	−	220	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see Figure 18)						
$t_{bit(Vi(diff))}$	Bit Time on Bus Pins (CANH − CANL)	$t_{bit(TxD)}$ = 500 ns (Note 12, Figure 17)	435	−	530	ns
		$t_{bit(TxD)}$ = 200 ns (Note 12, Figure 17)	155	−	210	ns
Δt_{rec}	Receiver Timing Symmetry $\Delta t_{rec} = t_{bit(RxD)} - t_{bit(Vi(diff))}$	$t_{bit(TxD)}$ = 500 ns (Note 12, Figure 17)	−65	−	+40	ns
		$t_{bit(TxD)}$ = 200 ns (Note 12, Figure 17)	−45	−	+15	ns
$t_{d(startup)}$	Power−on Event Device Sartup Time	$V_B > V_{uvr\_VB}$ to Standby Mode Delay (Figure 5)	−	−	100	μs
$t_{d(mode)}$	Operating Mode Change Delay	Mode change by STBN/EN pins (Figure 7 and Figure 8)	7.0	16	50	μs
$t_{d(mode\_wake)}$		Mode change after local wake−up (Figure 12 and Figure 13)	10	16	38	μs
$t_{d(mode\_wup)}$		Mode change after remote wake−up (Figure 14)	10	22	63	μs
$t_{h(mode)}$	Operating Mode Change Hold Time	Figure 7 and Figure 8	3.0	−	50	μs
$t_{h(go-to-sleep)}$	Go−to−Sleep Mode Entering Hold Time	STBN = Low, EN = High (Figure 9)	3.0	−	50	μs
$t_{d(wake\_startup)}$	Power−on Event WAKE Pin Enable Time	Standby mode to WAKE input enable delay (Power−on event only) (Figure 5)	40	70	200	μs
t_{wake_filt}	WAKE Pin Input Filter Time	Standby or Sleep mode (Figure 12 and Figure 13)	5.0	21	60	μs
$t_{d(wake\_flg)}$	Wake−up Flag Set Delay Time	Local wake−up detected, Standby or Sleep mode (Figure 12 and Figure 13)	3.0	5.5	13	μs
t_{wup_filt}	Bus Wake−up Pattern Filter Time (Short)	Standby or Sleep mode (Figure 14)	0.15	−	1.8	μs
t_{wup_to}	Bus Wake−up Pattern Timeout	Standby or Sleep mode (Figure 14)	1.0	2.0	5.0	ms
$t_{d(wup\_flg)}$	Wake−up Flag Set Delay Time	Remote wake−up detected, Standby or Sleep mode (Figure 14)	3.0	11	38	μs
t_{uv_det}	Transmitter Deactivation Time after V_{CC} or V_{IO} Undervoltage Condition Detection	$V_{CC} < V_{uvd\_VCC}$ or $V_{IO} < V_{uvd\_VIO}$ (Figure 6)	−	0.7	−	μs
t_{uv_rec}	Transmitter Activation Time after V_{CC} and V_{IO} Undervoltage Condition Removal	$V_{CC} > V_{uvr\_VCC}$ and $V_{IO} > V_{uvr\_VIO}$ (Figure 6)	14	25	75	μs
t_{uvd_VCC}	V_{CC} Undervoltage Detection Timeout	$V_{CC} < V_{uvd\_VCC}$ to V_{CC} UV flag set	100	160	400	ms
t_{uvd_VIO}	V_{IO} Undervoltage Detection Timeout	$V_{IO} < V_{uvd\_VIO}$ to V_{IO} UV flag set	100	160	400	ms
t_{uvr_VCC}	V_{CC} Undervoltage Recovery Timeout	$V_{CC} > V_{uvr\_VCC}$ to V_{CC} UV flag reset	0.35	0.6	1.3	ms
t_{uvr_VIO}	V_{IO} Undervoltage Recovery Timeout	$V_{IO} > V_{uvr\_VIO}$ to V_{IO} UV flag reset	0.35	0.6	1.3	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Values based on design and characterization, not tested in production.
12. C_{LT} = 100 pF, C_{ST} not present, C_{RxD} = 15 pF

FUNCTIONAL DESCRIPTION

POWER SUPPLY

NCV7343 implements three power supply inputs – battery supply input V_B, CAN transceiver supply input V_{CC} and digital IOs supply input V_{IO}.

V_B Supply Pin

V_B is the main supply pin of the NCV7343. The NCV7343 proceeds from Power−off mode to Standby mode as soon as the V_B supply is available. This supply input is used to provide the minimum power required for the operation in case of absence of the remaining supplies. Typically this is the only active supply in a low−power Sleep mode providing power supply to the low−power wake−up detector.

V_{CC} Supply Pin

V_{CC} pin is the CAN transceiver main supply input in Normal and Silent mode.

V_{IO} Supply Pin

Digital pins interfacing with the microcontroller have a separate IO supply. The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the IO levels between microcontroller and transceiver are properly adjusted. See Figure 1.

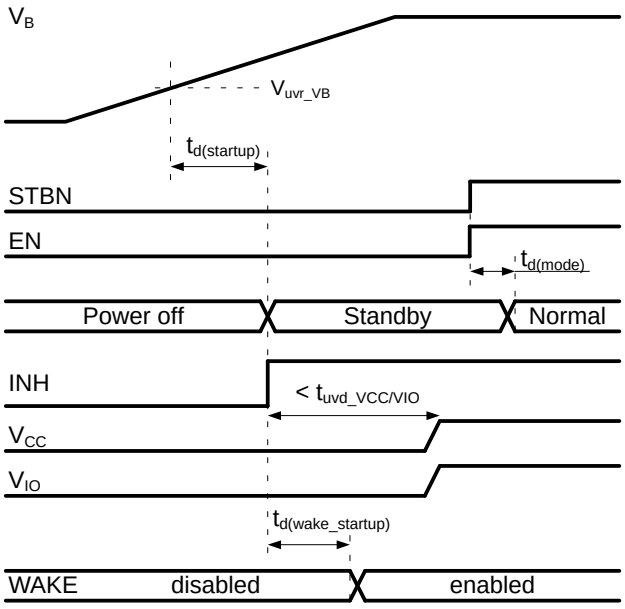


Figure 5. Typical Power−up Sequence

Power Supplies Monitoring

V_B, V_{CC} and V_{IO} supply inputs are monitored by undervoltage detectors with individual thresholds and filtering times both for undervoltage detection and undervoltage recovery.

In Normal mode, the transmitter is disabled t_{uv_det} after V_{CC} or V_{IO} voltage falls below respective undervoltage detection thresholds. The transmitter is re−enabled t_{uv_rec} after both V_{CC} and V_{IO} voltage rises above the undervoltage recovery thresholds (Figure 6).

V_B undervoltage is detected if V_B supply voltage falls below undervoltage detection threshold, V_{uvd_VB}. V_B undervoltage recovery is detected if V_B supply voltage rises above the undervoltage recovery threshold, V_{uvr_VB}.

V_{CC} undervoltage flag is set if V_{CC} supply voltage is lower than V_{uv_VCC} for longer than V_{CC} undervoltage detection time t_{uvd_VCC}. V_{CC} undervoltage recovery is detected and the flag is reset if V_{CC} supply voltage is higher than V_{uv_VCC} for longer than V_{CC} undervoltage recovery time t_{uvr_VCC}.

Similarly, V_{IO} undervoltage flag is set if V_{IO} supply voltage is lower than V_{uv_VIO} for longer than V_{IO} undervoltage detection time t_{uvd_VIO}. V_{IO} undervoltage recovery is detected and the flag is reset if V_{IO} supply voltage is higher than V_{uv_VIO} for longer than V_{IO} undervoltage recovery time t_{uvr_VIO}.

Both V_{CC} and V_{IO} undervoltage flags and the undervoltage detection timers are also reset after local or remote wake−up detection event or STBN pin rising edge detection in Sleep mode.

Once the V_{CC} and/or V_{IO} undervoltage flag is set the device changes to Sleep mode. The Sleep mode can be left and the operation mode control by STBN and EN pin is re−enabled as soon as both V_{CC} and V_{IO} supplies are recovered. The operating mode control state machine is not reset when an undervoltage condition is detected. Thus if Sleep mode was requested by the host prior to V_{CC} and/or V_{IO} undervoltage condition detection and the EN pin was set Low in Sleep mode, the device stays in Sleep once the undervoltage is recovered, although STBN and EN pins are both set Low, which is otherwise considered a Standby mode request.

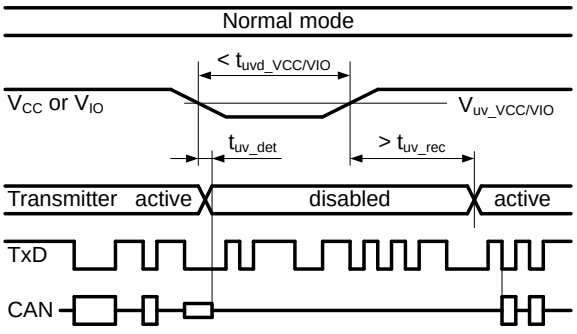


Figure 6. Transmitter Deactivation/Activation in Case of Undervoltage Event

INH Pin

The INH output pin is a high−voltage high−side switch to V_B supply. It can be used to control the V_{CC} or V_{IO} external supply voltage regulators. The output is switched high in all operating modes except for the Sleep mode. In Sleep mode the pin is left floating (high−impedance) which can be used to deactivate the external regulators in order to minimize the ECU current consumption. The INH switch is also deactivated in Power−off mode.

HIGH SPEED CAN TRANSCEIVER

NCV7343 implements high−speed physical layer CAN FD transceiver compatible with ISO11898−2:2016, implementing following optional features or alternatives:

- Extended bus load range
- Transmit dominant timeout, long
- Support of bit rates up to 5 Mbit/s
- Low−power modes with wake−up via wake−up pattern, Short CAN activity filter time and long wake−up timeout
- Normal Bus biasing

OPERATIONS MODES

NCV7343 provides five operation modes. These modes are either selectable through pins STBN and EN or entered automatically upon detection of specific event, such as power−on, undervoltage of wake−up (see Figure 11). Any mode transition is completed within a time given by operating mode change delay $t_{d(mode)}$.

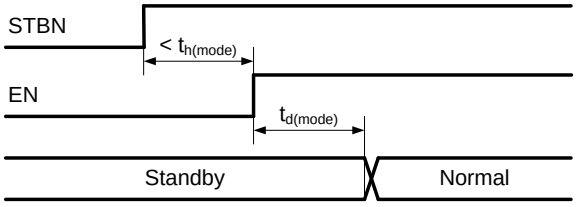


Figure 7. Operating Mode Transition Timing

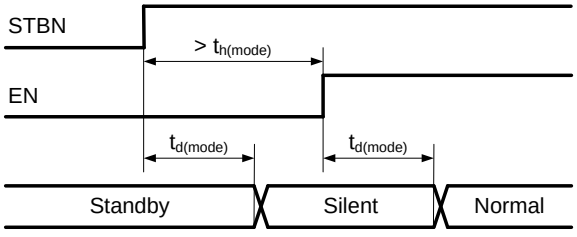


Figure 8. Operating Mode Transition Timing

Power−off

This virtual mode is entered as soon as the V_B voltage falls below the battery undervoltage detection threshold V_{uvd_VB} and a V_B undervoltage condition is detected. The internal logic is reset. The transceiver and wake−up detection is disabled, CAN bus pins are left floating and the INH pin is deactivated. The RxD pin is left High at V_{IO} level. As soon as the V_B voltage rises above battery undervoltage recovery threshold V_{uvr_VB}, the device proceeds to Standby mode.

Standby Mode

Standby mode is a low−power mode. In Standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are biased to ground and supply current is reduced to a minimum.

A wake−up event can be detected either on the CAN bus or on the WAKE pin. A valid wake−up is signaled on pins ERRN and RxD. Pin INH remains active (pulled high) so that the external regulators controlled by the INH pin remain switched on.

Standby mode is entered automatically upon Power−on event ($V_B > V_{uvr\_VB}$). It can be requested during normal operation by setting STBN and EN pins to Low. Standby mode is also entered if wake−up event is detected in Sleep mode or if V_{CC} and V_{IO} recovers after undervoltage condition has been detected.

Normal Mode

In the Normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

The bus lines (CANH and CANL) are internally biased to $V_{CC}/2$.

Pin INH is active (pulled high) so that the external regulators controlled by INH pin are switched on.

Normal mode can be requested by setting STBN and EN pin to High.

Silent Mode

In Silent mode, the CAN transmitter is disabled.

The CAN controller can still receive data from the bus via RxD Pin as the receiver part remains active. Equally to Normal mode, the bus lines (CANH and CANL) are internally biased to $V_{CC}/2$. Pin INH is also active (pulled high).

Silent mode can be requested by setting STBN to High and EN pin to Low.

Go−to−Sleep Mode

Go−to−sleep mode is an intermediate state used to put the transceiver into Sleep mode in a controlled way.

Go−to−sleep mode is entered when EN is set to High and STBN pin is set to Low. If the logical state of pins EN and STBN is kept unchanged for a minimum period of $t_{h(go-to-sleep)}$ and neither a wake−up nor a power−up event occur during this time, the transceiver enters Sleep mode.

While in Go−to−sleep mode, the transceiver behaves identically to Standby mode.

Sleep Mode

Sleep mode is a low−power mode in which the consumption is further reduced compared to Standby mode. Sleep mode can be entered via Go−to−sleep mode or is forced in case an undervoltage on either V_{CC} and/or V_{IO} occurs for longer than the undervoltage detection time.

The transceiver behaves identically to Standby mode, but the INH Pin is deactivated (left floating) and the external regulators controlled by INH pin are switched off. In this way, the V_B consumption is reduced to a minimum.

The device will leave sleep mode either after a wake−up event (in case of a CAN bus wake−up or wake−up via WAKE pin) or by changing STBN pin from Low to High (as long as an undervoltage on V_{IO} is not detected).

In case the Sleep mode was forced due to undervoltage detection, the device enters Standby mode and the operation mode control by STBN and EN pin is re−enabled as soon as both V_{CC} and V_{IO} supplies are recovered.

In case the Sleep mode was requested by the host, any potential V_{CC} and/or V_{IO} undervoltage detection and subsequent undervoltage recovery does not lead to any mode change and the device stays in Sleep mode until the mode change via STBN is requested by the host or a valid wake−up is detected.

Operating Modes Transition

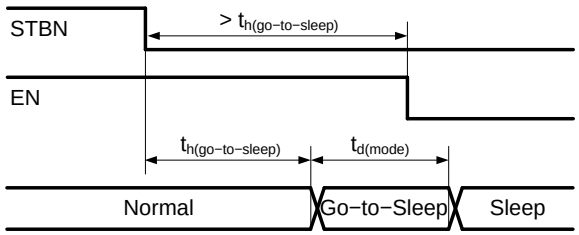


Figure 9. Correct Sleep Mode Entry Sequence

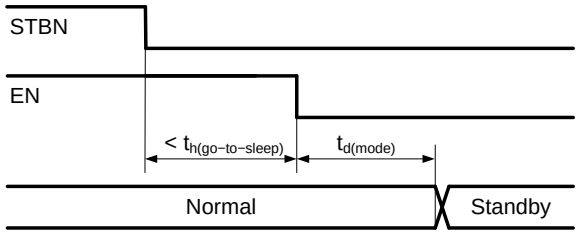
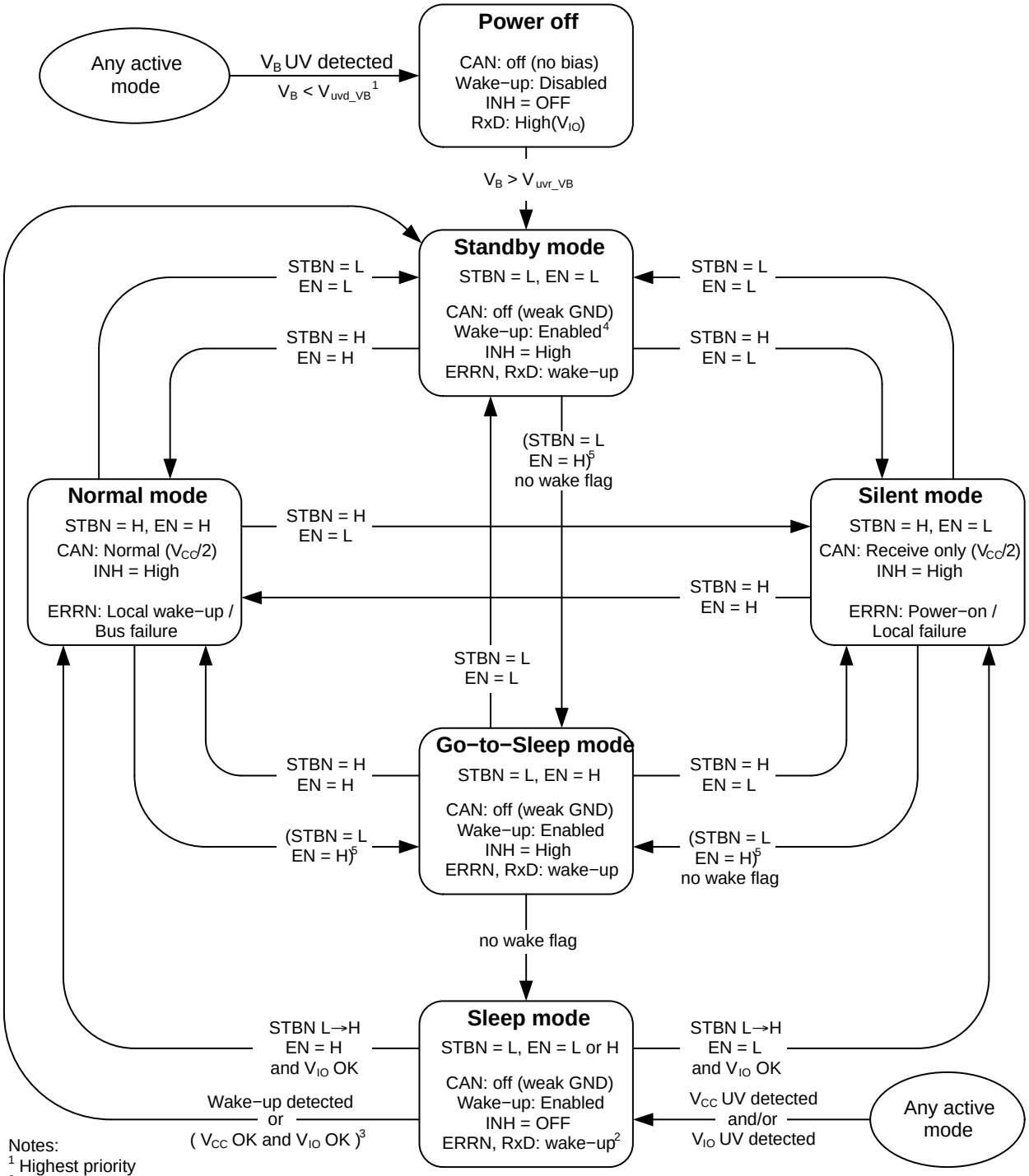


Figure 10. Sleep Mode Entry Sequence Interrupted



Notes:
[1] Highest priority
[2] If V_{IO} is active
[3] In case Sleep mode was requested by host command V_{CC} /V_{IO} undervoltage recovery event does not lead to mode change
[4] Upon Power−on event, Local wake−up detection is enabled after $t_{d(wake\_startup)}$
[5] For t > $t_{h(go-to-sleep)}$

V_{CC} UV detected:	$V_{CC} < V_{uv\_VCC}$	for t > t_{uvd_VCC};	V_{IO} UV detected:	$V_{IO} < V_{uv\_VIO}$	for t > t_{uvd_VIO}
V_{CC} OK:	$V_{CC} > V_{uv\_VCC}$	for t > t_{uvr_VCC} ;	V_{IO} OK:	$V_{IO} > V_{uv\_VIO}$	for t > t_{uvr_VIO}

Figure 11. Operation Modes

WAKE−UP

A Wake−up flag is set if Local wake−up via WAKE pin (positive or negative edge) is detected or Remote wake−up via bus (wake−up pattern) is detected. If the Wake−up flag is set in Sleep mode, the device changes to Standby mode. Undervoltage detection flags are cleared and the corresponding timers are restarted upon detection of valid wake−up event.

The Wake−up flag is cleared when entering Normal mode or when V_{CC} or V_{IO} undervoltage is detected.

Wake−up flag is signaled on ERRN and RxD pin in Standby, Go−to−sleep and Sleep mode provided the V_{IO} supply voltage is available.

Local Wake−up (WAKE pin)

The high−voltage input WAKE is monitored in Low−power Standby mode, Go−to−Sleep and Sleep mode. If a negative or positive edge is recognized on WAKE pin, a local wake−up is detected and a Wake−up flag is set. In order to avoid false wake−ups, the negative or positive edge must be followed by stable Low or High level, respectively, longer than t_{wake_filt} for the wake−up to be valid. The WAKE pin can be used, for example, for switch or contact monitoring.

Internal pull−up and pull−down current sources are connected to WAKE pin in order to minimize the risk of parasitic toggling. The current source polarity is automatically selected based on the WAKE input signal polarity – when the voltage on WAKE stays stable High (Low) for longer than t_{wake_filt}, the internal current source is switched to pull−up (pull−down).

Negative edge detection is depicted in Figure 12. Positive edge detection is depicted in Figure 13.

Besides, in order to be able to distinguish between local and remote wake−up events, a Wake−up source indication flag is set if local wake−up is detected. Wake−up source indication flag is reset upon Normal mode leaving. Wake−up source indication flag is signaled on ERRN pin in Normal mode, before first four consecutive dominant symbols are sent.

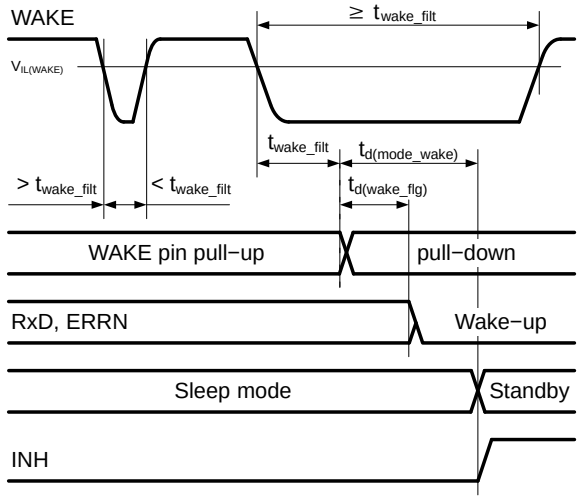


Figure 12. Local Wake−up Behavior (Negative Edge)

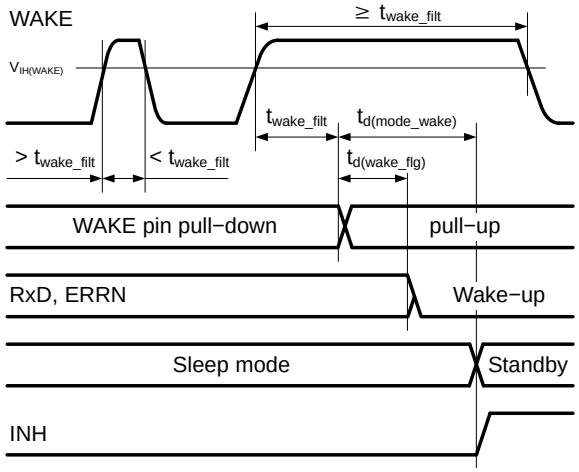


Figure 13. Local Wake−up Behavior (Positive Edge)

Remote Wake−up (Wake−up pattern)

When a valid wake−up pattern (phase in order dominant – recessive – dominant) is detected during the Standby, Go−to−Sleep or Sleep mode a Wake−up flag is set. Minimum length of each phase is t_{wup_filt} − see Figure 14.

Pattern must be received within t_{wup_to} to be recognized as valid wake−up otherwise internal logic is reset.

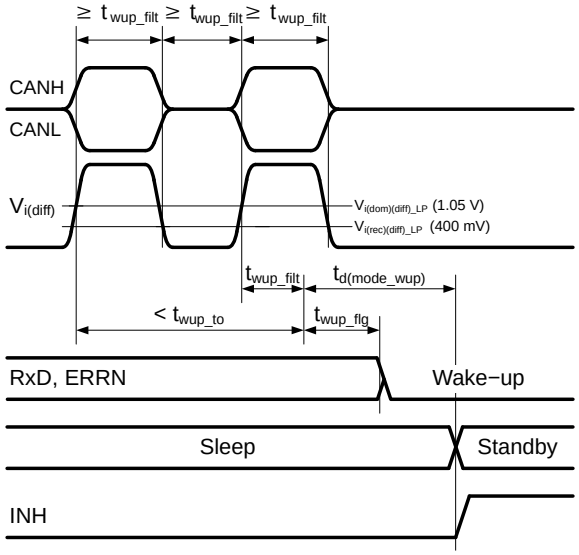


Figure 14. Remote Wake−up Behavior (Wake−up Pattern)

FAILURE DETECTION

Local Failures

A Local failure flag is set if any of the flowing flags are set:

- TxD Dominant Timeout
- Bus Dominant Timeout
- Short−TxD to RxD
- Overtemperature Detection

The local failure flag is signaled on ERRN pin in Silent mode entered from Normal mode. The flag is cleared if all of the mentioned flags are cleared.

TxD Dominant Timeout

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state if pin TxD is forced permanently low. The timer is triggered by a negative edge on pin TxD in Normal mode. If the duration of the Low level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the TxD dominant timeout flag is set. The transmitter is disabled, driving the bus into a recessive state, as long as the TxD dominant flag is set.

The timer and the flag is reset when TxD is High and either Normal mode is entered or bus dominant is received in Normal mode. The transmitter is reactivated latest $t_{en(TxD)}$ after TxD dominant flag has been cleared.

The minimum value of TxD dominant timeout time $t_{dom(TxD)}$ limits the minimum bit rate to 17 kbps.

Bus Dominant Timeout

Bus dominant timeout timer is started when CAN bus changes from recessive to dominant state. If the dominant state on the bus is kept for longer time than $t_{dom(BUS)}$, the RxD pin is released to High level and a Bus dominant timeout flag is set. No other action is taken upon Bus dominant timeout condition detection. The timer and the flag is reset when CAN bus changes back from dominant to recessive state in Normal or Silent mode, or when low−power mode is entered. The receiver is reactivated latest $t_{en(RxD)}$ after Bus dominant flag has been cleared.

This feature prevents potential bus dominant clamping condition from blocking the communication controller transmit task.

Short – TxD to RxD

If a short between TxD and RxD signal lines is detected during data transmission. Short TxD to RxD flag is set and the transmitter is disabled.

The transmitter can be re−enabled when either Normal mode is entered or bus dominant symbol is received on the bus, driving RxD Low, while TxD is High.

Overtemperature Detection

An overtemperature flag is set if the junction temperature exceeds a shutdown temperature T_{JSD}. The thermal protection circuit protects the IC from damage by switching off the transmitter if the overtemperature is detected. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is expected to be reduced once the transmitter is disabled. All other IC functions continue to operate.

The overtemperature flag is reset when the junction temperature decreases below the thermal shutdown threshold and either Normal mode is entered or bus dominant symbol is received on the bus while TxD is High.

The transmitter can be re−enabled when the flag is cleared.

The thermal protection circuit is particularly needed in case of a bus line short circuit.

CAN Bus Failure Flag

The transmitter of the NCV7343 device allows for bus failure detection. During dominant bit transmission in Normal mode, a short of the CANH or CANL line to supply or ground (V_B, V_{CC} or GND) is internally detected. If the short circuit condition lasts for four consecutive TxD dominant symbol requests, an internal bus failure flag is set. Minimum dominant symbol length for correct bus failure detection is 4 μs. The flag is visible on ERRN pin in Normal mode. The transmission and reception circuitry continues to function.

The bus failure flag is reset when Normal mode is entered or if four consecutive TxD dominant symbols are sent while no bus short circuit condition is present.

INTERNAL FLAGS AND THEIR SIGNALING

The transceiver keeps several internal flags reflecting conditions and events encountered during its operation. Some flags influence the transceiver operation mode. Beside the undervoltage flags all others can be read by the host microcontroller on pin ERRN. Pin ERRN signals internal flags depending on the operation mode of the transceiver. An overview of the flags and their visibility on pin ERRN is given in following table. Because the ERRN pin uses negative logic, it will be pulled low if the corresponding signaled flag is set and will be pulled high if the signaled flag is reset.

INTERNAL FLAGS AND THEIR VISIBILITY

Internal Flag	Set Conditions	Reset Conditions	Visibility on ERRN Pin
V_{CC} or V_{IO} Undervoltage	$V_{CC} < V_{uv\_VCC}$ for $t > t_{uvd\_VCC}$ or $V_{IO} < V_{uv\_VIO}$ for $t > t_{uvd\_VIO}$	($V_{CC} > V_{uv\_VCC}$ for $t > t_{uvr\_VCC}$ and $V_{IO} > V_{uv\_VIO}$ for $t > t_{uvr\_VIO}$) or power−on flag is set or wake flag is set or STBN is changed to High	No
V_B Undervoltage	$V_B < V_{uvd\_VB}$	$V_B > V_{uvr\_VB}$	No
Power−on	$V_B > V_{uvr\_VB}$	Normal mode is entered	In Silent mode entered from other than Normal mode
Wake−up	Local or remote wake−up is detected	Normal mode is entered or V_{CC} and/or V_{IO} flag is set	In Standby, Go−to−sleep or Sleep mode (if V_{IO} is active)
Wake−up Source indication	Local wake−up is detected	Normal mode is left	In Normal mode before first four consecutive dominant symbols are sent
TxD Dominant Timeout	TxD is Low for longer than $t_{dom(TxD)}$ while in Normal operation mode	TxD is High and either Normal mode is entered or bus dominant is received (RxD Low) in Normal mode	See Local Failure flag
Bus Dominant Timeout	Bus is dominant for longer than $t_{dom(BUS)}$	Bus is recessive in Normal or Silent mode, or Low−power mode is entered	
TxD Shorted to RxD	TxD is shorted to RxD during data transmission	TxD is High and either Normal mode is entered or bus dominant is received (RxD Low)	
Overtemperature	Junction temperature $T_J > T_{JSD}$	Junction temperature $T_J < T_{JSD}$ and either Normal mode is entered or bus dominant is received while TxD is High	
Local Failure	Any of the following flags is set • TxD dominant timeout • Bus dominant timeout • TxD shorted to RxD • Overtemperature detection	All of the following flags are reset • TxD dominant timeout • Bus dominant timeout • TxD shorted to RxD • Overtemperature detection	In Silent mode entered from Normal mode
Bus Failure	Bus failure detected during four consecutive TxD dominant symbol requests	Normal mode is entered or four consecutive TxD dominant symbols sent while no bus failure condition present	In Normal mode after first four consecutive dominant symbols are sent

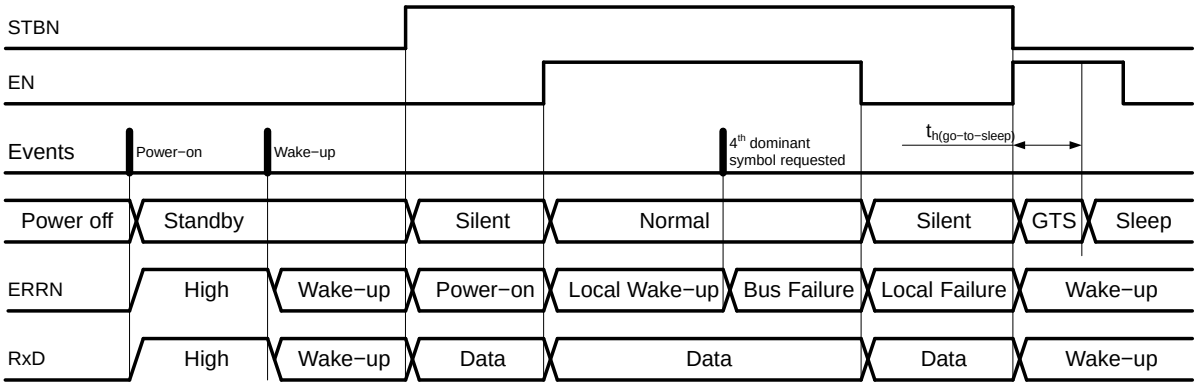


Figure 15. ERRN and RxD Pin Signaling

FAIL SAFE

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Undervoltage on supply pins prevents the chip from sending data on the bus when there is not enough V_{CC} supply voltage to build required bus differential voltage, or when V_{IO} supply voltage is low and thus the digital input or output signals might be interpreted falsely. After supply is recovered TxD pin must be first released to High to allow sending dominant bits again.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 19). Pin TxD is pulled high and pins STBN and EN are pulled low internally should the input become disconnected. Digital pins, TxD, STBN and EN will be floating, preventing reverse supply should the V_{IO} supply be removed. RxD and ERRN have forward diode to V_{IO} supply.

MEASUREMENT SETUPS AND DEFINITIONS

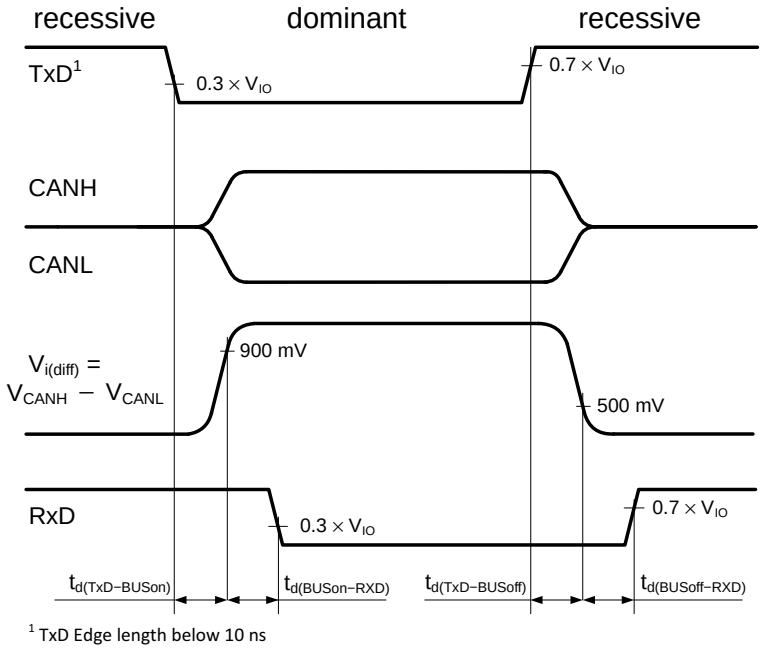


Figure 16. Transceiver Timing Diagram − Propagation Delays

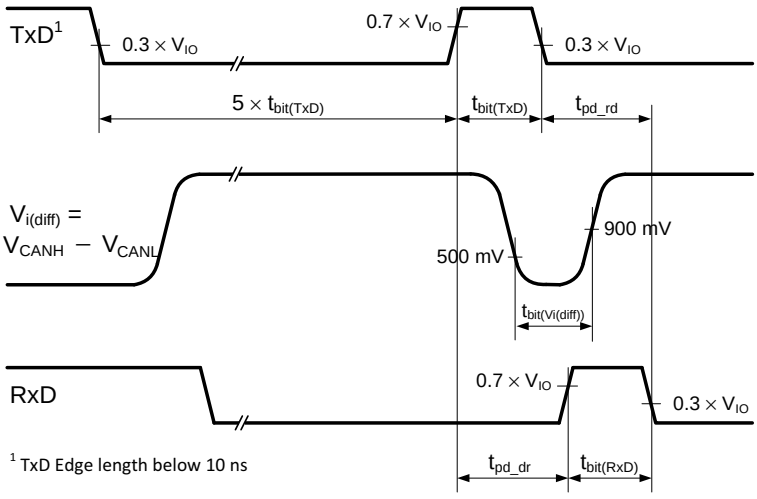


Figure 17. Transceiver Timing Diagram − Loop Delay and Recessive Bit Time

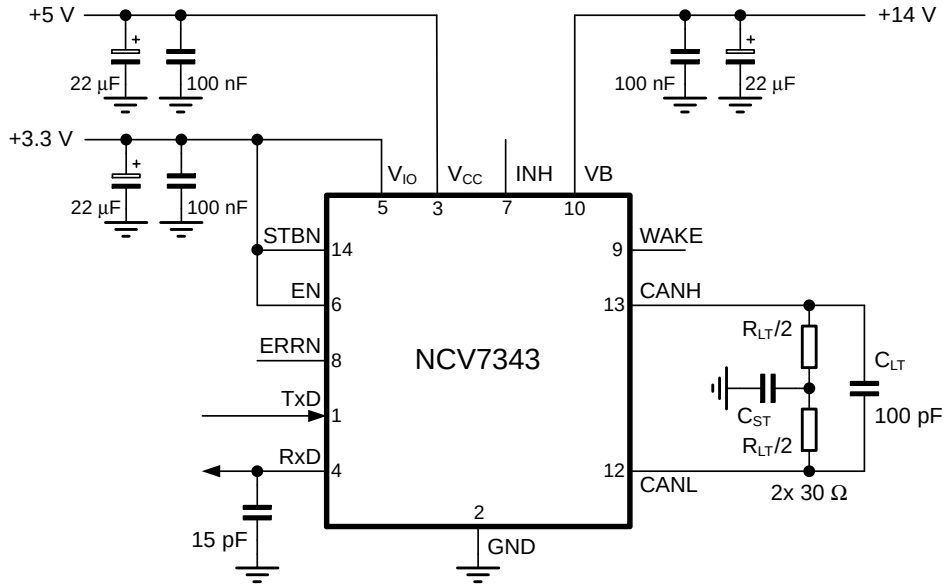


Figure 18. Test Circuit for Timing Characteristics

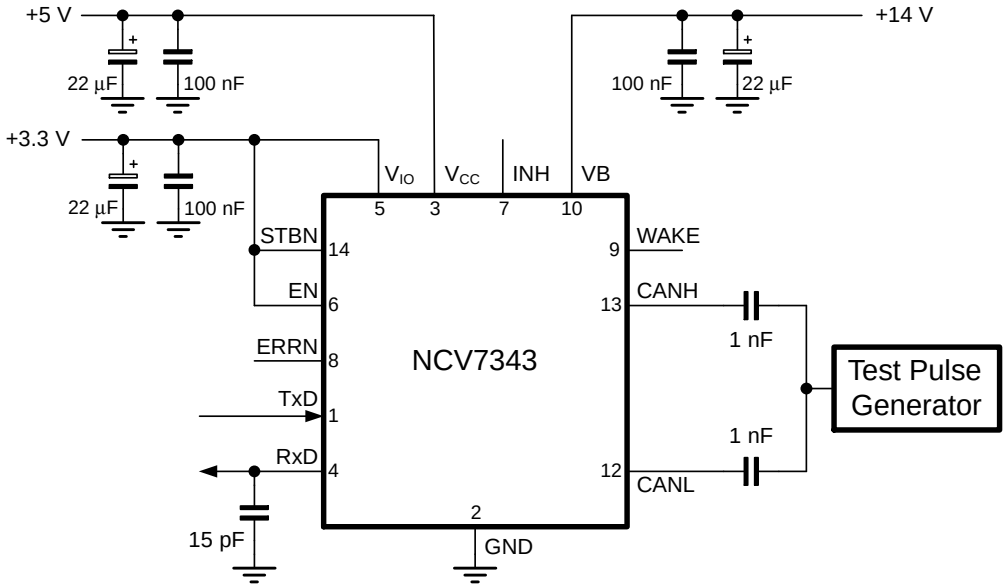


Figure 19. Test Circuit for Automotive Transients

ISO 11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7343 Datasheet
Parameter	**Notation**	**Symbol**
DOMINANT OUTPUT CHARACTERISTICS		
Single Ended Voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single Ended Voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential Voltage on Normal Bus Load	V_{Diff}	$V_{o(dom)(diff)}$
Differential Voltage on Effective Resistance During Arbitration	V_{Diff}	$V_{o(dom)(diff)\_ARB}$
Differential Voltage on Extended Bus Load Range	V_{Diff}	$V_{o(dom)(diff)\_E}$
DRIVER SYMMETRY		
Driver Symmetry	V_{SYM}	$V_{o(sym)}$
DRIVER OUTPUT CURRENT		
Absolute Current on CAN_H	I_{CAN_H}	$I_{o(SC)(CANH)}$
Absolute Current on CAN_L	I_{CAN_L}	$I_{o(SC)(CANL)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING ACTIVE		
Single Ended Output Voltage on CAN_H	V_{CAN_H}	$V_{o(rec)}$
Single Ended Output Voltage on CAN_L	V_{CAN_L}	$V_{o(rec)}$
Differential Output Voltage	V_{Diff}	$V_{o(rec)(diff)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING INACTIVE		
Single Ended Output Voltage on CAN_H	V_{CAN_H}	$V_{o(off)}$
Single Ended Output Voltage on CAN_L	V_{CAN_L}	$V_{o(off)}$
Differential Output Voltage	V_{Diff}	$V_{o(off)(diff)}$
TRANSMIT DOMINANT TIMEOUT		
Transmit Dominant Timeout	t_{dom}	$t_{dom(TxD)}$
Transmit Dominant Timeout, Short	t_{dom}	NA
STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING ACTIVE		
Recessive State Differential Input Voltage Range	V_{Diff}	$V_{i(rec)(diff)\_NM}$
Dominant State Differential Input Voltage Range	V_{Diff}	$V_{i(dom)(diff)\_NM}$
STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING INACTIVE		
Recessive State Differential Input Voltage Range	V_{Diff}	$V_{i(rec)(diff)\_LP}$
Dominant State Differential Input Voltage Range	V_{Diff}	$V_{i(dom)(diff)\_LP}$
RECEIVER INPUT RESISTANCE		
Differential Internal Resistance	R_{Diff}	$R_{i(diff)}$
Single Ended Internal Resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)}$
RECEIVER INPUT RESISTANCE MATCHING		
Matching of Internal Resistance	m_R	$R_{i(cm)(m)}$
LOOP DELAY REQUIREMENT		
Loop Delay	t_{Loop}	t_{pd_rd} t_{pd_dr}
DATA SIGNAL TIMING REQUIREMENTS FOR USE WITH BIT RATES ABOVE 1 Mbit/s AND UP TO 2 Mbit/s		
Transmitted Recessive Bit Width @ 2 Mbit/s	$t_{Bit(Bus)}$	$t_{bit(Vi(diff))}$
Received Recessive Bit Width @ 2 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RxD)}$
Receiver Timing Symmetry @ 2 Mbit/s	Δt_{Rec}	Δt_{rec}

ISO 11898−2:2016 PARAMETER CROSS−REFERENCE TABLE (continued)

Parameter	Notation	Symbol
DATA SIGNAL TIMING REQUIREMENTS FOR USE WITH BIT RATES ABOVE 2 Mbit/s AND UP TO 5 Mbit/s		
Transmitted Recessive Bit Width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{bit(Vi(diff))}$
Received Recessive Bit Width @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RxD)}$
Receiver Timing Symmetry @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}
MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{Diff}		
Maximum Rating V_{Diff}	V_{Diff}	V_{Diff}
General Maximum Rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CAN} V_{CAN}
Optional: Extended Maximum Rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
MAXIMUM LEAKAGE CURRENTS ON CAN_H and CAN_L, UNPOWERED		
Leakage Current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	$I_{LEAK(off)}$
BUS BIASING CONTROL TIMINGS		
CAN Activity Filter Time, Long	t_{Filter}	NA
CAN Activity Filter Time, Short	t_{Filter}	t_{wup_filt}
Wake−up Timeout, Short	t_{Wake}	NA
Wake−up Timeout, Long	t_{Wake}	t_{wup_to}
Timeout for Bus Inactivity (Required for Selective Wake−up Implementation Only)	$t_{Silence}$	NA
Bus Bias Reaction Time (Required for Selective Wake−up Implementation Only)	t_{Bias}	NA

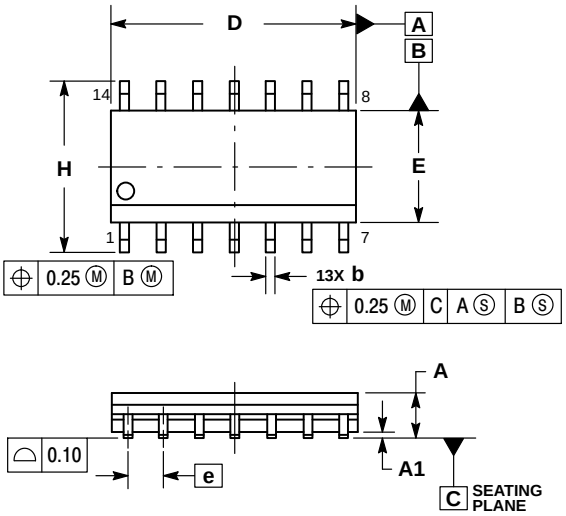
Table 1. ORDERING INFORMATION

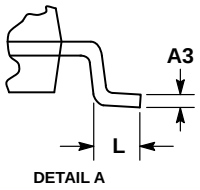
Part Number	Description	Package	Shipping†
NCV7343D20R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin	SOIC−14 (Pb−free)	3000 / Tape & Reel
NCV7343MW0R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin	DFNW14 Wettable Flank (Pb−free)	5000 / Tape & Reel
NCV7343D21R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin, EMC Improved	SOIC−14 (Pb−free)	3000 / Tape & Reel
NCV7343MW1R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin, EMC Improved	DFNW14 Wettable Flank (Pb−free)	5000 / Tape & Reel

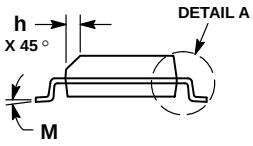
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L



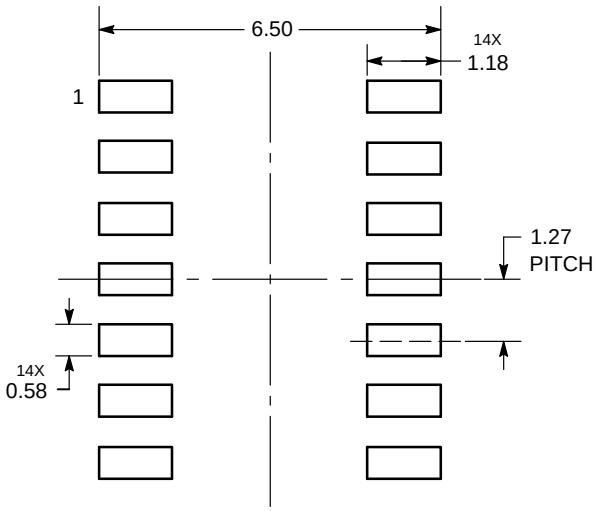




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*

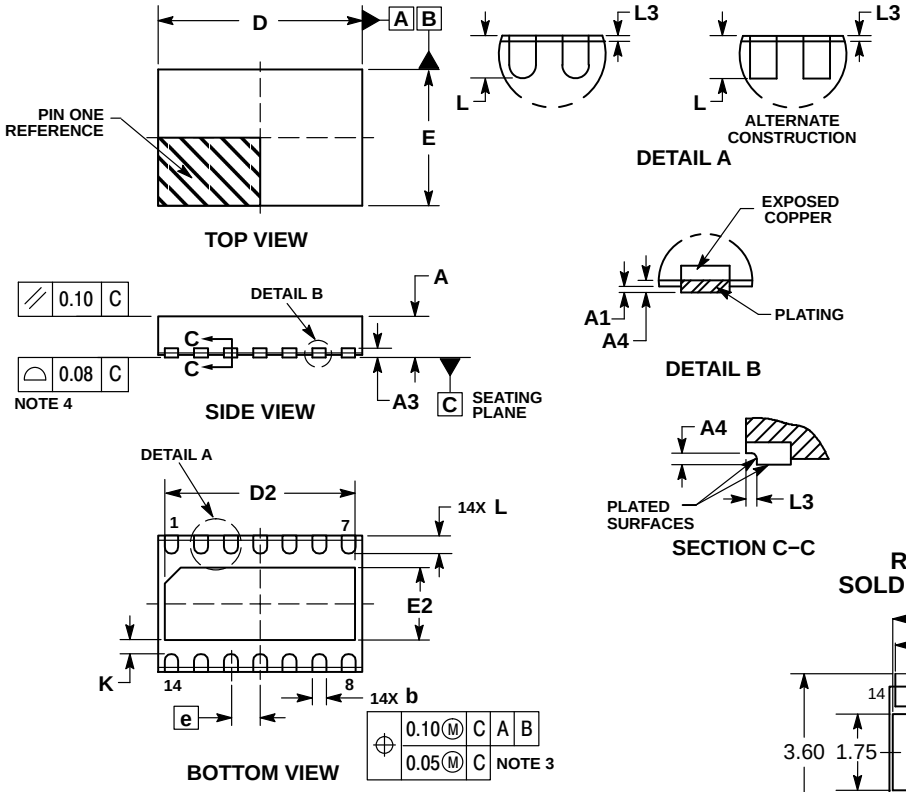


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

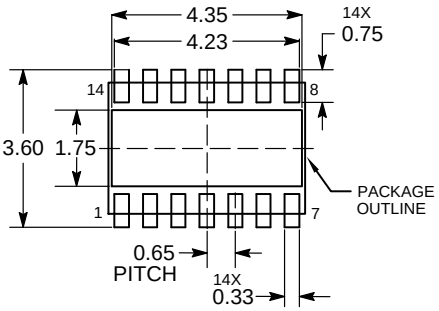
DFNW14 4.5x3, 0.65P
CASE 507AC
ISSUE D



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	4.40	4.50	4.60
D2	4.13	4.20	4.27
E	2.90	3.00	3.10
E2	1.53	1.60	1.67
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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