NCV7351, NCV7351F

High Speed CAN, CAN FD Transceiver

The NCV7351 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7351 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc. The NCV7351F is an addition to the family based on NCV7351 transceiver with improved bit timing symmetry behavior to cope with CAN flexible data rate requirements (CAN FD).

Due to the wide common−mode voltage range of the receiver inputs and other design features, the NCV7351 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Key Features

- Compatible with the ISO 11898−2 Standard
- High Speed (up to 1 Mbps)
- NCV7351F Version Has Specification for Loop Delay Symmetry (up to 2 Mbps according to ISO11898−2, up to 5 Mbps for information only)
- V_{IO} Pin on NCV7351(F)D13 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- EN Pin on NCV7351D1E Version Allowing Switching the Transceiver to a Very Low Current OFF Mode
- Excellent Electromagnetic Susceptibility (EMS) Level Over Full Frequency Range. Very Low Electromagnetic Emissions (EME) Low EME also Without Common Mode (CM) Choke
- Bus Pins Protected Against >15 kV System ESD Pulses
- Transmit Data (TxD) Dominant Time−out Function
- Under all Supply Conditions the Chip Behaves Predictably. No Disturbance of the Bus Lines with an Unpowered Node
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- Thermal Protection
- These are Pb−Free Devices

Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Automotive
- Industrial Networks

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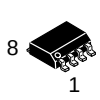
MARKING DIAGRAM



SOIC−8
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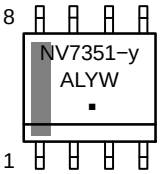
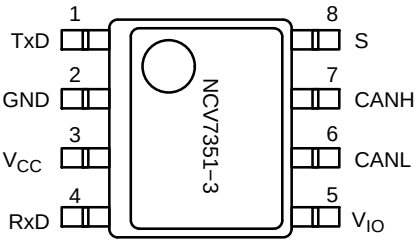
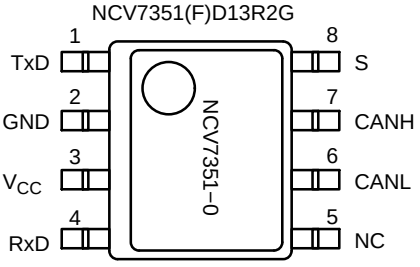


NV7351−y / NV7351Fy
y = 3, 0, or E
F = Flexible data rate version
(no dash used for CAN FD version)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

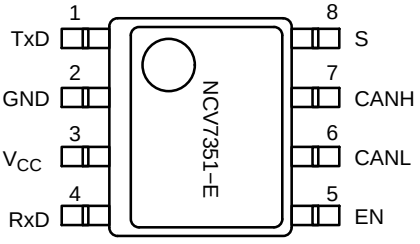
PIN ASSIGNMENT



NCV7351(F)D13R2G



NCV7351D10R2G



NCV7351D1ER2G

ORDERING INFORMATION

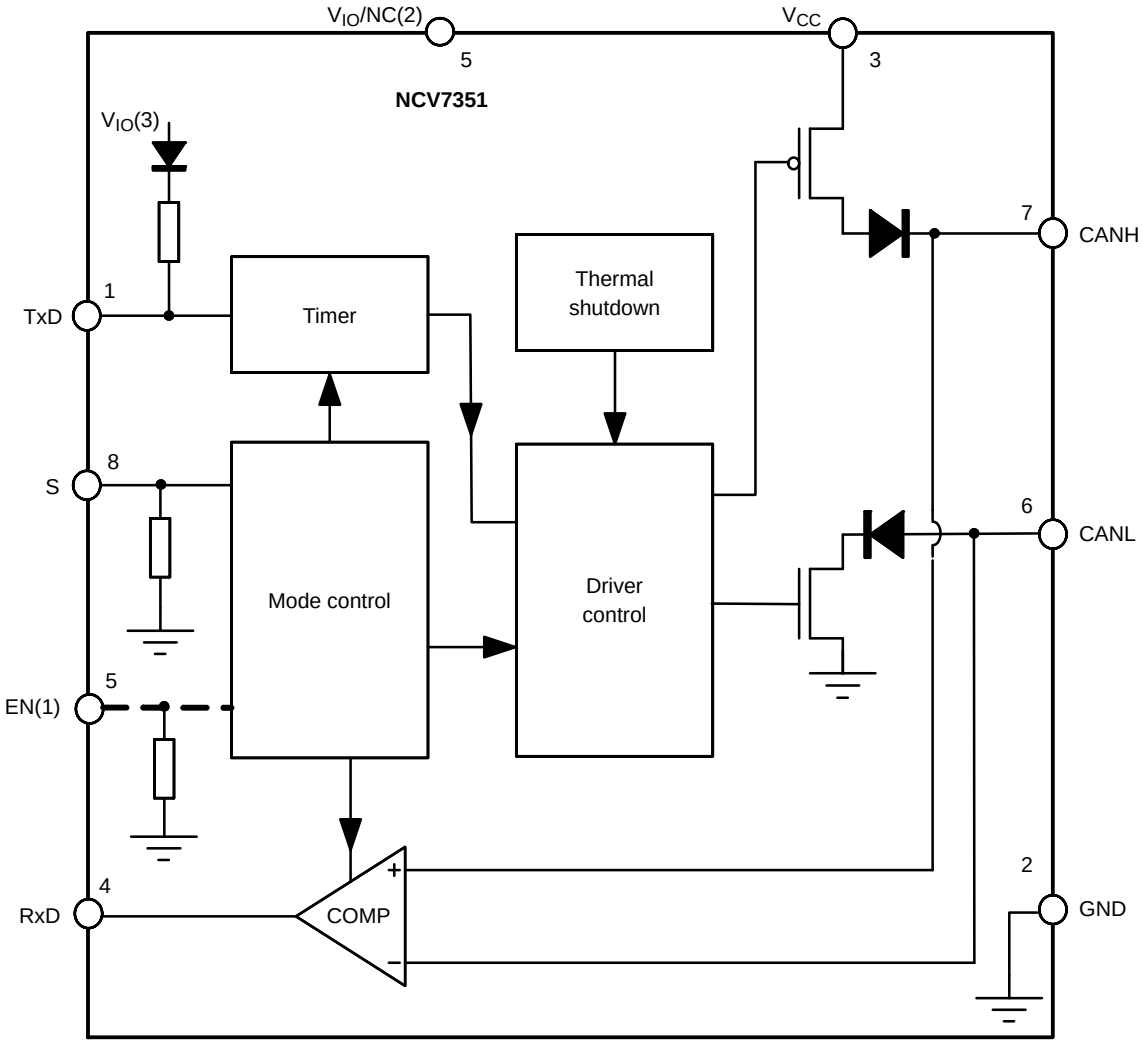
See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power supply voltage		4.5	5.5	V
V_{UV}	Undervoltage detection voltage on pin V_{CC}		3.5	4.5	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
$V_{CANH,L}$	DC voltage between CANH and CANL pin	$0 < V_{CC} < 5.5$ V	−50	+50	V
$V_{CANH,Lmax}$	DC voltage at pin CANH and CANL during load dump condition	$0 < V_{CC} < 5.5$ V, less than one second	−	+58	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000−4−2 at pins CANH and CANL	−15	+15	kV
$V_{O(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$45\ \Omega < R_{LT} < 65\ \Omega$	1.5	3	V
CM−range	Input common−mode range for comparator	Guaranteed differential receiver threshold and leakage current	−30	+35	V
I_{CC}	Supply current	Dominant; $V_{TxD} = 0$ V Recessive; $V_{TxD} = V_{CC}$	− 2.5	72 7.5	mA
I_{CCS}	Supply current in silent mode		1.4	3.5	mA
t_{pd}	Propagation delay TxD to RxD	See Figure 5	45	245	ns
T_J	Junction temperature		−40	+150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

BLOCK DIAGRAM



(1) Only present in the NCV7351D1E
(2) VIO for version NCV7351D13
NC for version NCV7351D10
(3) Internally connected to V_{CC} on versions without V_{IO} pin

Figure 1. Block Diagram of NCV7351

Table 2. NCV7351: PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Function
1	TxD	digital input, internal pull−up	Transmit data input; low input → dominant driver
2	GND	ground	Ground
3	V_{CC}	supply	Supply voltage
4	RxD	digital output	Receive data output; dominant bus → low output
5	NC	not connected	Not connected, NCV7351−0 version only
	V_{IO}	supply	Supply voltage for digital inputs/outputs, NCV7351−3 Version only
	EN	digital input, internal pull−down	Enable control input, NCV7351−E version only
6	CANL	high voltage input/output	Low−level CAN bus line (low in dominant mode)
7	CANH	high voltage input/output	High−level CAN bus line (high in dominant mode)
8	S	digital input, internal pull−down	Silent mode control input

APPLICATION INFORMATION

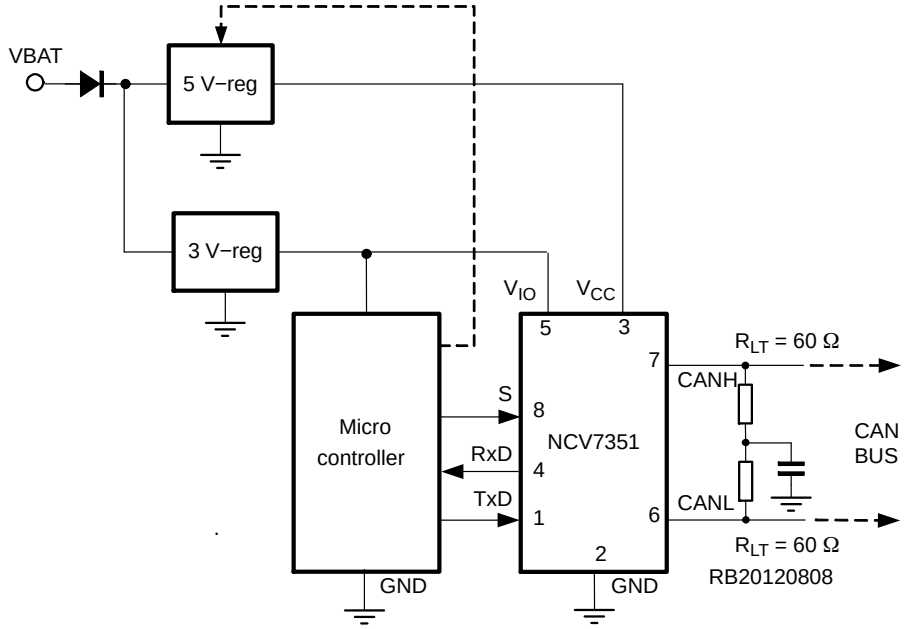


Figure 2. NCV7351−3 Application Diagram

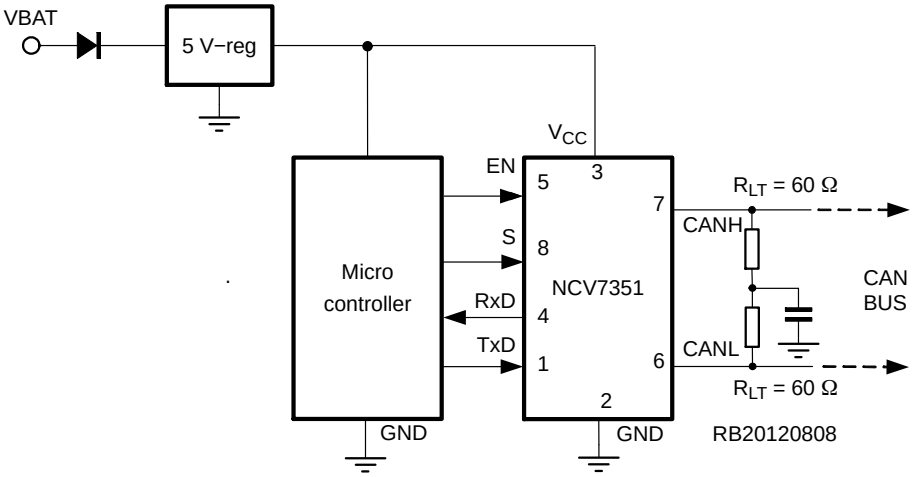


Figure 3. NCV7351−E Application diagram

FUNCTIONAL DESCRIPTION

NCV7351 has three versions which differ from each other only by function of pin 5. (See also Table 2) Devices marked with F (NCV7351F) are devices compliant to CAN flexible data rate timing specifications as detailed in electrical characteristics section. Except fulfilling these extra CAN FD requirements, all remaining specifications are equal to other devices from NCV7351 family. E.g. all specifications valid for NCV7351−3 versions are also valid for NCV7351F−3 version.

NCV7351−3: Pin 5 is V_{IO} pin, which is supply pin for transceiver digital inputs/output (supplying pins TxD, RxD, S, EN). The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. This allows in applications with microcontroller supply down to 3 V to easy communicate with the transceiver. (See Figure 2)

NCV7351−0: Pin 5 is not connected. This version is full replacement of the previous generation CAN transceiver AMIS30660.

NCV7351−E: Pin 5 is digital enable pin which allows transceiver to be switched off with very low supply current.

OPERATING MODES

The NCV7351 modes of operation are provided as illustrated in Table 3. These modes are selectable through pin S and also EN in case of NCV7351−E.

Table 3. OPERATING MODES

Mode	Pin S	Pin EN (Note 1)	Pin TxD	CANH,L Pins	RxD
Normal	0	1	0	Dominant	0
	0	1	1	Recessive	1
Silent	1	1	X	Recessive	1
	1	1	X	Dominant (Note 3)	0
Off (Note 1)	X	0	X	floating	floating

1. Only applicable to NCV7351−E
2. ‘X’ = don’t care
3. CAN bus driven to dominant by another transceiver on the bus

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

Silent Mode

In the silent mode, the transmitter is disabled. The bus pins are in recessive state independent of TxD input. Transceiver listens to the bus and provides data to controller, but controller is prevented from sending any data to the bus.

Off Mode

In Off mode, complete transceiver is disabled and consumes very low current. The CAN pins are floating not loading the CAN bus.

Over−temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 180°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed in case of the bus line short circuits.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value t_{dom}, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD. This TxD dominant time−out time ($t_{dom(TxD)}$) defines the minimum possible bit rate to 12 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; Figure 4). Internally, pin TxD is pulled high, pin EN and S low should the input become disconnected. Pins TxD, S, EN and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

Definitions: All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{sup}	Supply voltage V_{CC}		−0.3	+6	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{IOs}	DC voltage at pin TxD, RxD, S, EN, V_{IO}	Notes 4 and 5	−0.3	+6	V
V_{esd}	Electrostatic discharge voltage at all pins according to EIA−JESD22	Note 6	−6	+6	kV
	Electrostatic discharge voltage at CANH,CANL, pins according to EIA−JESD22	Note 6	−8	+8	kV
	Electrostatic discharge voltage at CANH, CANL pins According to IEC 61000−4−2	Note 7	−15	+15	kV
	Standardized charged device model ESD pulses according to ESD−STM5.3.1−1999		−750	+750	V
V_{schaff}	Transient voltage at CANH, CANL pins, See Figure 4	Note 8	−150	+100	V
Latch−up	Static latch−up at all pins	Note 9		+150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_J	Maximum junction temperature		−40	+170	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. EN pin Only available on NCV7351−E version
5. V_{IO} pin Only available on NCV7351−3 version
6. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
7. System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND. Verified by external test house
8. Pulses 1, 2a,3a and 3b according to ISO 7637 part 3. Results were verified by external test house.
9. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.

Table 5. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, 1S0P PCB (Note 10)	Free air	125	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, 2S2P PCB (Note 11)	Free air	75	K/W

10. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
11. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω unless specified otherwise.
On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Table 6. CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
I_{CC}	Supply current in normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	− 2.5	50 4.6	72 7.5	mA
I_{CCS}	Supply current in silent mode		1.4	2.3	3.5	mA
I_{CCOFF}	Supply current in OFF mode on NCV7351−E version only		−	7	18	μA
I_{CCOFF}	Supply current in OFF mode NCV7351−E version only	$T_J \leq 100°C$, Note 13	−	7	10	μA
V_{UVDVCC}	Undervoltage detection voltage on V_{CC} pin		3.5	4	4.5	V
SUPPLY (Pin V_{IO}) on NCV7351−3 Version Only						
$V_{iorange}$	Supply voltage range on pin V_{IO}		2.8	−	5.5	V
I_{IO}	Supply current on pin V_{IO} normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	100 50	240 125	500 265	μA
I_{IOS}	Supply current on pin V_{IO} silent mode	Bus is recessive; V_{TxD} = V_{IO}	−	2	16	μA
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		2.1	2.4	2.7	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage, on NCV7351−3 version only	Output recessive	0.7 x V_{IO}	−	V_{IO} + 0.3	V
V_{IH}	High−level input voltage, on NCV7351−0 and NCV7351−E versions only	Output recessive	2.5	−	V_{CC} + 0.3	V
V_{IL}	Low−level input voltage	Output dominant	−0.3	−	+0.3 x V_{IO}	V
R_{TxD}	TxD pin pull up		22	30	50	kΩ
C_i	Input capacitance	Note 13	−	5	10	pF
TRANSMITTER MODE SELECT (Pin S and EN)						
V_{IH}	High−level input voltage, on NCV7351−3 version only	Silent mode	0.7 x V_{IO}	−	V_{IO} + 0.3	V
V_{IH}	High−level input voltage on NCV7351−0 and NCV7351−E versions only	Silent or enable mode	2.5	−	V_{CC} + 0.3	V
V_{IL}	Low−level input voltage	Normal mode	−0.3	−	+0.3 x V_{IO}	V
$R_{S,EN}$	S and EN pin pull down	Note 12	0.55	1.1	1.5	MΩ
C_i	Input capacitance	Note 13	−	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level output current	Normal mode V_{RxD} = V_{IO} − 0.4 V	−1	−0.4	−0.1	mA
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1.5	6	11	mA
BUS LINES (Pins CANH and CANL)						

12. EN pin Only available on NCV7351−E version
13. Not tested in production. Guaranteed by design and prototype evaluation.
14. Only applicable for version NCV7351F

Table 6. CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(reces)}$ (norm)	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load normal mode	2.0	2.5	3.0	V
$I_{o(reces)}$ (CANH)	Recessive output current at pin CANH	−30 V < V_{CANH}< +35 V; 0 V < V_{CC} < 5.5 V	−2.5	−	+2.5	mA
$I_{o(reces)}$ (CANL)	Recessive output current at pin CANL	−30 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.5 V	−2.5	−	+2.5	mA
$I_{LI(CANH)}$	Input leakage current to pin CANH	0 Ω < R(V_{CC} to GND) < 1 MΩ $V_{CANL} = V_{CANH}$ = 5 V	−10	0	10	μA
$I_{LI(CANL)}$	Input leakage current to pin CANL		−10	0	10	μA
$V_{o(dom)}$ (CANH)	Dominant output voltage at pin CANH	V_{TxD} = 0 V; V_{CC} = 4.75 V to 5.25 V	3.0	3.6	4.25	V
$V_{o(dom)}$ (CANL)	Dominant output voltage at pin CANL	V_{TxD} = 0 V; V_{CC} = 4.75 V to 5.25 V	0.5	1.4	1.75	V
$V_{o(dif)}$ (bus_dom)	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; dominant; V_{CC} = 4.75 V to 5.25 V 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dif)}$ (bus_rec)	Differential bus output voltage (V_{CANH} − V_{CANL})	$V_{TxD} = V_{IO}$; recessive; no load	−120	0	+50	mV
$V_{o(sym)}$ (bus_dom)	Bus output voltage symmetry V_{CANH} + V_{CANL}	V_{TxD} = 0 V V_{CC} = 4.75 V to 5.25 V	0.9	−	1.1	V_{CC}
$I_{o(sc)}$ (CANH)	Short circuit output current at pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−90	−70	−40	mA
$I_{o(sc)}$ (CANL)	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	40	70	100	mA
$V_{i(dif)}$ (th)	Differential receiver threshold voltage	−12 V < V_{CANL} < +12 V; −12 V < V_{CANH} < +12 V;	0.5	0.7	0.9	V
$V_{ihcm(dif)}$ (th)	Differential receiver threshold voltage for high common−mode	−30 V < V_{CANL} < +35 V; −30 V < V_{CANH} < +35 V;	0.40	0.7	1.0	V
$R_{i(cm)}$ (CANH)	Common−mode input resistance at pin CANH		15	26	37	kΩ
$R_{i(cm)}$ (CANL)	Common−mode input resistance at pin CANL		15	26	37	kΩ
$R_{i(cm)}$ (m)	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$	−0.8	0	+0.8	%
$R_{i(dif)}$	Differential input resistance		25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = V_{IO}$; not tested	−	7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = V_{IO}$; not tested	−	7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	$V_{TxD} = V_{IO}$; not tested	−	3.75	10	pF
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	160	180	200	°C
TIMING CHARACTERISTICS (see Figures 5, 6 and 7)						
$t_{d(TxD−BUSon)}$	Delay TxD to bus active	C_i = 100 pF between CANH to CANL	−	75	−	ns
$t_{d(TxD−BUSoff)}$	Delay TxD to bus inactive	C_i = 100 pF between CANH to CANL	−	65	−	ns
$t_{d(BUSon−RxD)}$	Delay bus active to RxD	C_{rxd} = 15 pF	−	70	−	ns
$t_{d(BUSoff−RxD)}$	Delay bus inactive to RxD	C_{rxd} = 15 pF	−	70	−	ns
t_{pd}	Propagation delay TxD to RxD (both edges)	C_i = 100 pF between CANH to CANL, C_{rxd} = 15 pF	45	140	245	ns

12. EN pin Only available on NCV7351−E version
13. Not tested in production. Guaranteed by design and prototype evaluation.
14. Only applicable for version NCV7351F

Table 6. CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see Figures 5, 6 and 7)						
$t_{dom(TxD)}$	TxD dominant time for time−out	V_{TxD} = 0 V	1.5	2.5	5	ms
$t_{Bit2(Bus)}$	Transmitted recessive bit width, 2 Mbps	2 Mbps (500 ns TxD t_{bit}) 4.75 V < V_{CC} < 5.25 V Load: 60 Ω || 100 pF (Note 14)	435	−	530	ns
$t_{Bit2(RxD)}$	Received recessive bit width, 2 Mbps (RxD pin)		400	−	550	ns
$t_{Bit5(Bus)}$	Transmitted recessive bit width, 5 Mbps Info only	5 Mbps (200 ns TxD t_{bit}) 4.85 V < V_{CC} < 5.15 V −40°C < T_J < 105°C Load: 60 Ω || 100 pF (Note 14)	−	172	−	ns
$t_{Bit5(RxD)}$	Received recessive bit width, 5 Mbps (RxD pin) Info only		−	156	−	ns
Δt_{Rec2}	Receiver timing symmetry, intended for use up to 2 Mbps $\Delta t_{Rec2} = t_{Bit2(RxD)} - t_{Bit2(Bus)}$	Calculated parameter based on $t_{bit2(Bus)}$ and $t_{Bit2(RxD)}$ (Note 14)	−65	−	40	ns
Δt_{Rec5}	Receiver timing symmetry, intended for use up to 5 Mbps Info only $\Delta t_{Rec5} = t_{Bit5(RxD)} - t_{Bit5(Bus)}$	Calculated parameter based on $t_{bit5(Bus)}$ and $t_{Bit5(RxD)}$ (Note 14)	−	−16	−	ns

12. EN pin Only available on NCV7351−E version
13. Not tested in production. Guaranteed by design and prototype evaluation.
14. Only applicable for version NCV7351F

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MEASUREMENT SETUPS AND DEFINITIONS

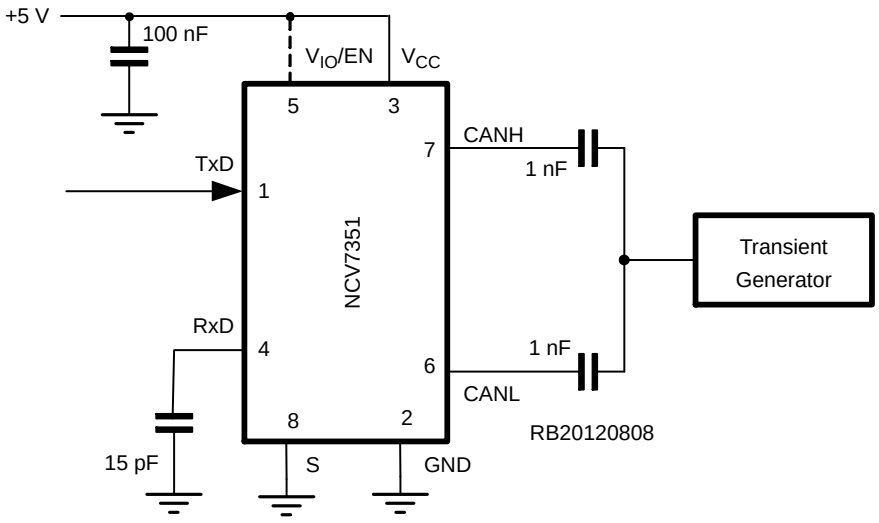


Figure 4. Test Circuit for Automotive Transients

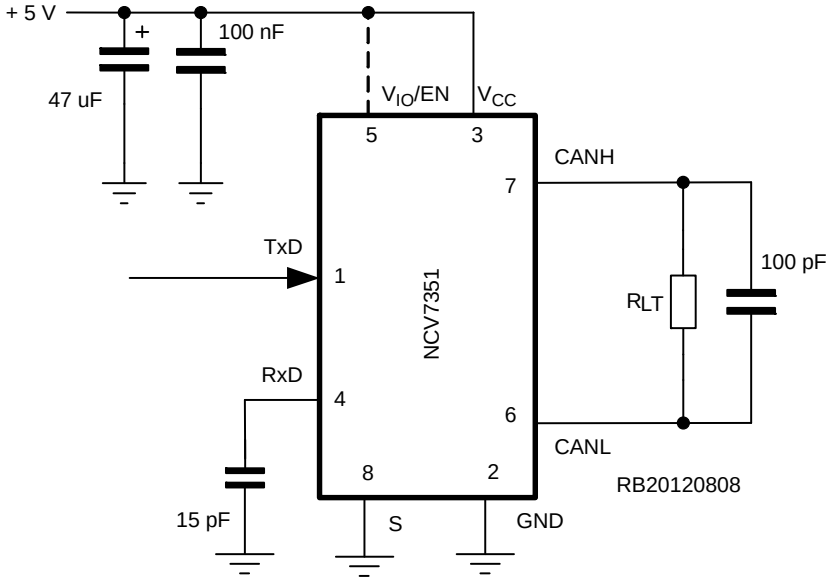


Figure 5. Test Circuit for Timing Characteristics

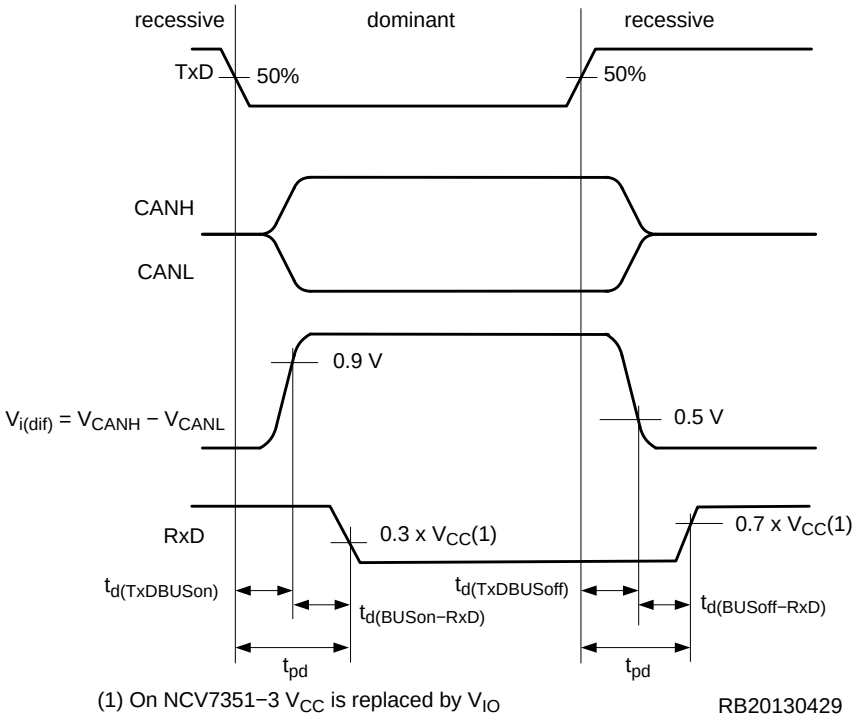


Figure 6. Transceiver Timing Diagram

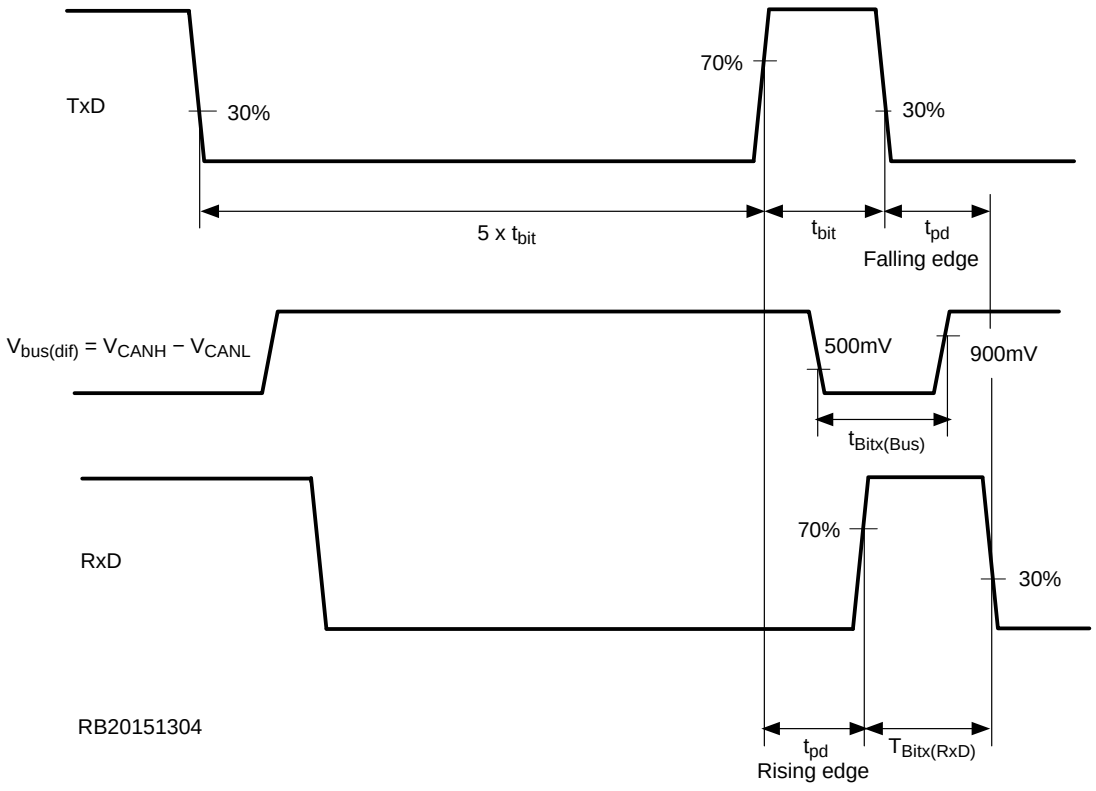


Figure 7. CAN FD Timing Diagram

DEVICE ORDERING INFORMATION

Part Number	Description	Marking	Temperature Range	Package	Shipping†
NCV7351D13R2G	High Speed CAN Transceiver with V_{IO} pin	NCV7351−3	−40°C to +125°C	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NCV7351FD13R2G	CAN FD Compliant High Speed CAN Transceiver with V_{IO} pin	NCV7351F			
NCV7351D10R2G	High Speed CAN Transceiver with pin 5 NC	NCV7351−0			
NCV7351D1ER2G	High Speed CAN Transceiver with EN pin	NCV7351−E			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

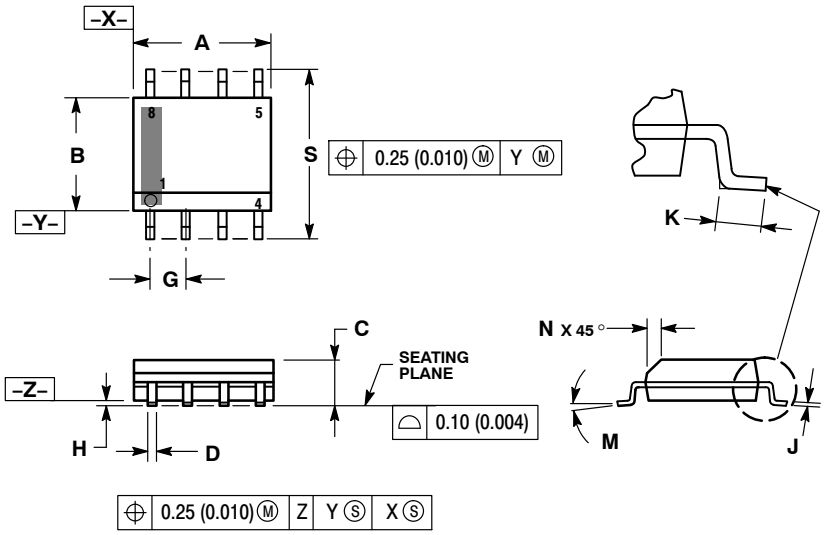
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

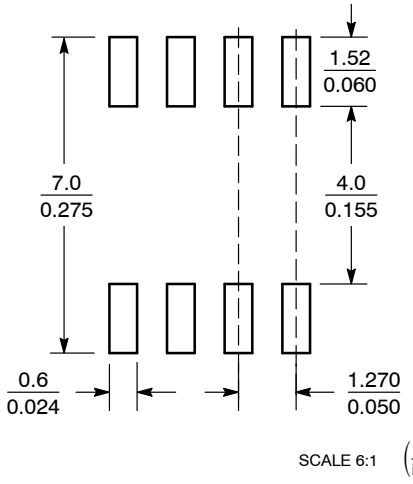
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

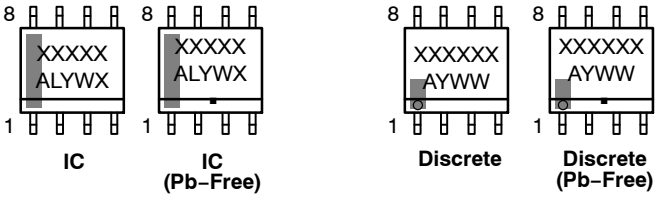
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

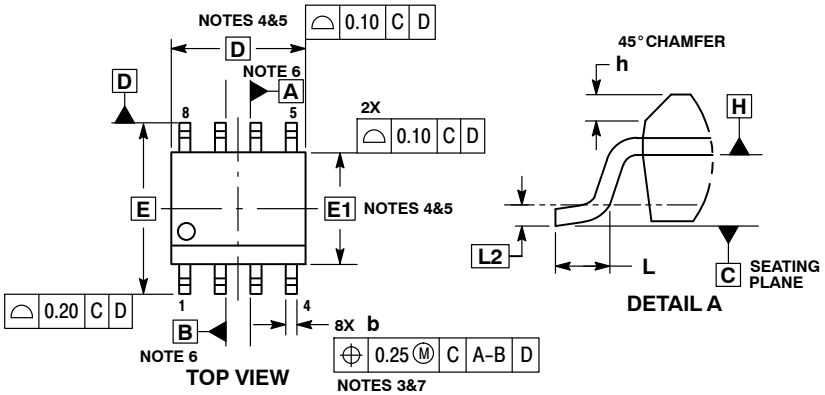
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

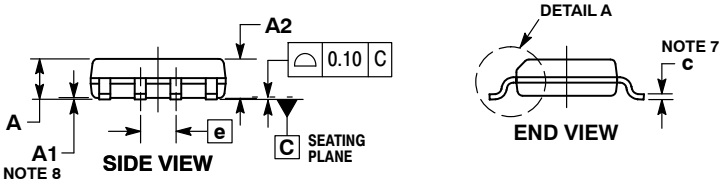
ON Semiconductor®

SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

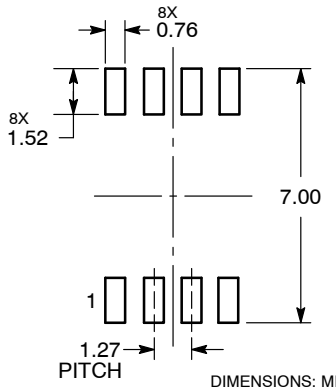




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

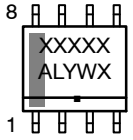
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**SOIC−8**	**PAGE 1 OF 1**

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