NCV7420

LIN Transceiver with 3.3 V or 5 V Voltage Regulator

General Description

The NCV7420 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus. The transceiver is implemented in I3T technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

The NCV7420 LIN device is a member of the in−vehicle networking (IVN) transceiver family of ON Semiconductor that integrates a LIN v2.0/2.1 physical transceiver and either a 3.3 V or a 5 V voltage regulator.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function. The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

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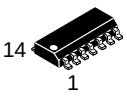
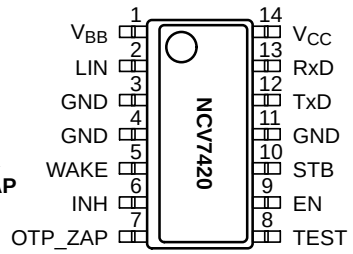


SOIC−14
D SUFFIX
CASE 751AP

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

KEY FEATURES

LIN−Bus Transceiver

- LIN compliant to specification revision 2.0 and 2.1 (backward compatible to version 1.3) and J2602
- I3T high voltage technology
- Bus voltage ±45 V
- Transmission rate up to 20 kBaud

Protection

- Thermal shutdown
- Indefinite short−circuit protection on pins LIN and WAKE towards supply and ground
- Load dump protection (45 V)
- Bus pins protected against transients in an automotive environment
- System ESD protection level for LIN, WAKE and V_{BB} up to ±12 kV

Voltage Regulator

- Output voltage 5 V / ~50 mA or 3.3 V / ~50 mA
- Wake−up input
- Enable inputs for standby and sleep mode
- INH output for auxiliary purposes (switching of an external pull−up or resistive divider towards battery, control of an external voltage regulator etc.)

EMI Compatibility

- Integrated slope control
- Meets most demanding EMS/EME requirements

Modes

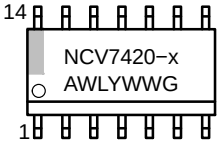
- Normal mode: LIN communication in either low (up to 10 kBaud) or normal slope
- Sleep mode: V_{CC} is switched “off” and no communication on LIN bus
- Standby mode: V_{CC} is switched “on” but there is no communication on LIN bus
- Wake−up bringing the component from sleep mode into standby mode is possible either by LIN command or digital input signal on WAKE pin. Wake−up from LIN bus can also be detected and flagged when the chip is already in standby mode.

Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Require−ments; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

May, 2015 − Rev. 9
Publication Order Number:
NCV7420/D

MARKING DIAGRAM



NCV7420 = Specific Device Code
−x = −3 = NCV7420D23G
−4 = NCV7420D24G
−5 = NCV7420D25G
−6 = NCV7420D26G
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

Table 1. KEY TECHNICAL CHARACTERISTICS − 3.3 V version

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Nominal battery operating voltage (Note 1)	5	12	26	V
	Load dump protection (Note 2)			45	
I_{BB_SLP}	Supply current in sleep mode			20	μA
V_{CC_OUT} (Note 4)	Regulated V_{CC} output, V_{CC} load 1 mA−30 mA	3.23	3.30	3.37	V
	Regulated V_{CC} output, V_{CC} load 0 mA−50 mA	3.19	3.30	3.41	
I_{OUT_MAX}	Maximum V_{CC} output current (Note 3)	50			mA
V_{WAKE}	Operating DC voltage on WAKE pin	0		V_{BB}	V
	Maximum rating voltage on WAKE pin	−45		45	
T_{JSD}	Junction thermal shutdown temperature	165		195	°C
T_J	Operating junction temperature	−40		+150	°C

Table 2. KEY TECHNICAL CHARACTERISTICS − 5 V version

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Nominal battery operating voltage (Note 1)	6	12	26	V
	Load dump protection			45	
I_{BB_SLP}	Supply current in sleep mode			20	μA
V_{CC_OUT} (Note 4)	Regulated V_{CC} output, V_{CC} load 1 mA−30 mA	4.9	5.0	5.1	V
	Regulated V_{CC} output, V_{CC} load 0 mA−50 mA	4.83	5.0	5.17	
I_{OUT_MAX}	Maximum V_{CC} output current (Note 3)	50			mA
V_{WAKE}	Operating DC voltage on WAKE pin	0		V_{BB}	V
	Maximum rating voltage on WAKE pin	−45		45	
T_{JSD}	Junction thermal shutdown temperature	165		195	°C
T_J	Operating junction temperature	−40		+150	°C

1. Below 5 V on V_{BB} in normal mode, the bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit.
2. The applied transients shall be in accordance with ISO 7637 part 1, test pulse 5. The device complies with functional class C; class A can be reached depending on the application and external conditions.
3. Thermal aspects of the entire end−application have to be taken into account in order to avoid thermal shutdown of NCV7420.
4. V_{CC} voltage regulator output must be properly decoupled by external capacitor of min. 8 μF with ESR < 1 Ω to ensure stability.

Table 3. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA1}$	Thermal resistance junction−to−ambient, 1S0P PCB (Note 5)	free air	140	K/W
$R_{\theta JA}2$	Thermal resistance junction−to−ambient, 2S2P PCB (Note 6)	free air	80	K/W

5. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 20% trace coverage
6. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 20% trace coverage

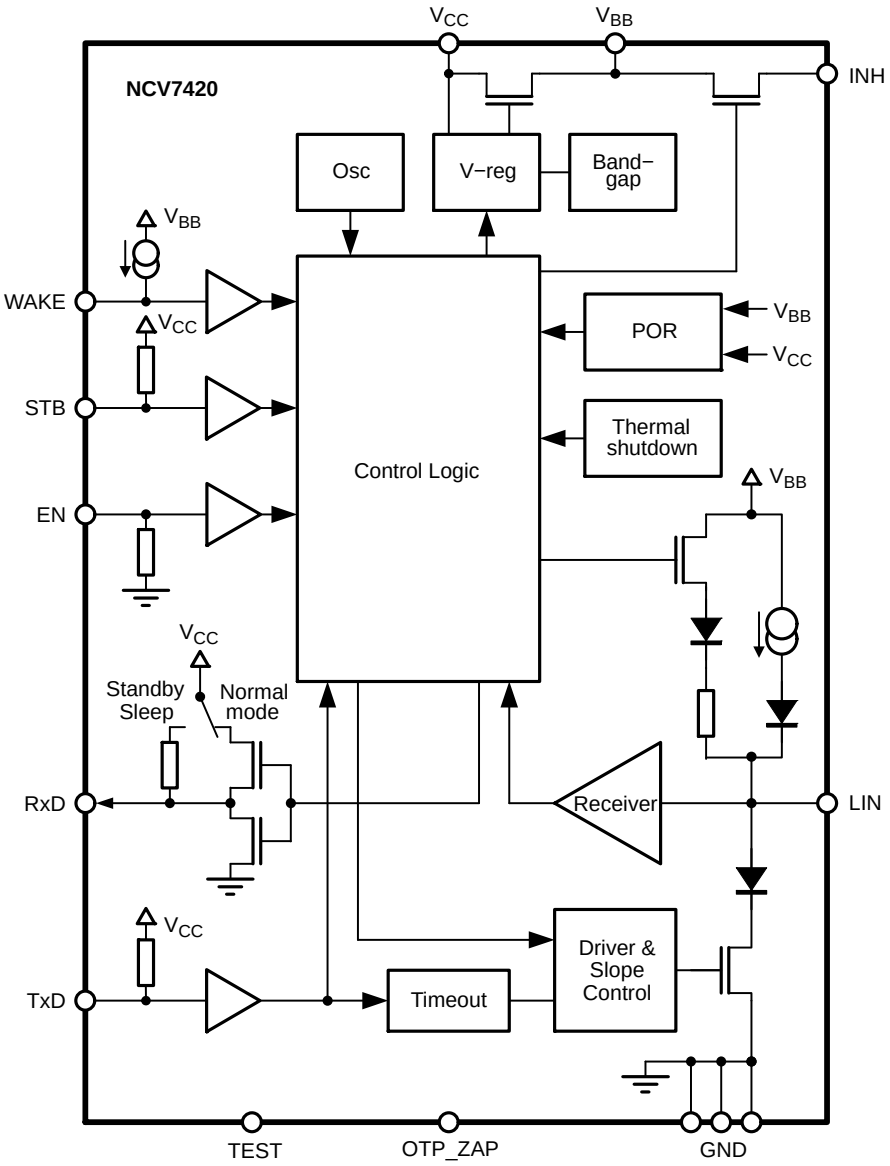


Figure 1. Block Diagram

Typical Application

Application Schematic

The EMC immunity of the Master−mode device can be further enhanced by adding a capacitor between the LIN output and ground. The optimum value of this capacitor is determined by the length and capacitance of the LIN bus, the number and capacitance of Slave devices, the pull−up resistance of all devices (Master & Slave), and the required time constant of the system, respectively.

V_{CC} voltage must be properly stabilized by external capacitor: capacitor of min. 8 μF (ESR < 1 Ω).

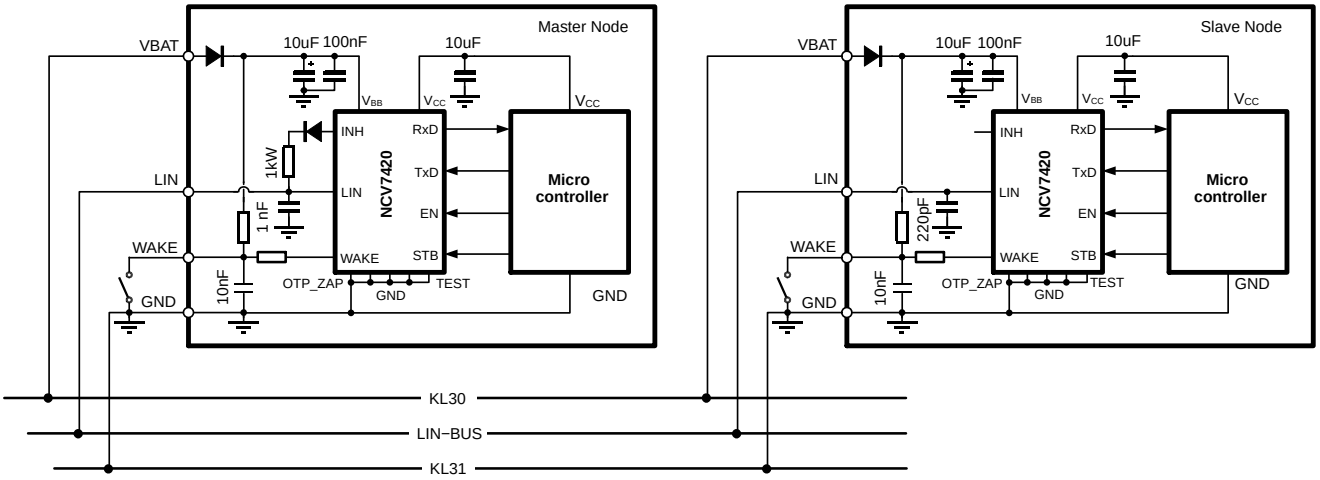


Figure 2. Typical Application Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	V_{BB}	Battery supply input
2	LIN	LIN bus output/input
3	GND	Ground
4	GND	Ground
5	WAKE	High voltage digital input pin to switch the part from sleep− to standby mode
6	INH	Inhibit output
7	OTP_ZAP	Supply for programming of trimming bits at factory testing, should be grounded in the application
8	TEST	Digital input for factory testing, should be grounded in the application
9	EN	Enable input, transceiver in normal operation mode when high
10	STB	Standby mode control input
11	GND	Ground
12	TxD	Transmit data input, low in dominant state
13	RxD	Receive data output; low in dominant state; push−pull output
14	V_{CC}	Supply voltage (output)

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class−A multiplex buses with a single master node and a set of slave nodes.

NCV7420 is designed as a master or slave node for the LIN communication interface with an integrated 3.3 V or 5 V voltage regulator having a current capability up to 50 mA for supplying any external components (microcontroller).

NCV7420 contains the LIN transmitter, LIN receiver, voltage regulator, power−on−reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for the maximum specified transmission speed of 20 kBaud with EMC performance due to reduced slew rate of the LIN output.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitter and voltage regulator off when temperature exceeds the TSD trigger level.

NCV7420 has four operating states (normal mode, low slope mode, standby mode, and sleep mode) that are determined by the input signals EN, WAKE, STB, and TxD.

Operating States

NCV7420 provides four operating states, two modes for normal operation with communication, one standby without communication and one low power mode with very low current consumption. See Figure 3.

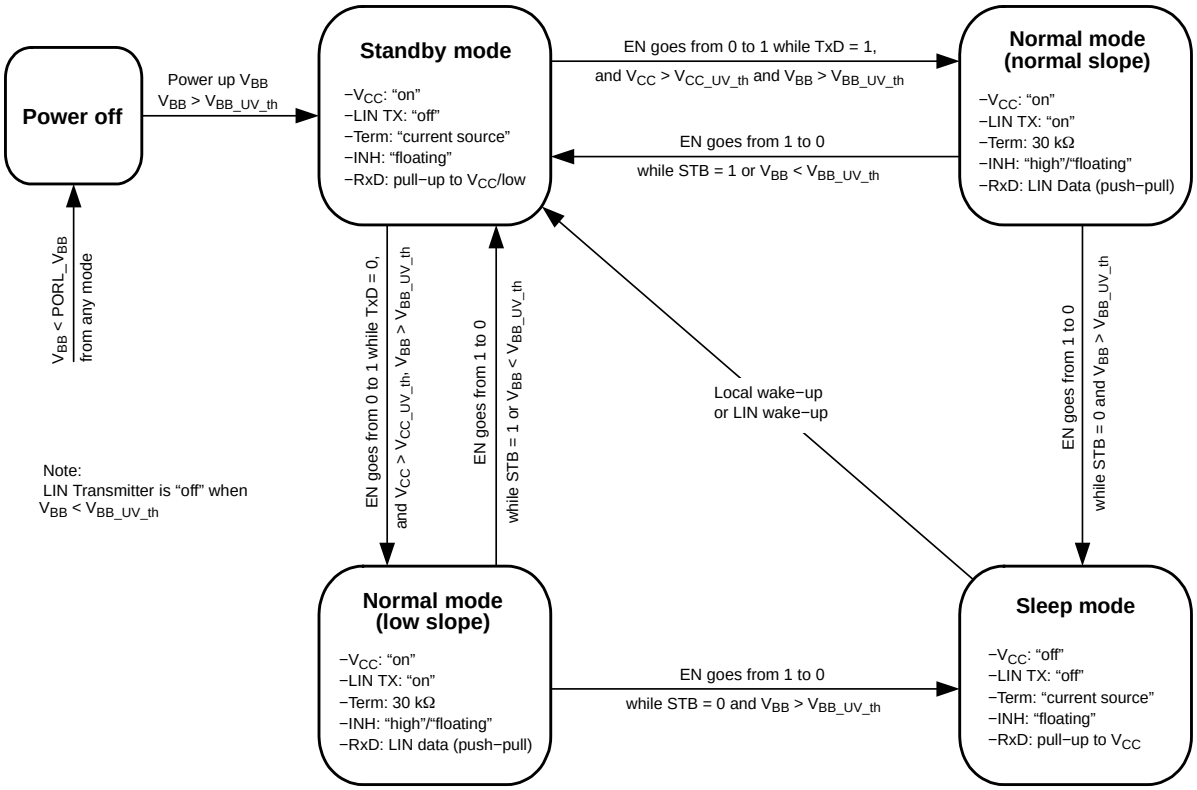


Figure 3. State Diagram

Table 5. MODE SELECTION

Mode	V_{CC}	RxD	INH	LIN	30 kΩ on LIN	Note
Normal − Slope	ON	Low = Dominant State High = Recessive State	High if STB=High during state transition; Floating otherwise	Normal Slope	ON	(Note 7)
Normal − Low Slope	ON	Low = Dominant State High = Recessive State	High if STB=High during state transition; Floating otherwise	Low Slope	ON	(Note 8)
Standby	ON	Low after LIN wake−up, high otherwise	Floating	OFF	OFF	(Notes 9 and 10)
Sleep	OFF	Clamped to V_{CC}	Floating	OFF	OFF	

7. The normal slope mode is entered when pin EN goes HIGH while TxD is in HIGH state during EN transition.
8. The low slope mode is entered when pin EN goes HIGH while TxD is in LOW state during EN transition. LIN transmitter gets on only after TxD returns to high after the state transition.
9. The standby mode is entered automatically after power−up.
10. In standby mode, RxD High state is achieved by internal pull-up resistor to V_{CC}.

Normal Slope Mode

In normal slope mode the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud. The transmit data stream of the LIN protocol is present on the TxD pin and converted by the transmitter into a LIN bus signal with controlled slew rate to minimize EMC emission. The receiver consists of the comparator that has a threshold with hysteresis in respect to the supply voltage and an input filter to remove bus noise. The LIN output is pulled HIGH via an internal 30 kΩ pull-up resistor. For master applications it is needed to put an external 1 kΩ resistor with a serial diode between LIN and V_{BB} (or INH). See Figure 2. The mode selection is done by EN=HIGH when TxD pin is HIGH. If STB pin is high during the standby-to-normal slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Low Slope Mode

In low slope mode the slew rate of the signal on the LIN bus is reduced (rising and falling edges of the LIN bus signal are longer). This further reduces the EMC emission. As a consequence the maximum speed on the LIN bus is reduced up to 10 kBaud. This mode is suited for applications where the communication speed is not critical. The mode selection is done by EN=HIGH when TxD pin is LOW. In order not to transmit immediately a dominant state on the bus (because

TxD=LOW), the LIN transmitter is enabled only after TxD returns to HIGH. If STB pin is high during the standby−to−low slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Standby Mode

The standby mode is always entered after power−up of the NCV7420. It can also be entered from normal mode when the EN pin is low and the standby pin is high. From sleep mode it can be entered after a local wake−up or LIN wake−up. In standby mode the V_{CC} voltage regulator for supplying external components (e.g. a microcontroller) stays active. Also the LIN receiver stays active to be able to detect a remote wake−up via bus. The LIN transmitter is disabled and the slave internal termination resistor of 30 kΩ between LIN and V_{BB} is disconnected in order to minimize current consumption. Only a pull−up current source between V_{BB} and LIN is active.

Sleep Mode

The Sleep Mode provides extreme low current consumption. This mode is entered when both EN and STB pins are LOW coming from normal mode. The internal termination resistor of 30 kΩ between LIN and V_{BB} is disconnected and also the V_{CC} regulator is switched off to minimize current consumption.

Wake−up

NCV7420 has two possibilities to wake−up from sleep or standby mode (see Figure 3):

- Local wake−up: enables the transition from sleep mode to standby mode
- Remote wake−up via LIN: enables the transition from sleep− to standby mode and can be also detected when already in standby mode.

A local wake−up is **only** detected in sleep mode if a transition from LOW to HIGH or from HIGH to LOW is seen on the WAKE pin.

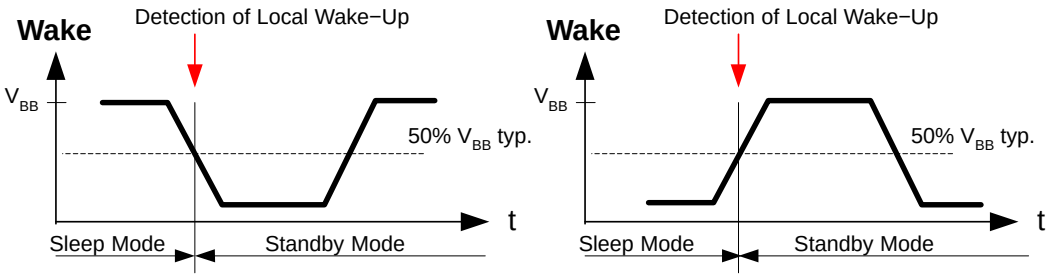


Figure 4. Local Wake−up Signal

A remote wake−up is **only** detected if a combination of (1) a falling edge at the LIN pin (transition from recessive to dominant) is followed by (2) a dominant level maintained for a time period > t_{WAKE} and (3) again a rising edge at pin LIN (transition from dominant to recessive) happens.

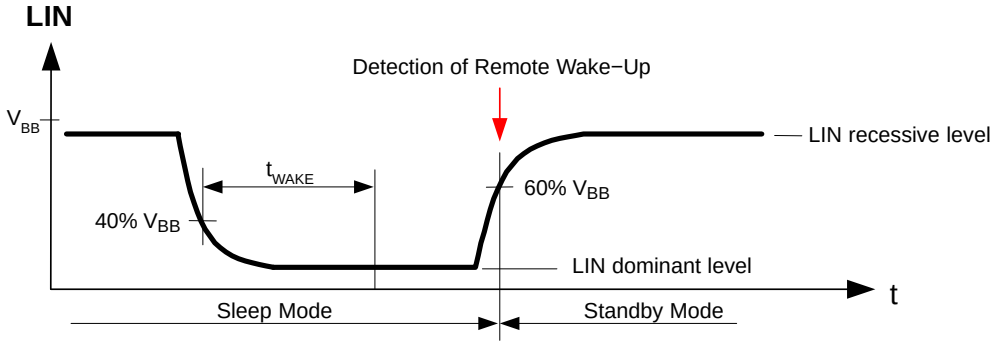


Figure 5. Remote Wake−up Behavior

The wake−up source is distinguished by pin RxD in the standby mode:

- RxD remains HIGH after power−up or local wake−up.
- RxD is kept LOW until normal mode is entered after a remote wake−up (LIN).

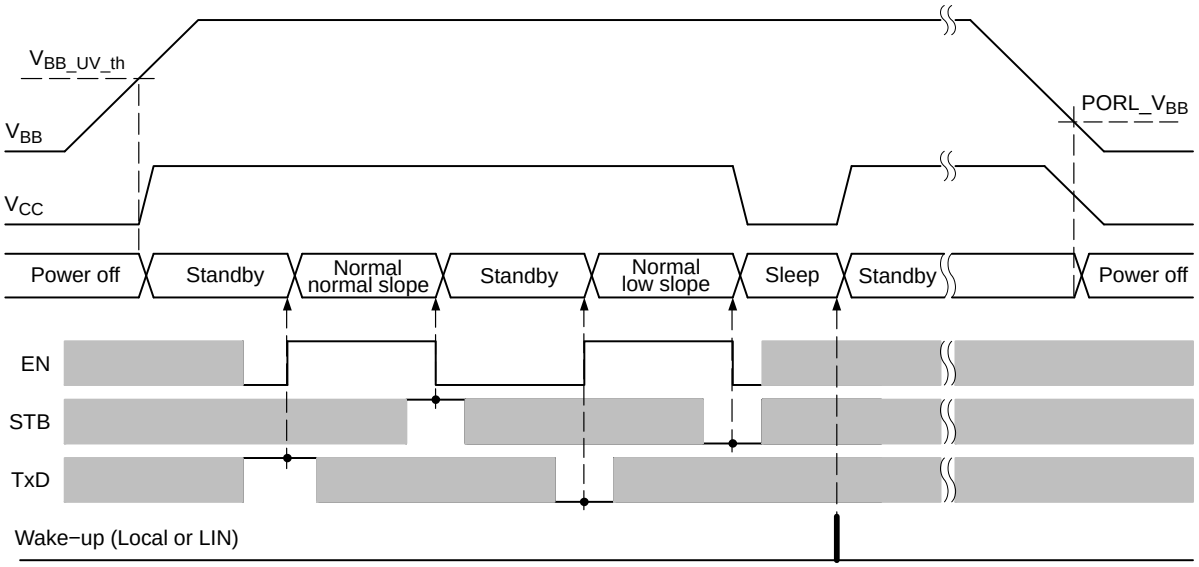


Figure 6. Operating Modes Transitions

Electrical Characteristics

Definitions

All voltages are referenced to GND (Pin 11). Positive currents flow into the IC.

Table 6. ABSOLUTE MAXIMUM RATINGS – 3.3 V and 5 V versions

Symbol	Parameter	Min	Max	Unit
V_{BB}	Battery voltage on pin V_{BB} (Note 11)	−0.3	+45	V
V_{CC}	DC voltage on pin V_{CC}	0	+7	V
I_{VCC}	Current delivered by the V_{CC} regulator	50		mA
V_{LIN}	LIN bus voltage (Note 12)	−45	+45	V
V_{INH}	DC voltage on inhibit pin	−0.3	V_{BB} + 0.3	V
V_{WAKE}	DC voltage on WAKE pin	−45	45	V
V_{DIG_IN}	DC input voltage on pins TxD, RxD, EN, STB	−0.3	V_{CC} + 0.3	V
T_J	Maximum junction temperature	−40	+165	°C
V_{ESD}	Electrostatic discharge voltage on all pins; HBM (Note 13)	−2	+2	kV
	Electrostatic discharge voltage on LIN, INH, WAKE and V_{BB} towards GND; HBM (Note 13)	−4	+4	kV
	Electrostatic discharge on LIN, WAKE and V_{BB}; system HBM (Note 14)	−8	+8	kV
	Electrostatic discharge voltage on all pins; CDM (Note 16)	−500	+500	V
V_{ESD} (EMC/ESD improved versions)	Electrostatic discharge voltage on all pins; HBM (Note 13)	−4	+4	kV
	Electrostatic discharge voltage on LIN, INH, WAKE and V_{BB} towards GND; HBM (Note 13)	−6	+6	kV
	Electrostatic discharge on LIN, WAKE and V_{BB}; system HBM (Note 15)	−12	+12	kV
	Electrostatic discharge voltage on all pins; CDM (Note 16)	−750	+750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

11. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, and 5. The device complies with functional class C; class A can be reached depending on the application and external components.
12. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. The device complies with functional class C; class A can be reached depending on the application and external components.
13. Equivalent to discharging a 100 pF capacitor through a 1500 Ω resistor.
14. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 61000−4−2. LIN bus filter 220 pF, V_{BB} blocking capacitor 100 nF, 3k3/10n R/C network on WAKE.
15. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 61000−4−2. No filter on LIN, V_{BB} blocking capacitor 100 nF, 3k3/10n R/C network on WAKE.
16. Charged device model according ESD-STM5.3.1.

Table 7. DC CHARACTERISTICS – 3.3 V version
(V_{BB} = 5 V to 26 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY − Pin V_{BB}						
I_{BB_ON}	Supply current	Normal mode; LIN recessive			1.6	mA
I_{BB_STB}	Supply current	Standby mode, V_{BB} = 5–18 V, T_J < 105°C			70	μA
I_{BB_SLP}	Supply current	Sleep mode, V_{BB} = 5–18 V, T_J < 105°C			20	μA
VOLTAGE REGULATOR − Pin V_{CC}						
V_{CC_OUT}	Regulator output voltage	V_{CC} load 1 mA − 30 mA	3.23	3.30	3.37	V
		V_{CC} load 0 mA − 50 mA	3.19	3.30	3.41	
$I_{OUT\_MAX\_ABS}$	Absolute maximum output current	Thermal shutdown must be taken into account			50	mA
I_{OUT_LIM}	Overcurrent limitation		50	100	170	mA
ΔV_{CC_OUT}	Line Regulation (Note 22)	V_{BB} 5−26 V, I_{OUT} = 5 mA, T_J = 25°C		0.5		mV
	Load Regulation (Note 22)	I_{OUT} 1−50 mA, V_{BB} = 14 V, T_J = 25°C		45		mV
V_{DO}	Dropout Voltage (V_{BB}−V_{CC_OUT}) Figure 11, (Notes 21, 22)	I_{OUT} = 1 mA, T_J = 25°C		13		mV
		I_{OUT} = 10 mA, T_J = 25°C		134		mV
		I_{OUT} = 50 mA, T_J = 25°C		732		mV
LIN TRANSMITTER − Pin LIN						
$V_{LIN\_dom\_LoSup}$	LIN dominant output voltage	TxD = low; V_{BB} = 7.3 V			1.2	V
$V_{LIN\_dom\_HiSup}$	LIN dominant output voltage	TxD = low; V_{BB} = 18 V			2.0	V
V_{LIN_REC}	LIN Recessive Output Voltage (Note 17)	TxD = high; I_{LIN} = 10 μA	V_{BB} − 1.5		V_{BB}	V
I_{LIN_lim}	Short circuit current limitation	V_{LIN} = V_{BB_MAX}	40		200	mA
R_{SLAVE}	Internal pull−up resistance		20	33	47	kΩ
C_{LIN}	Capacitance on pin LIN (Note 19)			15	25	pF
LIN RECEIVER − Pin LIN						
V_{bus_dom}	Bus voltage for dominant state				0.4	V_{BB}
V_{bus_rec}	Bus voltage for recessive state		0.6			V_{BB}
V_{rec_dom}	Receiver threshold	LIN bus recessive → dominant	0.4		0.6	V_{BB}
V_{rec_rec}	Receiver threshold	LIN bus dominant → recessive	0.4		0.6	V_{BB}
V_{rec_cnt}	Receiver centre voltage	(Vrec_dom + Vrec_rec) / 2	0.475		0.525	V_{BB}
V_{rec_hys}	Receiver hysteresis	(Vrec_rec − Vrec_dom)	0.05		0.175	V_{BB}
$I_{LIN\_off\_dom}$	LIN output current bus in dominant state	Driver off; V_{BB} = 12 V, V_{LIN} = 0 V	−1			mA
$I_{LIN\_off\_rec}$	LIN output current bus in recessive state	Driver off; V_{BB} < 18 V V_{BB} < V_{LIN} < 18 V			1	μA
$I_{LIN\_no\_GND}$	Communication not affected	V_{BB} = GND = 12 V; 0 < V_{LIN} < 18 V	−1		1	mA

17. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.
18. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420−3 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.
19. Guaranteed by design. Not tested.
20. V_{BB} undervoltage threshold is always higher than V_{BB} POR low level ($V_{BB\_UV\_th}$ > PORL_V_{BB})
21. Measured at output voltage V_{CC_OUT} = (V_{CC_OUT}@V_{BB} = 5 V) – 2%.
22. Values based on design and characterization. Not tested in production.

Table 7. DC CHARACTERISTICS – 3.3 V version
(V_{BB} = 5 V to 26 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN RECEIVER − Pin LIN						
$I_{LIN\_no\_VBB}$	LIN bus remains operational	V_{BB} = GND = 0 V; 0 < V_{LIN} < 18 V			5	μA
Pin WAKE						
V_{WAKE_th}	Threshold voltage		0.35		0.65	V_{BB}
I_{LEAK}	Input leakage current (Note 18)	V_{WAKE} = 0 V; V_{BB} = 18 V	−1	−0.5	1	μA
t_{WAKE_MIN}	Debounce time	Sleep mode; rising and falling edge	8		54	μs
Pins TxD and STB						
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
R_{PU}	Pull−up resistance to V_{CC} (Note 18)		50		200	kΩ
Pin INH						
Delta_V_H	High level voltage drop	I_{INH} = 15 mA		0.35	0.75	V
I_{LEAK}	Leakage current	Sleep mode; V_{INH} = 0 V	−1		1	μA
Pin EN						
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
R_{PD}	Pull−down resistance to ground (Note 18)		50		200	kΩ
Pin RxD						
V_{OL}	Low level output voltage	I_{SINK} = 2 mA			0.65	V
V_{OH}	High level output voltage (In Normal mode)	Normal mode, I_{SOURCE} = −2 mA	V_{CC} − 0.65 V			V
R_{PU}	Pull−up resistance to V_{CC} (In Standby and Sleep mode)	Standby mode, Sleep mode	5	10	15	kΩ
POR AND VOLTAGE MONITOR						
$V_{BB\_UV\_th}$	V_{BB} undervoltage threshold (Note 20)		3	4.2	4.75	V
PORL_V_{BB}	V_{BB} POR low level comparator	NCV7420D23	2.5		4.2	V
		NCV7420D24	1.7		3.8	V
$V_{CC\_UV\_th}$	V_{CC} undervoltage threshold		2		3	V
THERMAL SHUTDOWN						
T_{JSD}	Thermal Shutdown Junction Temperature	For shutdown	165		195	°C
T_{JSD_HYST}	Thermal shutdown hysteresis		9		18	°C

17. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.
18. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420−3 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.
19. Guaranteed by design. Not tested.
20. V_{BB} undervoltage threshold is always higher than V_{BB} POR low level ($V_{BB\_UV\_th}$ > PORL_V_{BB})
21. Measured at output voltage V_{CC_OUT} = (V_{CC_OUT}@V_{BB} = 5 V) – 2%.
22. Values based on design and characterization. Not tested in production.

Table 8. DC CHARACTERISTICS – 5 V version
(V_{BB} = 6 V to 26 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY − Pin V_{BB}						
I_{BB_ON}	Supply current	Normal mode; LIN recessive			1.6	mA
I_{BB_STB}	Supply current	Standby mode, V_{BB} = 6–18 V, T_J < 105°C			70	μA
I_{BB_SLP}	Supply current	Sleep mode, V_{BB} = 6–18 V, T_J < 105°C			20	μA
VOLTAGE REGULATOR − Pin V_{CC}						
V_{CC_OUT}	Regulator output voltage	V_{CC} load 1 mA − 30 mA	4.9	5.0	5.1	V
		V_{CC} load 0 mA − 50 mA	4.83	5.0	5.17	
$I_{OUT\_MAX\_ABS}$	Absolute maximum output current	Thermal shutdown must be taken into account			50	mA
I_{OUT_LIM}	Overcurrent limitation		50	100	170	mA
ΔV_{CC_OUT}	Line Regulation (Note 28)	V_{BB} 6−26 V, I_{OUT} = 5 mA, T_J = 25°C		0.9		mV
	Load Regulation (Note 28)	I_{OUT} 1−50 mA, V_{BB} = 14 V, T_J = 25°C		74		mV
V_{DO}	Dropout Voltage (V_{BB}−V_{CC_OUT}) Figure 19 (Notes 27, 28)	I_{OUT} = 1 mA, T_J = 25°C		13		mV
		I_{OUT} = 10 mA, T_J = 25°C		136		mV
		I_{OUT} = 50 mA, T_J = 25°C		794		mV
LIN TRANSMITTER − Pin LIN						
$V_{LIN\_dom\_LoSup}$	LIN dominant output voltage	TxD = low; V_{BB} = 7.3 V			1.2	V
$V_{LIN\_dom\_HiSup}$	LIN dominant output voltage	TxD = low; V_{BB} = 18 V			2.0	V
V_{LIN_rec}	LIN Recessive Output Voltage (Note 23)	TxD = high; I_{LIN} = 10 μA	V_{BB} − 1.5		V_{BB}	V
I_{LIN_lim}	Short circuit current limitation	V_{LIN} = V_{BB_MAX}	40		200	mA
R_{SLAVE}	Internal pull−up resistance		20	33	47	kΩ
C_{LIN}	Capacitance on pin LIN (Note 25)			15	25	pF
LIN RECEIVER − Pin LIN						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{bus_dom}	Bus voltage for dominant state				0.4	V_{BB}
V_{bus_rec}	Bus voltage for recessive state		0.6			V_{BB}
V_{rec_dom}	Receiver threshold	LIN bus recessive → dominant	0.4		0.6	V_{BB}
V_{rec_rec}	Receiver threshold	LIN bus dominant → recessive	0.4		0.6	V_{BB}
V_{rec_cnt}	Receiver center voltage	(Vrec_dom + Vrec_rec) / 2	0.475		0.525	V_{BB}
V_{rec_hys}	Receiver hysteresis	(Vrec_rec − Vrec_dom)	0.05		0.175	V_{BB}
$I_{LIN\_off\_dom}$	LIN output current bus in dominant state	Driver off; V_{BB} = 12 V; V_{LIN} = 0 V	−1			mA
$I_{LIN\_off\_rec}$	LIN output current bus in recessive state	Driver off; V_{BB} < 18 V V_{BB} < V_{LIN} < 18 V			1	μA

23. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.
24. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420−5 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.
25. Guaranteed by design. Not tested.
26. V_{BB} undervoltage threshold is always higher than V_{BB} POR low level ($V_{BB\_UV\_th}$ > PORL_V_{BB})
27. Measured at output voltage V_{CC_OUT} = (V_{CC_OUT}@V_{BB} = 6 V) – 2%.
28. Values based on design and characterization. Not tested in production.

Table 8. DC CHARACTERISTICS – 5 V version
(V_{BB} = 6 V to 26 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_{BB} to LIN); unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN RECEIVER − Pin LIN						
$I_{LIN\_no\_GND}$	Communication not affected	V_{BB} = GND = 12 V; 0 < V_{LIN} < 18 V	−1		1	mA
$I_{LIN\_no\_VBB}$	LIN bus remains operational	V_{BB} = GND = 0 V; 0 < V_{LIN} < 18 V			5	μA
Pin WAKE						
V_{WAKE_th}	Threshold voltage		0.35		0.65	V_{BB}
I_{LEAK}	Input leakage current (Note 24)	V_{WAKE} = 0 V; V_{BB} = 18 V	−1	−0.5	1	μA
t_{WAKE_MIN}	Debounce time	Sleep mode; rising and falling edge	8		54	μs
Pins TxD and STB						
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
R_{PU}	Pull−up resistance to V_{CC} (Note 24)		50		200	kΩ
Pin INH						
Delta_V_H	High level voltage drop	I_{INH} = 15 mA		0.35	0.75	V
I_{LEAK}	Leakage current	Sleep mode; V_{INH} = 0 V	−1		1	μA
Pin EN						
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
R_{PD}	Pull−down resistance to ground (Note 24)		50		200	kΩ
Pin RxD						
V_{OL}	Low level output voltage	I_{SINK} = 2 mA			0.65	V
V_{OH}	High level output voltage (In Normal mode)	Normal mode, I_{SOURCE} = −2 mA	V_{CC} − 0.65 V			V
R_{PU}	Pull−up resistance to V_{CC} (In Standby and Sleep mode)	Standby mode, Sleep mode	5	10	15	kΩ
POR AND VOLTAGE MONITOR						
$V_{BB\_UV\_th}$	V_{BB} undervoltage threshold (Note 26)		3	4.2	4.75	V
PORL_V_{BB}	V_{BB} POR low level comparator	NCV7420D25	2.5		4.2	V
		NCV7420D26	1.7		3.8	V
$V_{CC\_UV\_th}$	V_{CC} undervoltage threshold		3		4.5	V
THERMAL SHUTDOWN						
T_{JSD}	Thermal Shutdown Junction Temperature	For shutdown	165		195	°C
T_{JSD_HYST}	Thermal shutdown hysteresis		9		18	°C

23. The voltage drop in Normal mode between LIN and V_{BB} pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.
24. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420−5 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.
25. Guaranteed by design. Not tested.
26. V_{BB} undervoltage threshold is always higher than V_{BB} POR low level ($V_{BB\_UV\_th}$ > PORL_V_{BB})
27. Measured at output voltage V_{CC_OUT} = (V_{CC_OUT}@V_{BB} = 6 V) – 2%.
28. Values based on design and characterization. Not tested in production.

AC Characteristics – 3.3 V and 5 V versions – (V_{BB} = 7 V to 18 V; T_J = −40°C to +150°C; unless otherwise specified.)

Table 9. AC CHARACTERISTICS LIN TRANSMITTER − Pin LIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT}) see Figure 23	Normal slope mode $TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} t_{BIT} = 50 μs V_{BB} = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT}) see Figure 23	Normal slope mode $TH_{REC(min)}$ = 0.422 x V_{BB} $TH_{DOM(min)}$ = 0.284 x V_{BB} t_{BIT} = 50 μs V_{BB} = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT}) see Figure 23	Normal slope mode $TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} t_{BIT} = 96 μs V_{BB} = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT}) see Figure 23	Normal slope mode $TH_{REC(min)}$ = 0.389 x V_{BB} $TH_{DOM(min)}$ = 0.251 x V_{BB} t_{BIT} = 96 μs V_{BB} = 7.6 V to 18 V	0.5		0.590	
$t_{trx\_prop\_down}$	Propagation Delay of TxD to LIN. TxD high to low	(Note 29)			6	μs
$t_{trx\_prop\_up}$	Propagation Delay of TxD to LIN. TxD low to high	(Note 29)			6	μs
t_{fall_norm}	LIN falling edge	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 30)			22.5	μs
t_{rise_norm}	LIN rising edge	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 30)			22.5	μs
t_{sym_norm}	LIN slope symmetry	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 30)	−4		4	μs
t_{fall_norm}	LIN falling edge	Normal slope mode; V_{BB} = 12 V; L3 (Note 30)			27	μs
t_{rise_norm}	LIN rising edge	Normal slope mode; V_{BB} = 12 V; L3 (Note 30)			27	μs
t_{sym_norm}	LIN slope symmetry	Normal slope mode; V_{BB} = 12 V; L3 (Note 30)	−5		5	μs
t_{fall_low}	LIN falling edge	Low slope mode (Note 31); V_{BB} = 12 V; L3 (Note 30)			62	μs
t_{rise_low}	LIN rising edge	Low slope mode (Note 31); V_{BB} = 12 V; L3 (Note 30)			62	μs
t_{wake}	Dominant timeout for wake−up via LIN bus		30		150	μs
t_{dom}	TxD dominant timeout	TxD = low	6		20	ms

29. Values based on design and characterization. Not tested in production.
30. The AC parameters are specified for following RC loads on the LIN bus: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF.
31. Low slope mode is not compliant to the LIN standard.

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V VERSION

Load Transient Responses

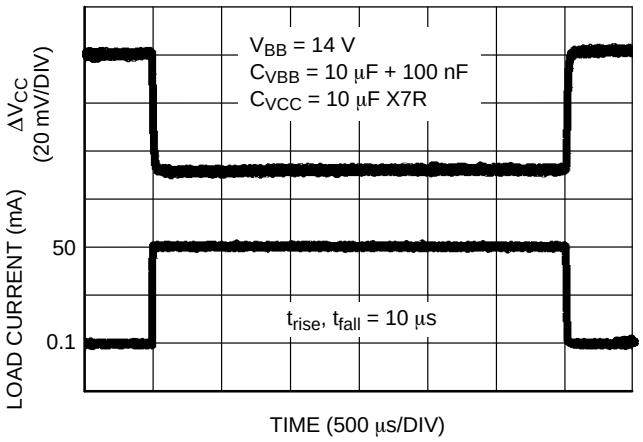


Figure 7. Load Transient Response (I_{CC} 100 μA to 50 mA)

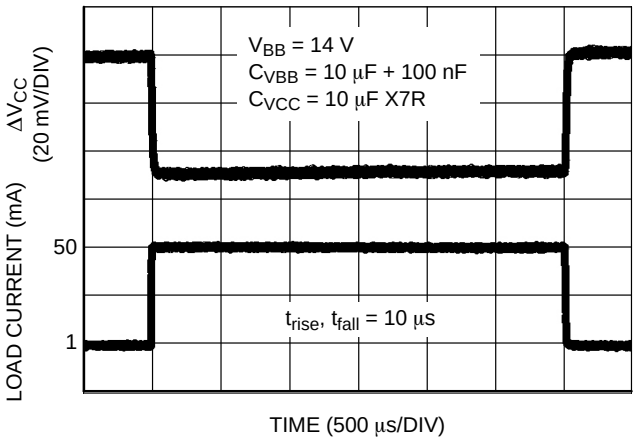


Figure 8. Load Transient Response (I_{CC} 1 mA to 50 mA)

Line Transient Responses

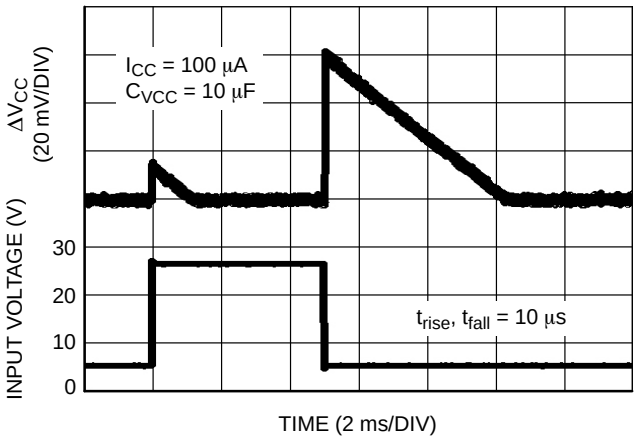


Figure 9. Line Transient Response (V_{BB} 5 V to 26 V)

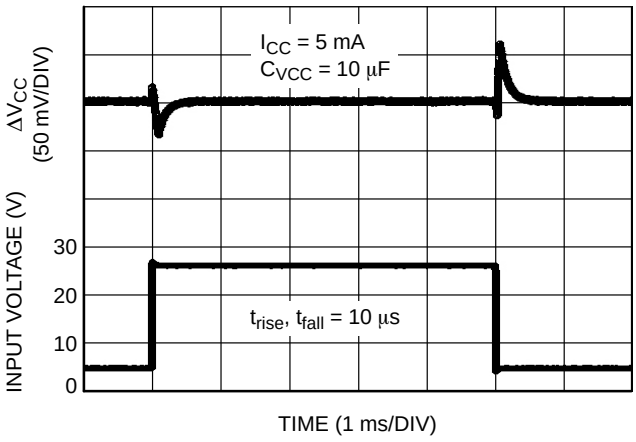


Figure 10. Line Transient Response (V_{BB} 5 V to 26 V)

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V VERSION

Static Characteristics

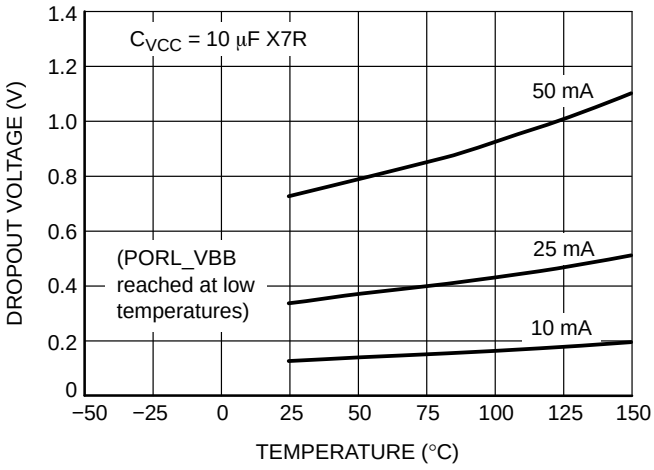


Figure 11. Dropout Voltage vs. Temperature

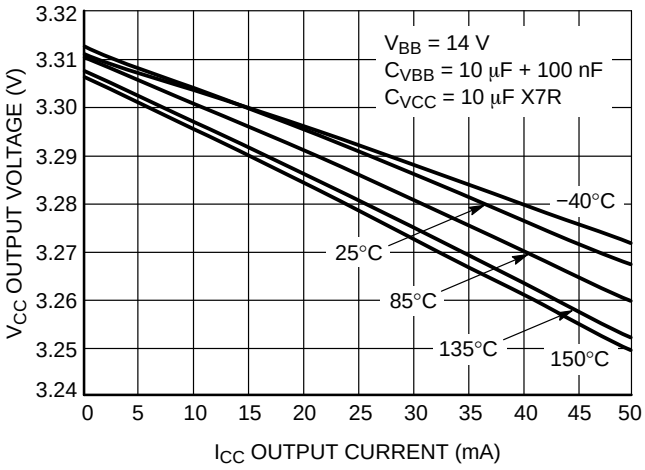


Figure 12. Output Voltage vs. Output Current

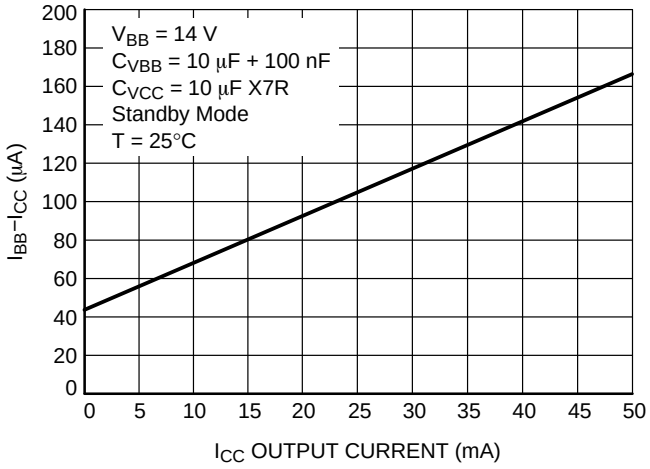


Figure 13. Ground Current vs. Output Current

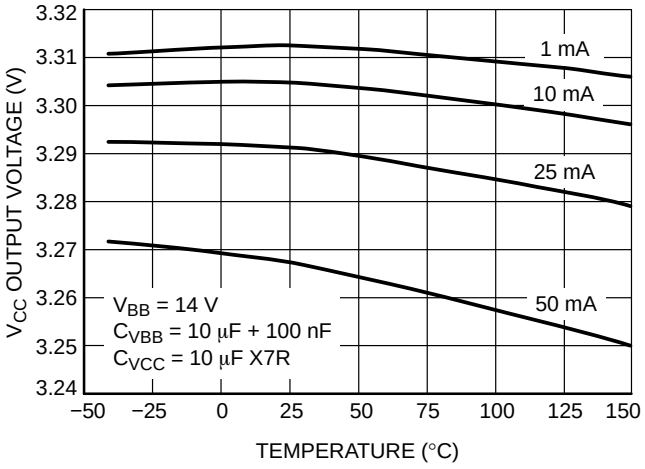


Figure 14. Output Voltage vs. Temperature

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS − 5 V VERSION

Load Transient Responses

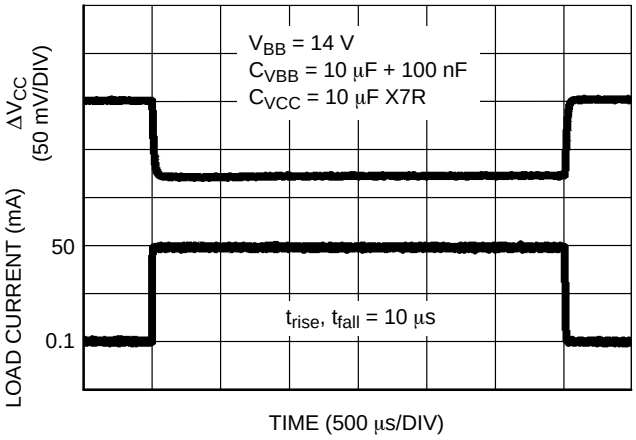


Figure 15. Load Transient Response (I_{CC} 100 μA to 50 mA)

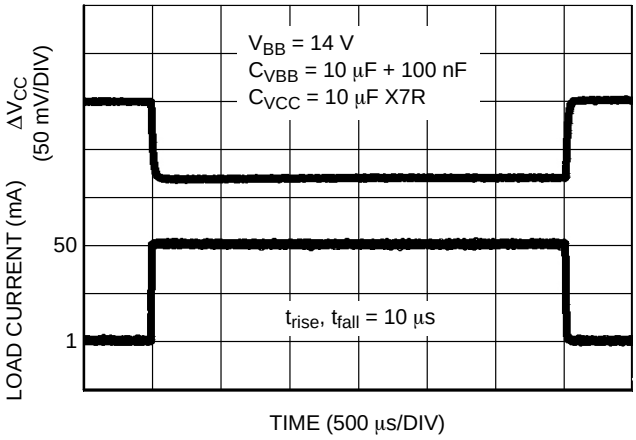


Figure 16. Load Transient Response (I_{CC} 1 mA to 50 mA)

Line Transient Responses

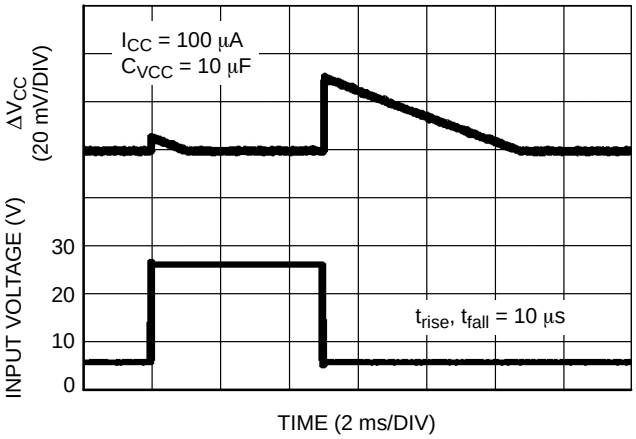


Figure 17. Line Transient Response (V_{BB} 6 V to 26 V)

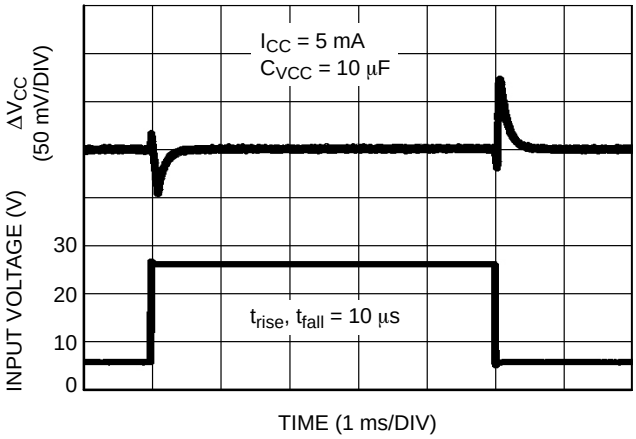


Figure 18. Line Transient Response (V_{BB} 6 V to 26 V)

REGULATOR TYPICAL PERFORMANCE CHARACTERISTICS − 5 V VERSION

Static Characteristics

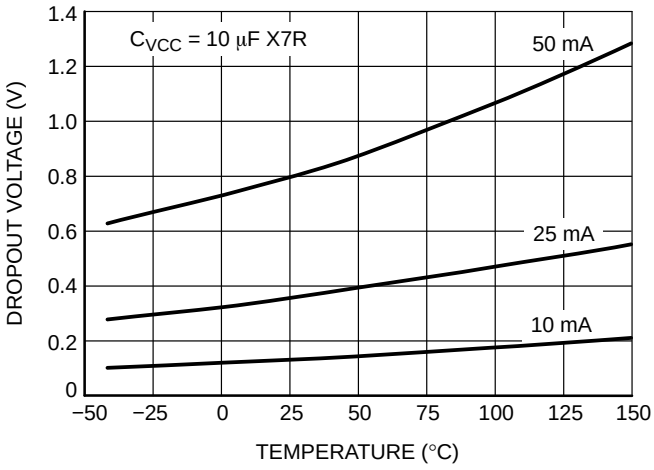


Figure 19. Dropout Voltage vs. Temperature

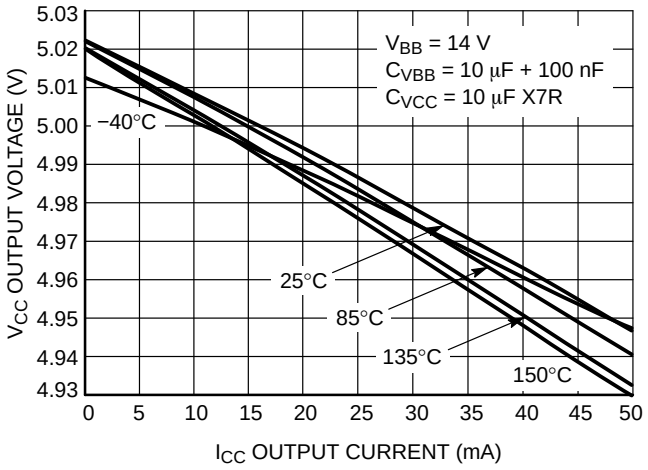


Figure 20. Output Voltage vs. Output Current

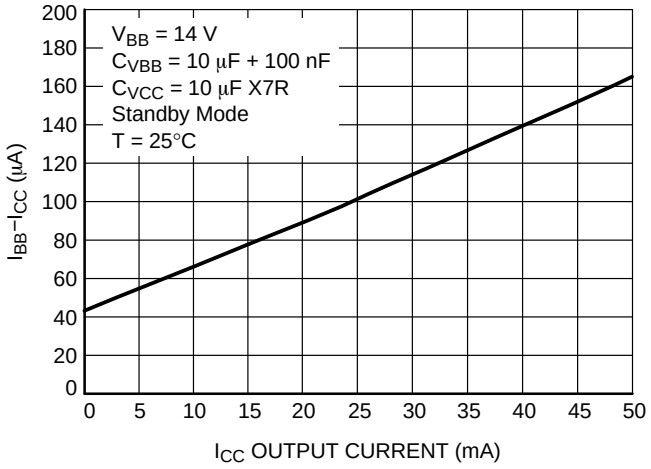


Figure 21. Ground Current vs. Output Current

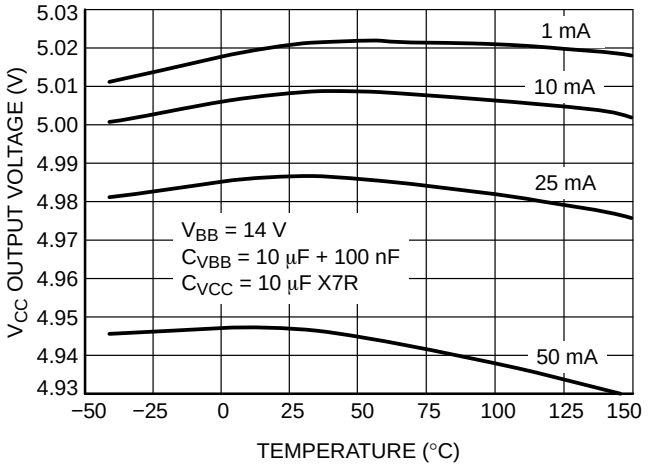


Figure 22. Output Voltage vs. Temperature

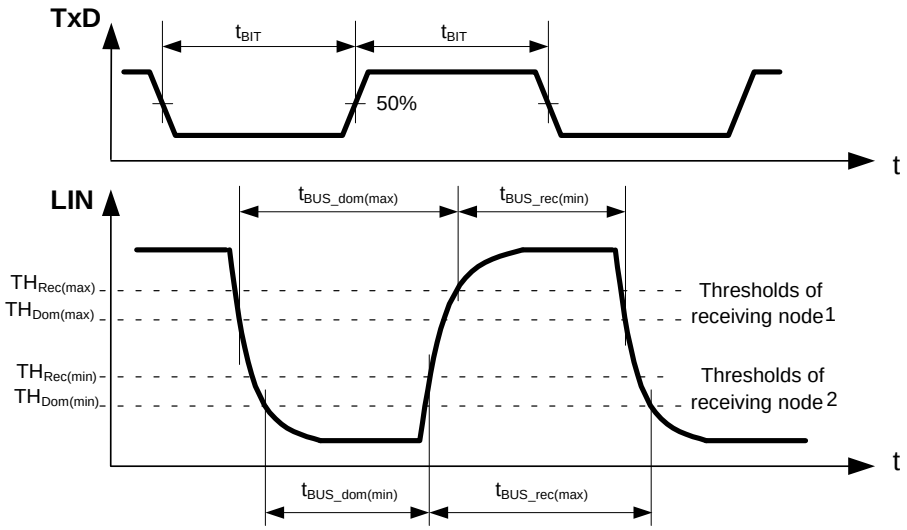


Figure 23. LIN Transmitter Duty Cycle

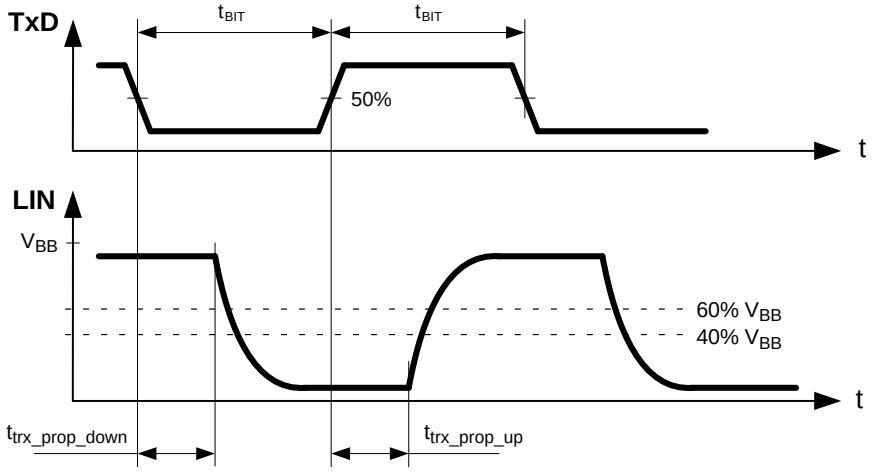


Figure 24. LIN Transmitter Timing

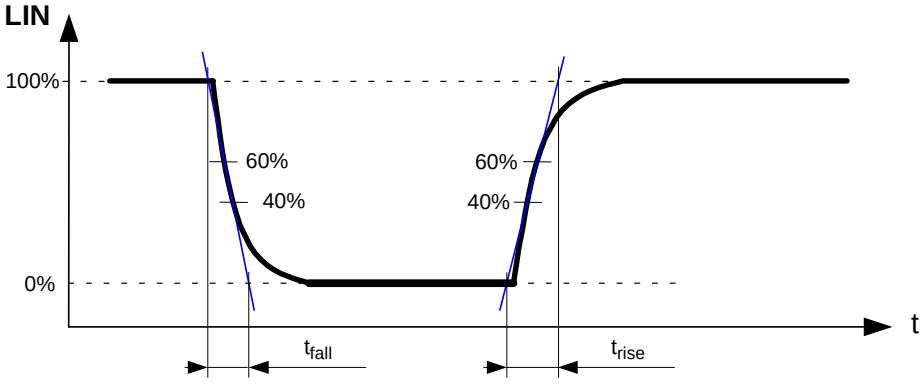


Figure 25. LIN Transmitter Rising and Falling Times

Table 10. AC CHARACTERISTICS LIN RECEIVER

Symbol Pin LIN	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rec\_prop\_down}$	Propagation delay of receiver falling edge		0.1		6	μs
$t_{rec\_prop\_up}$	Propagation delay of receiver rising edge		0.1		6	μs
t_{rec_sym}	Propagation delay symmetry	$t_{rec\_prop\_down} - t_{rec\_prop\_up}$	−2		2	μs

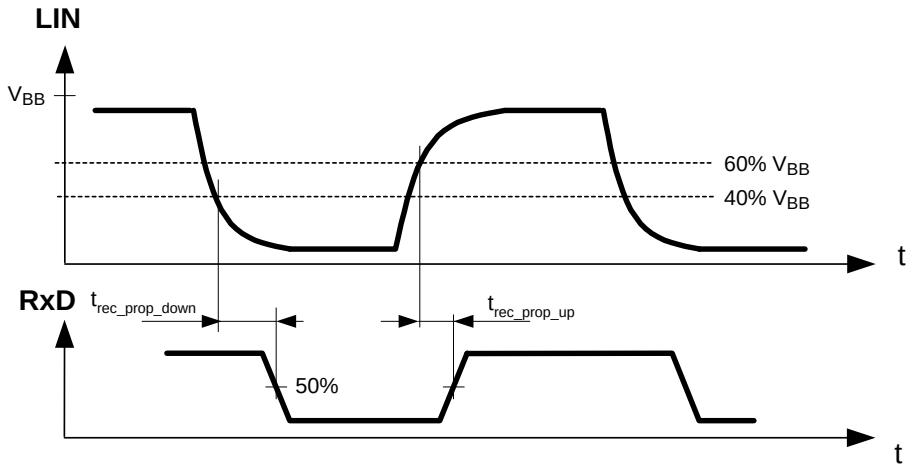


Figure 26. LIN Receiver Timing

ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping†
NCV7420D23G	LIN Transceiver + 3.3 V Vreg.	−40°C to 125°C	SOIC−14 (Pb−Free)	55 / Tube/Rail
NCV7420D23R2G	LIN Transceiver + 3.3 V Vreg.			3000 / Tape & Reel
NCV7420D24G	EMC/ESD Improved LIN Transceiver + 3.3 V Vreg.			55 / Tube/Rail
NCV7420D24R2G	EMC/ESD Improved LIN Transceiver + 3.3 V Vreg.			3000 / Tape & Reel
NCV7420D25G	LIN Transceiver + 5 V Vreg.			55 / Tube/Rail
NCV7420D25R2G	LIN Transceiver + 5 V Vreg.			3000 / Tape & Reel
NCV7420D26G	EMC/ESD Improved LIN Transceiver + 5 V Vreg.			55 / Tube/Rail
NCV7420D26R2G	EMC/ESD Improved LIN Transceiver + 5 V Vreg.			3000 / Tape & Reel

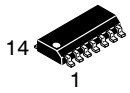
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SOIC−14
CASE 751AP
ISSUE B

DATE 18 MAY 2015



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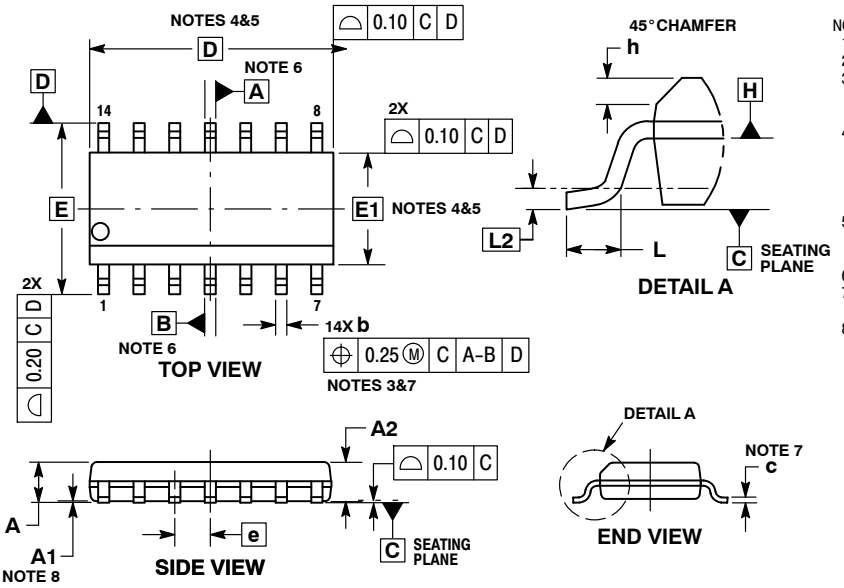
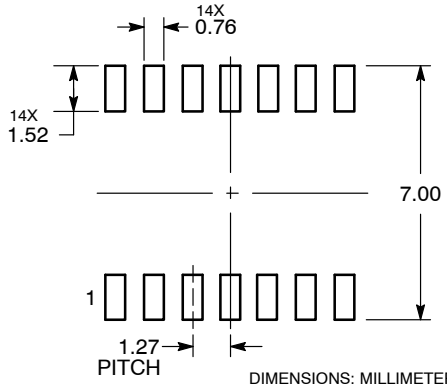


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

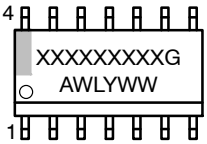
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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