Dual CAN FD Transceiver, High Speed, Low Power

NCV7446

ON Semiconductor®

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Description

NCV7446 is a dual CAN FD physical layer transceiver. It allows interfacing of two independent CAN physical buses and two independent CAN protocol controllers. The transceivers provide differential transmit capability to the bus and differential receive capability to the CAN controllers.

It is consisted of two fully independent NCV7344 transceivers. The NCV7446 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbps to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7446 an excellent choice for all types of HS−CAN networks, in nodes that require a low−power mode with wake−up capability via the CAN bus.

Features

- Compliant with the ISO 11898−2:2016
- CAN FD Timing Specified up to 5 Mbps
- Very Low Current Standby Mode with Wake−up via the Bus
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity
- No Disturbance of the Bus Lines with an Un−powered Node
- Transmit Data (TxD) Dominant Timeout Function
- Under All Supply Conditions the Chip Behaves Predictably
- Very High ESD Robustness of Bus Pins
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment

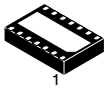
Quality

- Wettable Flank Package for Enhanced Optical Inspection
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive
- Industrial Networks

MARKING DIAGRAM



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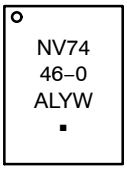
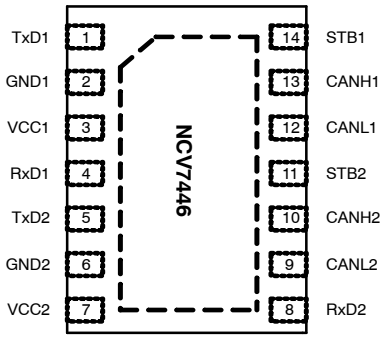


NV7446−0 = Specific Device Code
A = Assembly Site
L = Wafer Lot
Y = Year of Production, Last Number
W = Work Week Number
▪ = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

BLOCK DIAGRAM

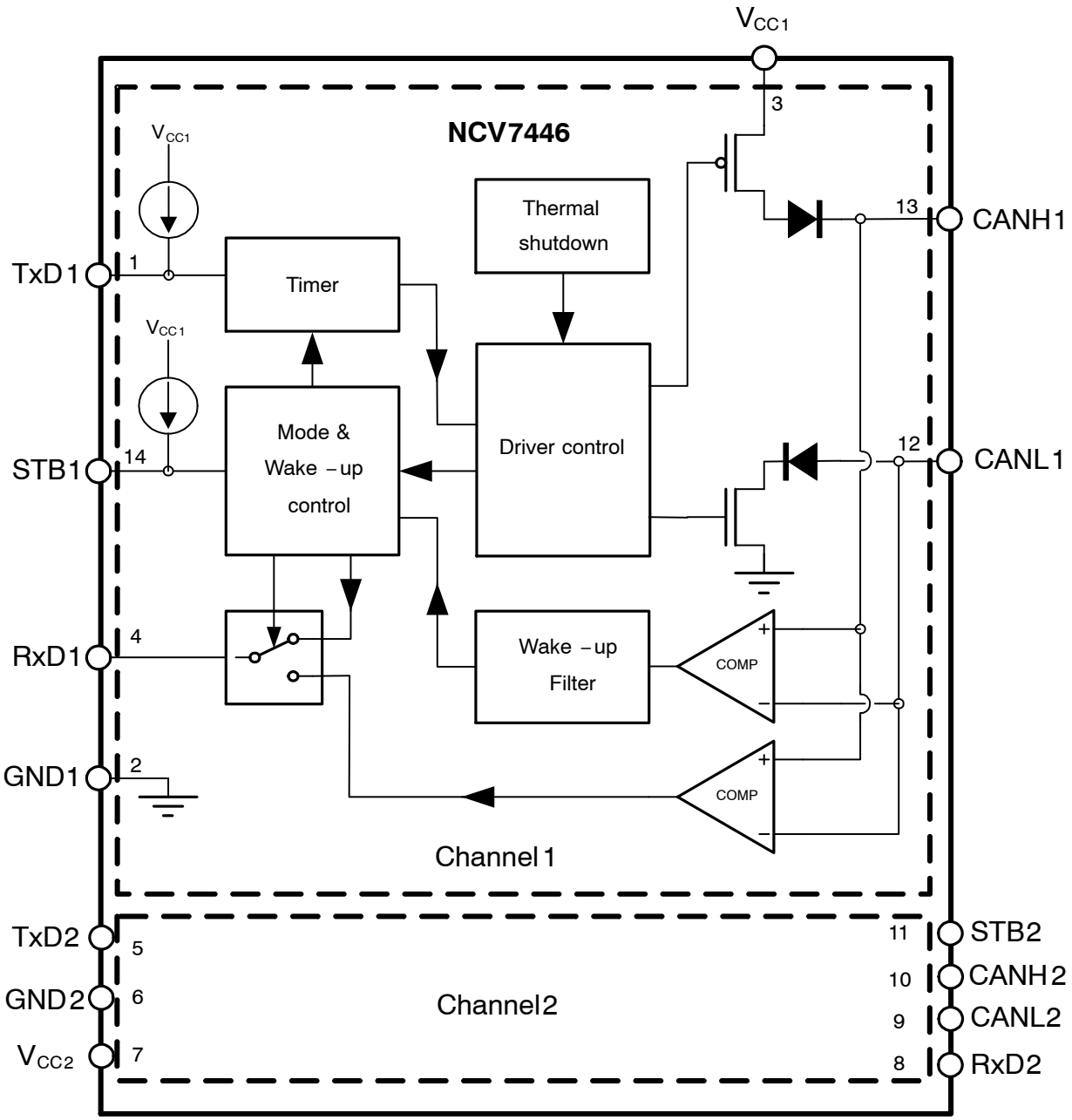


Figure 1. NCV7446 Block Diagram

TYPICAL APPLICATION DIAGRAM

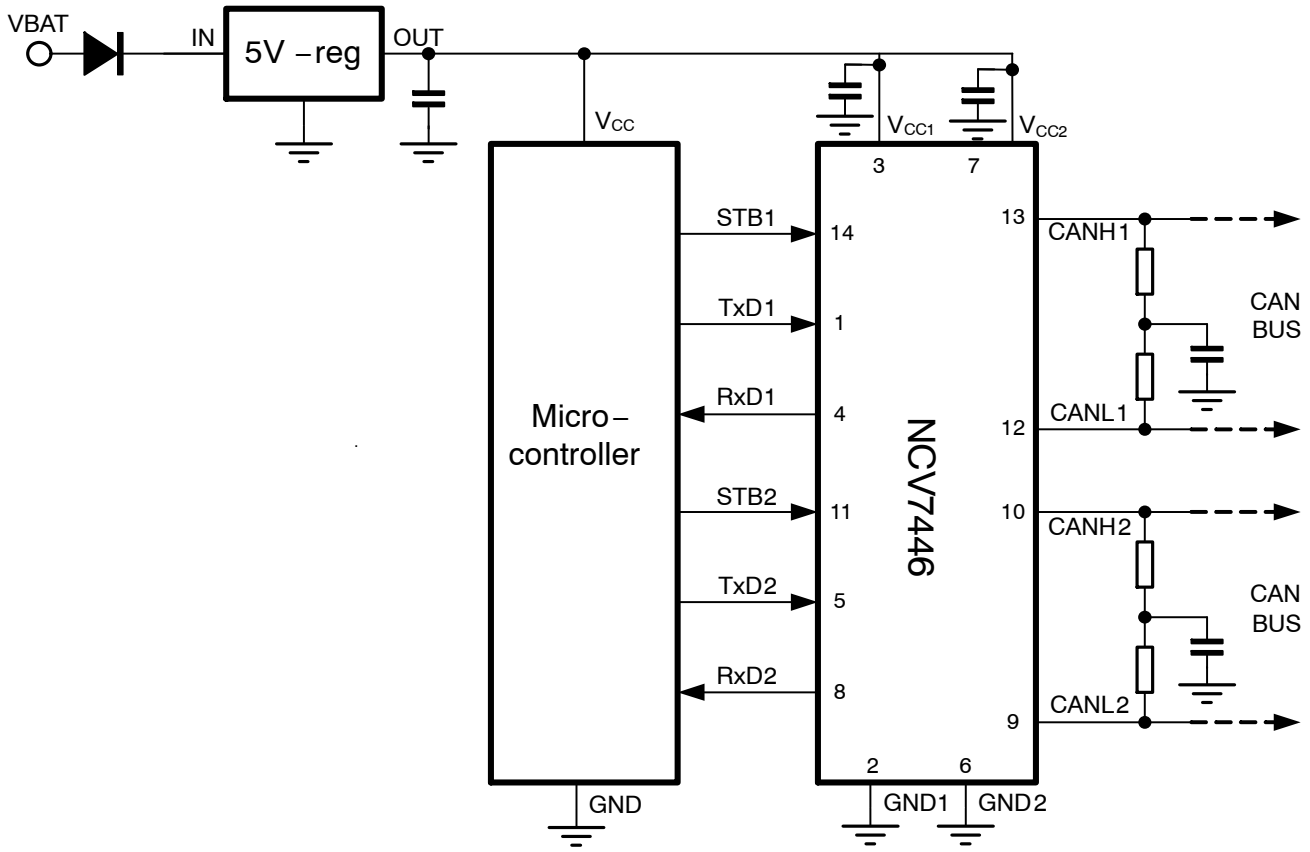


Figure 2. NCV7446 Application Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
1	TxD1	Transmit data input for channel 1; low input → dominant driver; internal pull−up current
2	GND1	Ground for channel 1
3	V_{CC1}	Supply voltage for channel 1
4	RxD1	Receive data output for channel 1; dominant transmitter → low output
5	TxD2	Transmit data input for channel 2; low input → dominant driver; internal pull−up current
6	GND2	Ground for channel 2
7	V_{CC2}	Supply voltage for channel 2
8	RxD2	Receive data output for channel 2; dominant transmitter → low output
9	CANL2	Low−level CAN bus line channel 2 (low in dominant mode)
10	CANH2	High−level CAN bus line channel 2 (high in dominant mode)
11	STB2	Standby mode control input for channel 2; internal pull−up current
12	CANL1	Low−level CAN bus line channel 1 (low in dominant mode)
13	CANH1	High−level CAN bus line channel 1 (high in dominant mode)
14	STB1	Standby mode control input for channel 1; internal pull−up current
EP	Exposed Pad	Recommended to connect to GND or left floating in application

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7446 provides two modes of operation per transceiver as illustrated in Table 2. These modes are selectable through pins STB1 and STB2 independently for each transceiver.

Table 2. OPERATING MODES

Pins STBx	Mode	Pins RxDx	
Low	Normal	Low when bus dominant	High when bus recessive
High	Standby	Follows the bus when wake−up detected	High when no wake−up request detected

Normal Mode

In the normal mode, the selected transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxDx and RxDx. The slopes on the bus lines outputs are optimized to give low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are biased to ground and supply current is reduced to a minimum. When a wake−up request is detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of t_{wake_filt}, the corresponding RxDx pin is driven low by the transceiver (following the bus) to inform the controller of the wake−up request.

Wake−up

When a valid wake−up pattern (phase in order dominant − recessive − dominant) is detected during the standby mode the RxDx pins follows the bus. Minimum length of each phase is t_{wake_filt} − see Figure 3.

Pattern must be received within t_{wake_to} to be recognized as valid wake−up otherwise internal logic is reset.

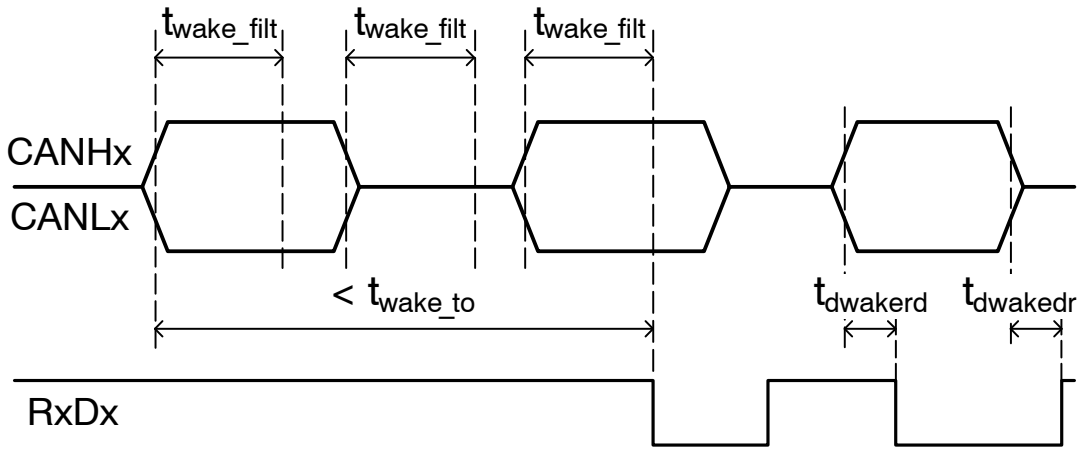


Figure 3. NCV7446 Wake−up behavior

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the affected transmitter if the junction temperature exceeds a value of approximately 170°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pins TxDx goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxDx Dominant Timeout Function

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pins TxDx are forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pins TxDx. If the duration of the low−level on pins TxDx exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pins TxDx.

This TxD dominant timeout time $t_{dom(TxD)}$ defines the minimum possible bit rate to 17 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Undervoltage on V_{CC1} or V_{CC2} pins prevents the chip sending data on the bus when there is not enough V_{CC} supply voltage.

After supply is recovered, corresponding TxD pin must be first released to high to allow sending dominant bits again. Recovery time from undervoltage detection is equal to td(stb−nm) time.

The pins CANHx and CANLx are protected from automotive electrical transients (according to ISO 7637; see Figure 5). Pins TxDx and STBx are pulled high internally should the input become disconnected. Pins TxDx, STBx and RxDx will be floating, preventing reverse supply should the adjacent VCCx supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GNDx (pin 2 or pin 6). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply voltage V_{CC1}, V_{CC2}		−0.3	+6	V
V_{CANH}	DC voltage at pins CANHx	0 < V_{CCX} < 5.25 V; no time limit	−42	+42	V
V_{CANL}	DC voltage at pins CANLx	0 < V_{CCX} < 5.25 V; no time limit	−42	+42	V
$V_{CANH-CANL}$	DC voltage between any two pins (including CANHx and CANLx)		−42	+42	V
V_{IN}	DC Voltage at pins TxDx, STBx		−0.3	+6	V
V_{OUT}	DC Voltage at pin RxDx		−0.3	V_{CCx} + 0.3	V
V_{esdHBM}	Electrostatic discharge voltage at all pins, Component HBM	(Note 1)	−8	+8	kV
V_{esdCDM}	Electrostatic discharge voltage at all pins, Component CDM	(Note 2)	−750	+750	V
V_{esdIEC}	Electrostatic discharge voltage at pins CANHx and CANLx, System HBM (Note 4)	Without bus filter (Note 3)	−7	+7	kV
		With bus filter (Note 3)	−11	+11	kV
V_{schaff}	Voltage transients, pins CANHx, CANLx. According to ISO7637−3, Class C (Note 4)	test pulses 1	−100		V
		test pulses 2a		+75	V
		test pulses 3a	−150		V
		test pulses 3b		+100	V
Latch−up	Static latch−up at all pins	(Note 5)		150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_J	Maximum junction temperature		−40	+170	°C
MSL	Moisture Sensitivity Level		1		−
T_{SLD}	Lead temperature Soldering − Reflow (Note 11)		−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC−Q100−011.
3. System human body model electrostatic discharge (ESD) pulses in accordance to IEC 61000−4−2. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GNDx.
4. Results were verified by external test house.
5. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.
6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, JEDEC 1S0P PCB	Free air; (Note 8)	101	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, JEDEC 2S2P PCB	Free air; (Note 9)	53	K/W
$R_{\theta JA\_3}$	Thermal Resistance Junction−to−Air	Free air; (Note 10)	76	K/W
$R_{\theta JA\_4}$	Thermal Resistance Junction−to−Air	Free air; (Note 11)	46	K/W

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
9. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.
10. Test board according to EIA/JEDEC Standard JESD51−3 and JESD51−5 , signal layer with 10% trace coverage and with thermal via array under the exposed pad connected to the second copper layer.
11. Test board according to EIA/JEDEC Standard JESD51−5 and JESD51−7, signal layers with 10% trace coverage and thermal via array under the exposed pad connected to the first inner copper layer.

Table 5. ELECTRICAL CHARACTERISTICS
V_{CC1}, V_{CC2} = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF, unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (PINS V_{CCx})						
V_{CCx}	Power supply voltage	(Note 12)	4.75	5.0	5.25	V
I_{CCx}	Supply current on **single** channel	Dominant; V_{TxDx} = Low	20	45	55	mA
		Recessive; V_{TxDx} = Low	1.9	5.0	10	mA
		Normal mode, Dominant; V_{TxDx} = 0 V; one of bus wires shorted; −3 V ≤ (V_{CANHx}, V_{CANLx}) ≤ +18 V	2.0	–	105	mA
I_{CCSx}	Supply current in standby mode on **single** channel	T_J ≤ 100°C, (Note 13)	–	10	15	μA
$V_{UVD(VCC)(stby)}$	Standby undervoltage detection V_{CCx} pins		3.5	4.0	4.3	V
$V_{UVD(VCC)(swoff)}$	Switch−off undervoltage detection V_{CCx} pins		2.0	2.3	2.6	V
TRANSMITTER DATA INPUT (Pins TxDx)						
V_{IH}	High−level input voltage	Output recessive	2.0	–	–	V
V_{IL}	Low−level input voltage	Output dominant	–	–	+0.8	V
I_{IH}	High−level input current	V_{TxDx} = V_{CCx}	−5.0	0	+5.0	μA
I_{IL}	Low−level input current	V_{TxDx} = 0 V	−300	−150	−70	μA
C_i	Input capacitance	(Note 13)	–	5	10	pF
TRANSMITTER MODE SELECT (Pins STBx)						
V_{IH}	High−level input voltage	Standby mode	2.0	–	–	V
V_{IL}	Low−level input voltage	Normal mode	–	–	+0.8	V
I_{IH}	High−level input current	V_{STBx} = V_{CCx}	−1.0	0	+1.0	μA
I_{IL}	Low−level input current	V_{STBx} = 0 V	−15	–	−1.0	μA
C_i	Input capacitance	(Note 13)	–	5	10	pF
RECEIVER DATA OUTPUT (Pins RxDx)						
I_{OH}	High−level output current	Normal mode V_{RxDx} = V_{CCx} − 0.4 V	−8.0	−3.0	−1.0	mA
I_{OL}	Low−level output current	V_{RxDx} = 0.4 V	1.0	6.0	12	mA
BUS LINES (Pins CANHx and CANLx)						
$I_{o(rec)}$	Recessive output current at pins CANHx and CANLx	−27 V < V_{CANHx}, V_{CANLx} < +32 V; Normal mode	−5.0	–	+5.0	mA
I_{LI}	Input leakage current	0 Ω < R(V_{CCx} to GNDx) < 1 MΩ; V_{CANLx} = V_{CANHx} = 5 V	−5.0	0	+5.0	μA
$V_{o(rec)(CANH)}$	Recessive output voltage at pins CANHx	Normal mode, V_{TxDx} = High; R_{LT} and C_{LT} not used	2.0	2.5	3.0	V
$V_{o(rec)(CANL)}$	Recessive output voltage at pins CANLx	Normal mode, V_{TxDx} = High; R_{LT} and C_{LT} not used	2.0	2.5	3.0	V
$V_{o(off)(CANH)}$	Recessive output voltage at pin CANHx	Standby mode; R_{LT} and C_{LT} not used	−0.1	–	+0.1	V
$V_{o(off)(CANL)}$	Recessive output voltage at pin CANLx	Standby mode; R_{LT} and C_{LT} not used	−0.1	–	+0.1	V
$V_{o(off)(CANL)}$	Differential bus output voltage (V_{CANHx} − V_{CANLx})	Standby mode; R_{LT} and C_{LT} not used	−0.2	–	+0.2	V
$V_{o(dom)(CANH)}$	Dominant output voltage at pins CANHx	V_{TxDx} = 0 V; t < $t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	2.75	3.5	4.5	V
$V_{o(dom)(CANL)}$	Dominant output voltage at pins CANLx	V_{TxDx} = 0 V; t < $t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	0.5	1.5	2.25	V

Table 5. ELECTRICAL CHARACTERISTICS
V_{CC1}, V_{CC2} = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF, unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANHx and CANLx)						
$V_{o(dom)(diff)}$	Differential bus output voltage ($V_{CANHx} - V_{CANLx}$)	V_{TxDx} = 0 V; dominant; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(rec)(diff)}$	Differential bus output voltage ($V_{CANHx} - V_{CANLx}$)	V_{TxDx} = High; recessive; no load	−50	0	+50	mV
$V_{o(dom)(diff)\_arb}$	Differential bus output voltage during arbitration ($V_{CANHx} - V_{CANLx}$)	R_{LT} = 2.24kΩ (Note 13)	1.5	–	5.0	V
$V_{o(dom)(sym)}$	Dominant output voltage driver symmetry ($V_{CANHx} + V_{CANLx}$)	R_{LT} = 60Ω; C_1 = 4.7 nF; C_{LT} not used; TxDx = square wave up to 1 MHz	0.9	1.0	1.1	V_{CCx}
$I_{o(sc)(CANH)}$	Short circuit output current at pins CANHx	−3 V < V_{CANHx} < +18 V	−100	–	1.5	mA
$I_{o(sc)(CANL)}$	Short circuit output current at pins CANLx	−3 V < V_{CANLx} < +36 V	−1.5	–	100	mA
$V_{i(rec)(diff)\_NM}$	Differential input voltage range recessive state	Normal mode; −12 V ≤ V_{CANHx}, V_{CANLx} ≤ +12 V; no load	−3.0	–	0.5	V
$V_{i(rec)(diff)\_LP}$		Standby mode; −12 V ≤ V_{CANHx}, V_{CANLx} ≤ +12 V; no load	−3.0		0.4	V
$V_{i(dom)(diff)\_NM}$	Differential input voltage range dominant state	Normal mode; −12 V ≤ V_{CANHx}, V_{CANLx} ≤ +12 V; no load	0.9	–	8.0	V
$V_{i(dom)(diff)\_LP}$		Standby mode; −12 V ≤ V_{CANHx}, V_{CANLx} ≤ +12 V; no load	1.05		8.0	V
$V_{i(diff)(th)\_NORM}$	Differential receiver threshold voltage in normal mode	−12 V ≤ V_{CANLx} ≤ +12 V; −12 V ≤ V_{CANHx} ≤ +12 V	0.5	–	0.9	V
$V_{i(diff)(th)\_NORM\_H}$	Differential receiver threshold voltage in normal mode, extended range	−30 V < V_{CANLx} < +35 V; −30 V < V_{CANHx} < +35 V	0.4	–	1.0	V
$V_{i(diff)(th)\_STDBY}$	Differential receiver threshold voltage in standby mode	−12 V ≤ V_{CANLx} ≤ +12 V; −12 V ≤ V_{CANHx} ≤ +12 V	0.4	–	1.05	V
$R_{i(cm)(CANH)}$	Common−mode input resistance at pin CANHx	−2 V ≤ V_{CANLx} ≤ +7 V; −2 V ≤ V_{CANHx} ≤ +7 V	15	26	37	kΩ
$R_{i(cm)(CANL)}$	Common−mode input resistance at pin CANLx	−2 V ≤ V_{CANLx} ≤ +7 V; −2 V ≤ V_{CANHx} ≤ +7 V	15	26	37	kΩ
$R_{i(cm)(m)}$	Matching between pin CANHx and pin CANLx common mode input resistance	V_{CANHx} = V_{CANLx} = +5 V	−1	0	+1	%
$R_{i(diff)}$	Differential input resistance	−2 V ≤ V_{CANLx} ≤ +7 V; −2 V ≤ V_{CANHx} ≤ +7 V	25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pins CANHx	V_{TxDx} = High; (Note 13)	–	4.5	20	pF
$C_{i(CANL)}$	Input capacitance at pins CANLx	V_{TxDx} = High; (Note 13)	–	4.5	20	pF
$C_{i(diff)}$	Differential input capacitance	V_{TxDx} = High; (Note 13)	–	3.75	10	pF
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature per channel	Junction temperature rising	160	180	200	°C
TIMING CHARACTERISTICS (see Figure 4 and Figure 6)						
$t_{d(TxD-BUSon)}$	Delay TxDx to bus active		–	75	–	ns
$t_{d(TxD-BUSoff)}$	Delay TxDx to bus inactive		–	85	–	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxDx		–	24	–	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxDx		–	32	–	ns
t_{pd_dr}	Propagation delay TxDx to RxDx dominant to recessive transition		50	100	210	ns

Table 5. ELECTRICAL CHARACTERISTICS
V_{CC1}, V_{CC2} = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF, unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see Figure 4 and Figure 6)						
t_{pd_rd}	Propagation delay TxDx to RxDx recessive to dominant transition		50	120	210	ns
$t_{d(stb-nm)}$	Delay standby mode to normal mode		5.0	11	20	μs
t_{wake_filt}	Dominant time for wake−up via bus		0.5	–	5.0	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake−up event	0.5	2.6	6.0	μs
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake−up event	0.5	2.6	6.0	μs
t_{wake_to}	Bus time for wake−up timeout	Standby mode	1.0	–	10	ms
$t_{dom(TxD)}$	TxDx dominant time for timeout	V_{TxDx} = 0 V; Normal mode	1.0	–	10	ms
$t_{Bit(RxD)}$	Bit time on RxDx pin	$t_{Bit(TxD)}$ = 500 ns	400	–	550	ns
		$t_{Bit(TxD)}$ = 200 ns	120	–	220	ns
$t_{Bit(Vi(diff))}$	Bit time on bus (CANHx − CANLx pin)	$t_{Bit(TxD)}$ = 500 ns	435	–	530	ns
		$t_{Bit(TxD)}$ = 200 ns	155	–	210	ns
Δt_{Rec}	Receiver timing symmetry $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Vi(diff))}$;	$t_{Bit(TxD)}$ = 500 ns	−65	–	+40	ns
		$t_{Bit(TxD)}$ = 200 ns	−45	–	+15	ns

12. In the range of 4.5 V to 4.75 V and from 5.25 V to 5.5 V the chip is fully functional; some parameters may be outside of the specification.
13. Values based on design and characterization, not tested in production.

MEASUREMENT SETUPS AND DEFINITIONS

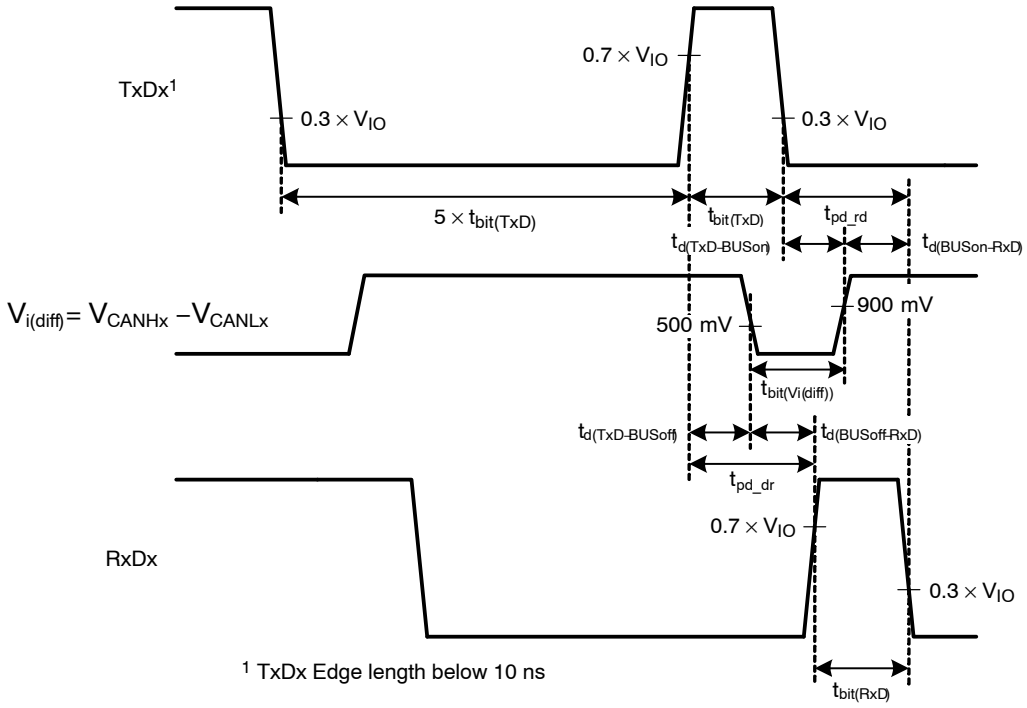


Figure 4. Transceiver Timing Diagram

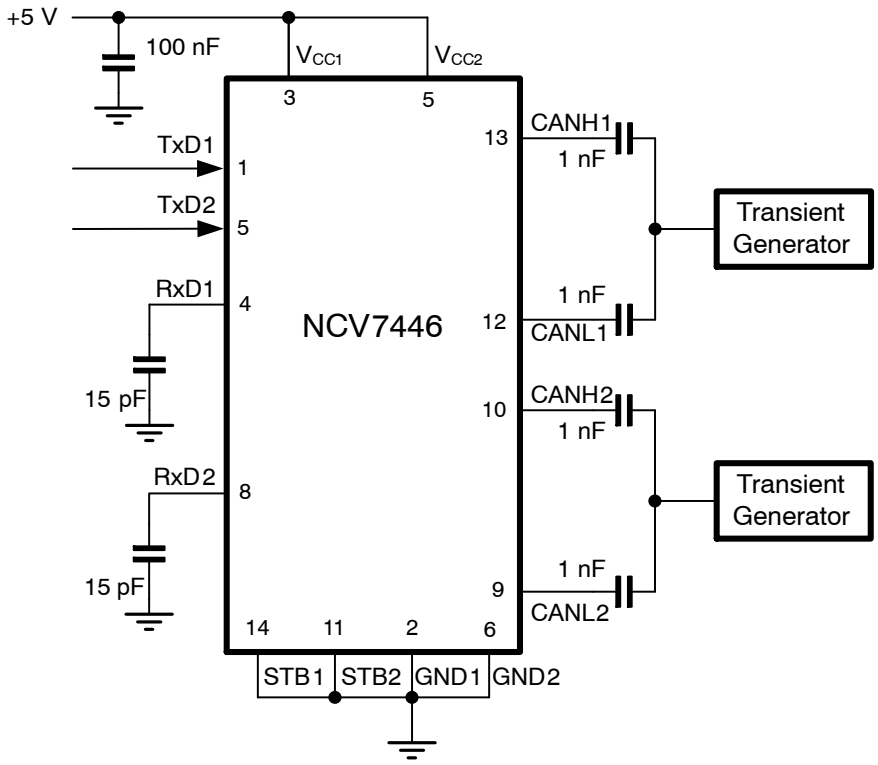


Figure 5. Test Circuit for Automotive Transients

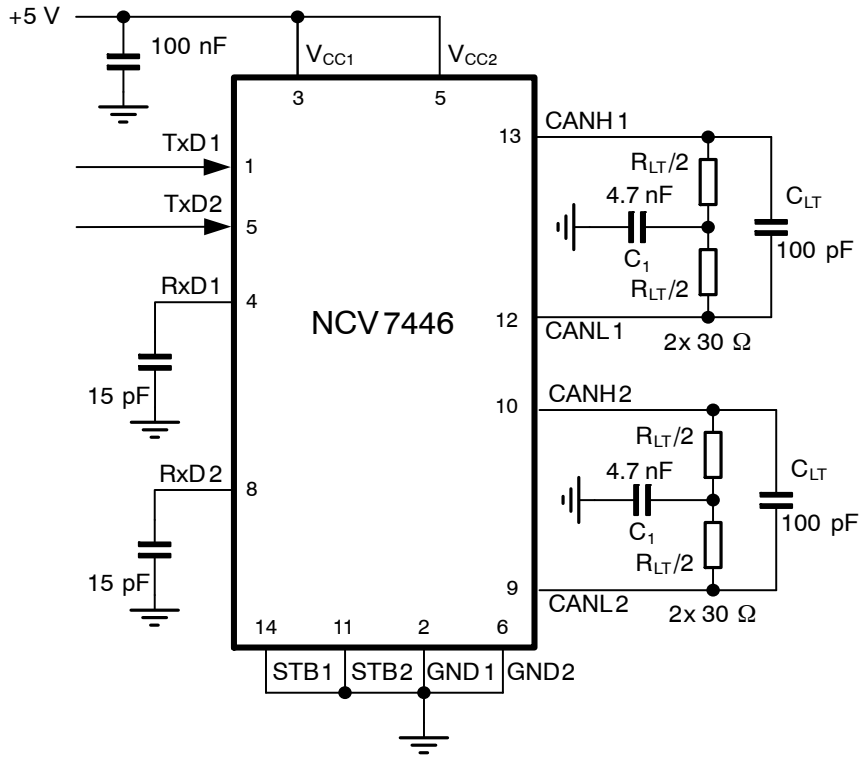


Figure 6. Test Circuit for Timing Characteristics

Table 6. ISO 11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7446 Datasheet
Parameter	**Notation**	**Symbol**
Dominant output characteristics		
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)(diff)}$
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)(diff)\_arb}$
Differential voltage on extended bus load range (optional)	V_{Diff}	$V_{o(dom)(diff)}$
Driver symmetry		
Driver symmetry	V_{SYM}	$V_{o(dom)(sym)}$
Driver output current		
Absolute current on CAN_H	I_{CAN_H}	$I_{o(SC)(CANH)}$
Absolute current on CAN_L	I_{CAN_L}	$I_{o(SC)(CANL)}$
Receiver output characteristics, bus biasing active		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(rec)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(rec)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(rec)(diff)}$
Receiver output characteristics, bus biasing inactive		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(off)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(off)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(off)(dif)}$
Optional transmit dominant timeout		
Transmit dominant timeout, long	t_{dom}	$t_{dom(TxD)}$
Transmit dominant timeout, short	t_{dom}	NA
Static receiver input characteristics, bus biasing active		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)\_NM}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)\_NM}$
Static receiver input characteristics, bus biasing inactive		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)\_LP}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)\_LP}$
Receiver input resistance		
Differential internal resistance	R_{Diff}	$R_{i(diff)}$
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)(CANH)}$ $R_{i(cm)(CANL)}$
Receiver input resistance matching		
Matching a of internal resistance	m_R	$R_{i(cm)(m)}$
Implementation loop delay requirement		
Loop delay	t_{Loop}	t_{pd_rd} t_{pd_dr}
Optional implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s		
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Received recessive bit width @ 2 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}	Δ_{tRec}

Table 6. ISO 11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7446 Datasheet
Parameter	**Notation**	**Symbol**
Optional implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Received recessive bit width @ 5 Mbit/s	Δt_{Rec}	Δt_{Rec}
Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}		
Maximum rating V_{Diff}	V_{Diff}	$V_{CANH-CANL}$
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CANH} V_{CANL}
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
Maximum leakage currents on CAN_H and CAN_L, unpowered		
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_{LI}
Bus biasing control timings		
CAN activity filter time, long	t_{Filter}	t_{wake_filt}
CAN activity filter time, short	t_{Filter}	NA
Wake−up timeout, short	t_{Wake}	NA
Wake−up timeout, long	t_{Wake}	t_{wake_to}
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

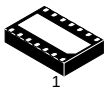
ORDERING INFORMATION

Device	Description	Package	Shipping†
NCV7446MW0R2G	Dual CAN FD Transceiver, High Speed, Low Power	DFNW14 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

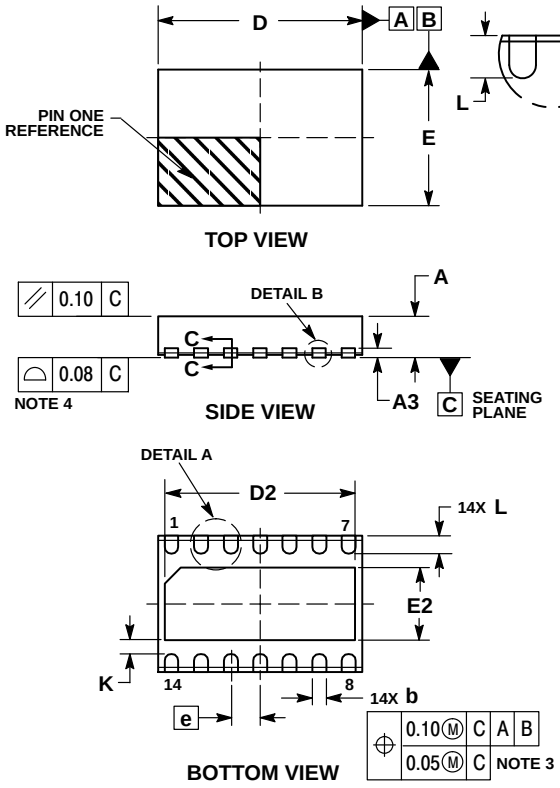
ON Semiconductor®



SCALE 2:1

DFNW14 4.5x3, 0.65P
CASE 507AC
ISSUE D

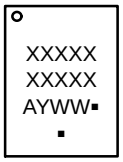
DATE 03 JUL 2018



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	4.40	4.50	4.60
D2	4.13	4.20	4.27
E	2.90	3.00	3.10
E2	1.53	1.60	1.67
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

GENERIC MARKING DIAGRAM*

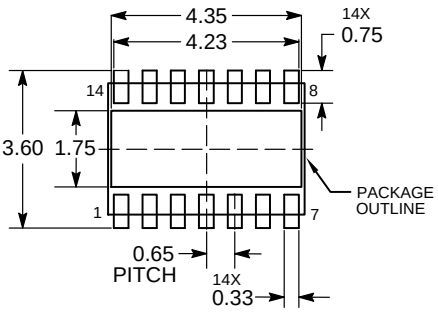


XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14979G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFNW14 4.5x3, 0.65P**	**PAGE 1 OF 1**

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