NCV7710

Door-Module Driver-IC (Lock Driver-IC)

The NCV7710 is a powerful Driver−IC for automotive body control systems. The IC is designed to control lock motor in the door of a vehicle. With the monolithic full−bridge driver stage, the IC is able to control lock motor. The NCV7710 is controlled thru a 24 bit SPI interface with in−frame response.

Features

- Operating Range from 5.5 V to 28 V
- Two High−Side and Two Low−Side Drivers Connected as Half−bridges
  - 2 Half−bridges Iload = 6 A; Rdson = 150 mΩ @ 25°C
- Programmable Soft−Start Function to Drive Loads with Higher Inrush Currents as Current Limitation Value
- Support of PWM Control Frequency Outside the Audible Noise
- Support of Active Freewheeling to Reduce Power Dissipation
- Multiplex Current Sense Analog Output for Advanced Load Monitoring
- Very Low Current Consumption in Standby Mode
- Charge Pump Output to Control an External Reverse Polarity Protection MOSFET
- 24−Bit SPI Interface for Output Control and Diagnostic
- Protection Against Short Circuit, Overvoltage and Over−temperature
- Downwards Pin−to−pin and SPI Registers Compatible with NCV7707
- SSOP36−EP Power Package
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- De−centralized Door Electronic Systems
- Rear Door Electronic Unit
- Body Control Units (BCUs)
- Several H−bridge Applications

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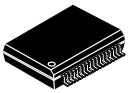
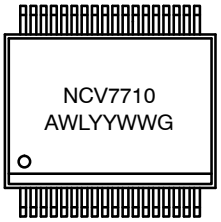


SSOP36−EP
DQ SUFFIX
CASE 940AB

MARKING DIAGRAM



NCV7710 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

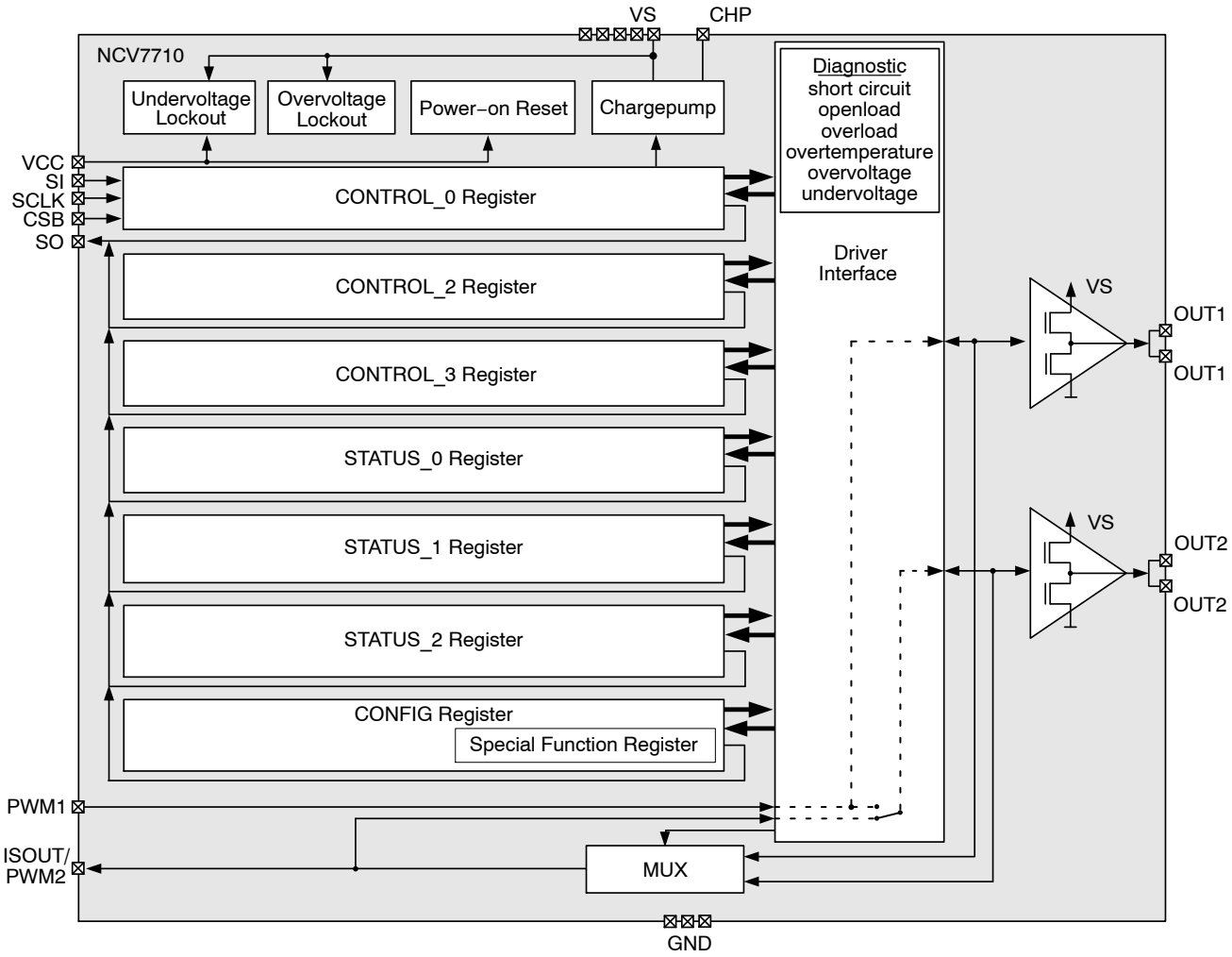


Figure 1. Block Diagram

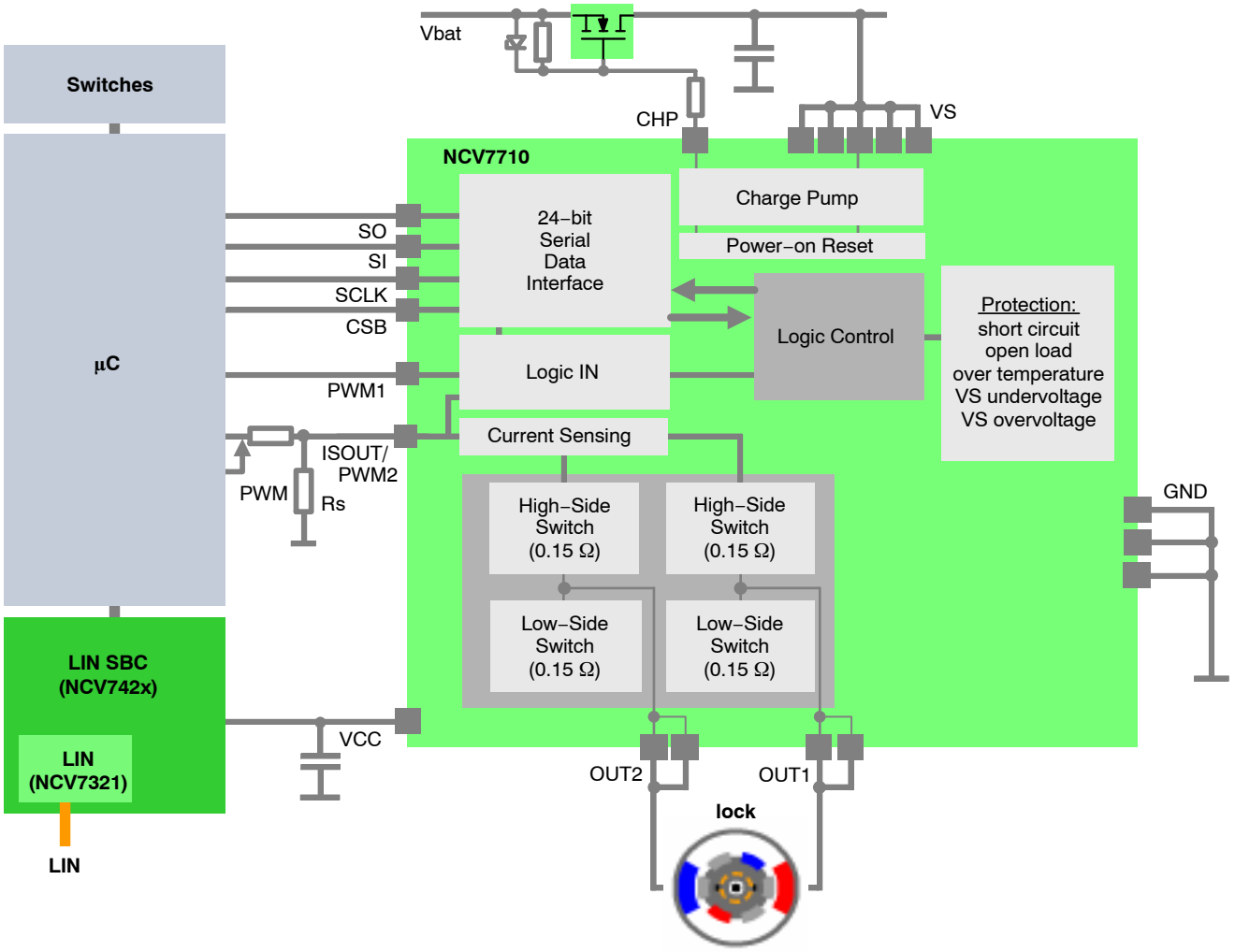


Figure 2. Application Diagram

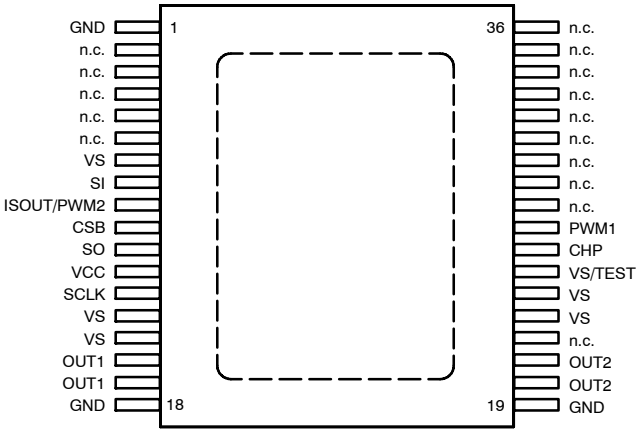


Figure 3. Pin Connections (Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	GND	Ground	Ground Supply (all GND pins have to be connected externally)
2	n.c.		Not connected
3	n.c.		Not connected
4	n.c.		Not connected
5	n.c.		Not connected
6	n.c.		Not connected
7	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
8	SI	Digital Input	SPI interface Serial Data Input
9	ISOUT/PWM2	Digital Input / Analog Output	PWM control Input / Current Sense Output. This pin is a bidirectional pin. Depending on the selected multiplexer bits, an image of the instant current of the corresponding HS stage can be read out. This pin can also be used as PWM control input pin for OUT2.
10	CSB	Digital Input	SPI interface Chip Select
11	SO	Digital Output	SPI interface Serial Data Output
12	VCC	Supply	Logic Supply Input
13	SCLK	Digital Input	SPI interface Shift Clock
14	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
15	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
16	OUT1	Half bridge driver Output	Door Lock Output (has to be connected externally to pin 17)
17	OUT1	Half bridge driver Output	Door Lock Output (has to be connected externally to pin 16)
18	GND	Ground	Ground Supply (all GND pins have to be connected externally)
19	GND	Ground	Ground Supply (all GND pins have to be connected externally)
20	OUT2	Half bridge driver Output	Door Lock Output (has to be connected externally to pin 21)
21	OUT2	Half bridge driver Output	Door Lock Output (has to be connected externally to pin 20)
22	n.c.		Not connected
23	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
24	VS	Supply	Battery Supply Input (all VS pins have to be connected externally)
25	VS/TEST	Supply/Test Input	Test Input, has to be connected to VS in application
26	CHP	Analog Output	Reverse Polarity FET Control Output
27	PWM1	Digital Input	PWM control Input
28	n.c.		Not connected
29	n.c.		Not connected
30	n.c.		Not connected
31	n.c.		Not connected
32	n.c.		Not connected
33	n.c.		Not connected
34	n.c.		Not connected
35	n.c.		Not connected
36	n.c.		Not connected
	Heat slug	Ground	Substrate; Heat slug has to be connected to all GND pins

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
Vs	Power supply voltage – Continuous supply voltage – Transient supply voltage (t < 500 ms, “clamped load dump”)	 –0.3 –0.3	 28 40	V
Vcc	Logic supply	–0.3	5.5	V
Vdig	DC voltage at all logic pins (SO, SI, SCLK, CSB, PWM1)	–0.3	Vcc + 0.3	V
Visout/pwm2	Current monitor output / PWM2 logic input	–0.3	Vcc + 0.3	V
Vchp	Charge pump output (the most stringent value is applied)	–25 Vs – 25	40 Vs + 15	V
Voutx	Static output voltage (OUT1/2)	–0.3	Vs + 0.3	V
Iout1/2	OUT1/2 Output current	–10	10	A
ESD_HBM	ESD Voltage, HBM (Human Body Model); (100 pF, 1500 Ω) (Note 1) – All pins – Output pins OUT1/2 to GND (all unzapped pins grounded)	 –2 –4	 2 4	kV
ESD_CDM	ESD according to CDM (Charge Device Model) (Note 1) – All pins – Corner pins	 –500 –750	 500 750	V
T_J	Operating junction temperature range	–40	150	°C
Tstg	Storage temperature range	–55	150	°C
MSL	Moisture sensitivity level (Note 2)	MSL3		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charge Device Model tested per EIA/JES D22/C101, Field Induced Charge Model
2. For soldering information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, SSOP36−EP, 1−layer PCB Thermal Resistance, Junction−to−Air (Note 3)	49.4	°C/W
$R_{\theta JA}$	Thermal Characteristics, SSOP36−EP, 4−layer PCB Thermal Resistance, Junction−to−Air (Note 4)	24	°C/W

3. Values based on PCB of 76.2 x 114.3 mm, 72 μm copper thickness, 20 % copper area coverage and FR4 PCB substrate.
4. Values based on PCB of 76.2 x 114.3 mm, 72 / 36 μm copper thickness (signal layers / internal planes), 20 / 90 % copper area coverage (signal layers / internal planes) and FR4 PCB substrate.

ELECTRICAL CHARACTERISTICS

4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Vs	Supply voltage	Functional (see Vuv_vs / Vov_vs) Parameter specification	5.5 8		28 18	V
Is(standby)	Supply Current (VS), Standby mode	Standby mode, VS = 16 V, 0 V ≤ VCC ≤ 5.25 V, CSB = VCC, OUT1/2 = floating, SI = SCLK = 0 V, Tj < 85°C (T_J = 150°C)		3 (6)	12 (25)	μA
Is(active)	Supply current (VS), Active mode	Active mode, VS = 16 V, OUT1/2 = floating		6	20	mA
Icc(standby)	Supply Current (VCC), Standby mode	Standby mode, VCC = 5.25 V, SI = SCLK = 0 V, T_J < 85°C (T_J = 150°C)		3 (12)	6 (50)	μA
Icc(active)	Supply current (VCC), Active mode	Active mode, VS = 16 V, OUT1/2 = floating		3.3	8	mA
I(stdby)	Total Standby mode supply current (Is + Icc)	Standby mode, VS = 16 V, T_J < 85°C, CSB = VCC, OUT1/2 = floating		8	18	μA
OVERVOLTAGE AND UNDERVOLTAGE DETECTION						
Vuv_vs(on)	VS Undervoltage detection	VS increasing	5.6		6.2	V
Vuv_vs(off)		VS decreasing	5.2		5.8	V
Vuv_vs(hys)	VS Undervoltage hysteresis	Vuv_vs(on) − Vuv_vs(off)		0.65		V
Vov_vs(off)	VS Overvoltage detection	VS increasing	20		24.5	V
Vov_vs(on)		VS decreasing	18		23.5	V
Vov_vs(hys)	VS Overvoltage hysteresis	Vov_vs(off) − Vov_vs(on)		2		V
Vuv_vcc(off)	VCC Undervoltage detection	VCC increasing			2.9	V
Vuv_vcc(on)		VCC decreasing	2			V
Vuv_vcc(hys)	VCC Undervoltage hysteresis	Vuv_vcc(off) − Vuv_vcc(on)		0.11		V
td_uvov	VS Undervoltage / Overvoltage filter time	Time to set the power supply fail bit UOV_OC in the Global Status Byte	6		100	μs
CHARGE PUMP OUTPUT CHP						
Vchp8	Chargepump Output Voltage	Vs = 8 V, Ichp = −60 μA	Vs + 6	Vs + 9	Vs + 13	V
Vchp10	Chargepump Output Voltage	Vs = 10 V, Ichp = −80 μA	Vs + 8	Vs + 11	Vs + 13	V
Vchp12	Chargepump Output Voltage	VS > 12 V, Ichp = −100 μA	Vs + 9.5	Vs + 11	Vs + 13	V
Ichp	Chargepump Output current	VS = 13.5 V, Vchp = Vs + 10 V	−750		−95	μA

ELECTRICAL CHARACTERISTICS

4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DOOR LOCK OUTPUTS OUT1, OUT2						
Ron_out1,2	On−resistance HS or LS	T_J = 25°C, Iout1,2 = ± 3 A		0.15		Ω
		T_J = 125°C, Iout1,2 = ± 3 A			0.3	Ω
Ioc1,2_hs	Overcurrent threshold HS	T_J > 0°C	−10		−6	A
Ioc1,2_hs_ct	Overcurrent threshold HS	$T_J \leq$ 0°C	−10		−5.75	A
Ioc1,2_ls	Overcurrent threshold LS		6		10	A
Vlim1,2	Vds voltage limitation HS or LS		2		3	V
Iuld1,2_hs	Underload detection threshold HS		−300		−60	mA
Iuld1,2_ls	Underload detection threshold LS		60		300	mA
td_HS1,2(on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT1,2) = 0.9·Vs / 0.1·Vs (on/off)		1.3	3	μs
td_HS1,2(off)	Output delay time, HS Driver off			1.5	3	μs
td_LS1,2(on)	Output delay time, LS Driver on	Time from CSB going high to V(OUT1,2) = 0.1·Vs / 0.9·Vs (on/off)		1	3	μs
td_LS1,2(off)	Output delay time, LS Driver off			1.5	3	μs
tdLH1,2	Cross conduction protection time, low−to−high transition including LS slew−rate			2	7	μs
tdHL1,2	Cross conduction protection time, high−to−low transition including HS slew−rate			5.5	7	μs
Ileak_act_hs1,2	Output HS leakage current, Active mode	V(OUT1,2) = 0 V	−40	−17		μA
Ileak_act_ls1,2	Output pull−down current, Active mode	V(OUT1,2) = VS		150	210	μA
Ileak_stdby_hs1,2	Output HS leakage current, Standby mode	V(OUT1,2) = 0 V	−5			μA
Ileak_stdby_ls1,2	Output pull−down current, Standby mode	V(OUT1,2) = VS, Tj ≥ 25°C V(OUT1,2) = VS, Tj < 25°C		60	120 175	μA μA
td_uld1,2	Underload blanking delay		430		3000	μs
td_old1,2	Overload shutdown blanking delay		5		8	μs
frec1,2L	Recovery frequency, slow recovery mode	CONTROL_3.OCRF = 0		7.4		kHz
frec1,2H	Recovery frequency, fast recovery mode	CONTROL_3.OCRF = 1		14.9		kHz
dVout1,2	Slew rate of HS driver	Vs = 13.5 V, Rload = 4 Ω to GND	9	20	30	V/μs
CURRENT SENSE MONITOR OUTPUT ISOUT/PWM2						
Vis	Current Sense output functional voltage range	VCC = 5 V, Vs = 8−20 V	0		Vcc − 0.5	V
Kis (Note 5)	Current Sense output ratio OUT1/2	K = Iout / Iis, 0 V ≤ Vis ≤ 4.5 V, Vcc = 5 V		13400		
Iis,acc (Notes 6, 7)	Current Sense output accuracy OUT1/2	0.3 V ≤ Vis ≤ 4.5 V, Vcc = 5 V Iout1/2 = 0.5−5.9 A	−7% − 4% FS		7% + 4% FS	
tis_blank	Current Sense blanking time	CONTROL_2.OUTx_PWM = 0	50		65	μs
		CONTROL_2.OUTx_PWM = 1	5		10	
tis	Current Sense settling time	0 V to FSR (full scale range)		230	265	μs

5. Kis trimmed at 150°C at higher value of spec range to be more centered over temp range.
6. Current sense output accuracy = Isout−Isout_ideal relative to Isout_ideal
7. FS (Full scale) = Ioutmax/Kis

ELECTRICAL CHARACTERISTICS

4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS CSB, SCLK, PWM1/2, SI						
Vinl	Input low level	Vcc = 5 V			0.3·Vcc	V
Vinh	Input high level		0.7·Vcc			V
Vin_hyst	Input hysteresis		500			mV
Rcsb_pu	CSB pull−up resistor	Vcc = 5 V, 0 V < Vcsb < 0.7·Vcc	30	120	250	kΩ
Rsclk_pd	SCLK pull−down resistor	Vcc = 5 V, Vsclk = 1.5 V	30	60	220	kΩ
Rsi_pd	SI pull−down resistor	Vcc = 5 V, Vsi = 1.5 V	30	60	220	kΩ
Rpwm1_pd	PWM1 pull−down resistor	Vcc = 5 V Vpwm1 = 1.5 V	30	60	220	kΩ
Rpwm2_pd	PWM2 pull−down resistor	Vcc = 5 V, Vpwm2 = 1.5 V, current sense disabled	30	60	220	kΩ
Ileak_isout	Output leakage current	Vpwm2 = 0 V, current sense enabled	−1		1	μA
Ccsb/sclk/pwm1/2	Pin capacitance	0 V < Vcc < 5.25 V (Note 8)			10	pF
DIGITAL INPUTS CSB, SCLK, SI; TIMING						
tsclk	Clock period	Vcc = 5 V		1000		ns
tsclk_h	Clock high time		115			ns
tsclk_l	Clock low time		115			ns
tset_csb	CSB setup time, CSB low before rising edge of SCLK		400			ns
tset_sclk	SCLK setup time, SCLK low before rising edge of CSB		400			ns
tset_si	SI setup time		200			ns
thold_si	SI hold time		200			ns
tr_in	Rise time of input signal SI, SCLK, CSB				100	ns
tf_in	Fall time of input signal SI, SCLK, CSB				100	ns
tcsb_hi_stdby	Minimum CSB high time, switching from Standby mode	Transfer of SPI−command to input register, valid before tsact mode transition delay expires		5	10	μs
tcsb_hi_min	Minimum CSB high time, Active mode			2	4	μs

8. Values based on design and/or characterization.

ELECTRICAL CHARACTERISTICS

4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT SO						
Vsol	Output low level	Iso = 5 mA			0.2·Vcc	V
Vsoh	Output high level	Iso = −5 mA	0.8·Vcc			V
Ileak_so	Tristate leakage current	Vcsb = Vcc, 0 V < Vso < Vcc	−10		10	μA
Cso	Tristate input capacitance	Vcsb = Vcc, 0 V < Vcc < 5.25 V (Note 9)			10	pF
DIGITAL OUTPUT SO; TIMING						
tr_so	SO rise time	Cso = 100 pF		80	140	ns
tf_so	SO fall time	Cso = 100 pF		50	100	ns
ten_so_tril	SO enable time from tristate to low level	Cso = 100 pF, Iload = 1 mA, pull−up load to VCC		100	250	ns
tdis_so_ltri	SO disable time from low level to tristate	Cso = 100 pF, Iload = 4 mA, pull−up load to VCC		380	450	ns
ten_so_trih	SO enable time from tristate to high level	Cso = 100 pF, Iload = −1 mA, pull−down load to GND		100	250	ns
tdis_so_htri	SO disable time from high level to tristate	Cso = 100 pF, Iload = −4 mA, pull−down load to GND		380	450	ns
td_so	SO delay time	Vso < 0.3·Vcc, or Vso > 0.7·Vcc, Cso = 100 pF		50	250	ns

9. Values based on design and/or characterization.

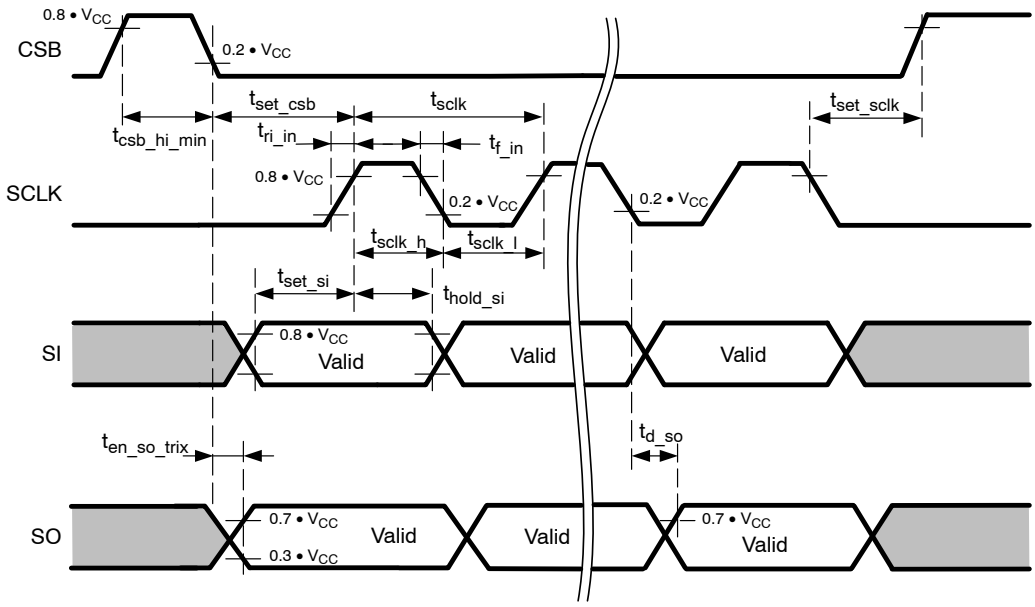


Figure 4. SPI Signals Timing Parameters

ELECTRICAL CHARACTERISTICS

4.5 V < Vcc < 5.25 V, 8 V < Vs < 18 V, −40°C < Tj < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
THERMAL PROTECTION						
Tjtw_on	Temperature warning threshold	Junction temperature	140		160	°C
Tjtw_hys	Thermal warning hysteresis			5		°C
Tjsd_on	Thermal shutdown threshold, T_J increasing	Junction temperature	160		180	°C
Tjsd_off	Thermal shutdown threshold, T_J decreasing	Junction temperature	160			°C
Tjsd_hys	Thermal shutdown hysteresis			5		°C
Tjsdtw_delta	Temperature difference between warning and shutdown threshold			20		°C
td_tx	Filter time for thermal warning and shutdown	TW / TSD Global Status bits	10		100	μs
OPERATING MODES TIMING						
tact	Time delay for mode change from Unpowered mode into Standby mode	SPI communication ready after VCC reached Vuv_vcc(off) threshold			30	μs
tsact	Time delay for mode change from Standby mode into Active mode	Time until output drivers are enabled after CSB going to high and CONTROL_0.MODE = 1		190	360	μs
tacts	Time delay for mode change from Active mode into Standby mode via SPI	Time until output drivers are disabled after CSB going to high and CONTROL_0.MODE = 0			8	μs

DETAILED OPERATING AND PIN DESCRIPTION

General

The NCV7710 provides two half−bridge drivers. Strict adherence to integrated circuit die temperature is necessary, with a static maximum die temperature of 150°C. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port. A SPI−controlled mode control provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Supply Concept

Power Supply Scheme − VS and VCC

The Vs power supply voltage is used to supply the half bridges and the high−side drivers. An all−internal chargepump is implemented to provide the gate−drive voltage for the n−channel type high−side transistors. The VCC voltage is used to supply the logic section of the IC, including the SPI interface.

Due to the independent logic supply voltage the control and status information will not be lost in case of a loss of Vs supply voltage. The device is designed to operate inside the specified parametric limits if the VCC supply voltage is within the specified voltage range (4.5 V to 5.25 V). Between the operational level and the VCC undervoltage threshold level (Vuv_VCC) it is guaranteed that the device remains in a safe functional state without any inadvertent change to logic information.

Device / Module Ground Concept

The heat slug is not hard−connected to internal GND rail. It has to be connected externally.

Power Up/Down Control

In order to prevent uncontrolled operation of the device during power/up down, an undervoltage lockout feature is implemented. Both supply voltages (VCC and Vs) are monitored for undervoltage conditions supporting a safe power−up transition. When Vs drops below the undervoltage threshold Vuv_vs(off) (Vs undervoltage threshold) both output stages are switched to high−impedance state and the global status bit UOV_OC is set. This bit is a multi information bit in the Global Status Byte which is set in case of overcurrent, Vs over− and undervoltage. In case of undervoltage the status bit STATUS_2.VSUV is set, too.

Bit CONTROL_3.OVUVR (Vs under−/overvoltage recovery behavior) can be used to select the desired recovery behavior after a Vs under−voltage event. In case of OVUVR = 0, both output stages return to their programmed state as soon as Vs recovers back to its normal operating range. If OVUVR is set, the automatic recovery function is disabled thus the output stages will remain in high−impedance condition until the status bits have been cleared by the microcontroller. To avoid high current oscillations in case of output short to GND and low Vs voltage conditions, it is recommended to disable the Vs−auto−recovery by setting OVUVR = 1.

Chargepump

In Standby mode, the chargepump is disabled. After enabling the device by setting bit CONTROL_0.MODE to active (1), the internal oscillator is started and the voltage at the CHP output pin begins to increase. The output drivers are enabled after a delay of tsact once MODE was set to active.

Driver Outputs

Output PWM Control

For both−half bridge outputs the device features the possibility to logically combine the SPI−setting with a PWM signal that can be provided to the inputs PWM1 and ISOUT/PWM2, respectively. Each of the outputs has a fixed PWM signal assigned which is shown in Table 1. The PWM modulation is enabled by the respective bits in the control registers (CONTROL_2.OUTx_PWMx). In case of using pin ISOUT/PWM2, the application design has to take care of either disabling the current sense feature or to provide sufficient overdrive capability to maintain proper logic input levels for the PWM input. To improve power performances, fast PWMing up to 30 kHz is foreseen.

By setting PWM_SWAP bit in the configurations register CONFIG it is possible to map both outputs to PWM1.

This is useful if PWM control and current sensing is required at OUT1 and OUT2.

Table 1. PWM CONTROL SCHEME

	PWM Control Input	
Output	CONFIG.PWM_SWAP = 0	CONFIG.PWM_SWAP = 1
OUT1	PWM1	PWM1
OUT2	PWM2	PWM1

In case of using pin ISOUT/PWM2, the application design can decide:

- To control all PWM via PWM1 by setting bit CONFIG.PWM_SWAP to 1
- or to disable the current sense feature
- or to provide sufficient overdrive capability to maintain proper logic input levels for the PWM input

Due to the used external network connected between microcontroller and ISOUT/PWM2 pin, the digital input signal cannot be guaranteed to be a clean digital high or low level when the current output ISOUT is activated. During Current sense the PWM2 digital input stays functional (the input to the digital is not gated), but the internal pull down on PWM2 is disabled when CS is activated.

Table 2. OUT1/2 CONTROL AND FREEWHEELING SELECTION

CONTROL_2	PWM input pin	CONTROL_0		Output pin state
OUTx_PWM1/2	PWM1/2	OUTx_HS	OUTx_LS	OUTx
0 (PWM disabled)	X	0	0	High Impedance
		0	1	L
		1	0	H
		1	1	High Impedance
1 (PWM enabled)	0	0	0	High Impedance
		0	1	High Impedance
		1	0	High Impedance
		1	1	L
	1	0	0	High Impedance
		0	1	L
		1	0	H
		1	1	H

Programmable Soft−start Function to Drive Loads with Inrush Current Behavior

Loads with startup currents higher than the overcurrent limits (e.g. block current of motors) can be driven using the programmable soft−start function (Overcurrent auto−recovery mode). Each output driver provides a corresponding overcurrent recovery bit (CONTROL_2.OCRx) to control the output behavior in case of a detected overcurrent event. If auto−recovery is enabled, the device automatically re−enables the output after a programmable recovery time. For both half−bridge outputs, the recovery frequency can be selected via SPI. It is recommended to only enable auto−recovery for a minimum amount of time to drive the connected load into a steady state condition. After turning off the auto−recovery function, the respective channel is automatically disabled if the overload condition still persists.

Inductive Loads

Each half bridge (OUT1/2) is built by internally connected low−side and high−side N−MOS transistors. Due to the built−in body diodes of the output transistors, inductive loads can be driven at the outputs without external free−wheeling diodes.

Current Sensing

Current Sense Output / PWM2 Input (bidirectional pin ISOUT/PWM2)

The current sense output allows a more precise analysis of the actual state of the load rather than the basic detection of an under− or overload condition. The sense output provides an image of the actual load current at the selected high side driver transistor. The current monitor function is available for both high current half−bridge outputs (OUT1/2).

The current sense ratio is fixed to 1/13400. To prevent from false readouts, the signal at pin ISOUT is blanked after switching on the driver until correct settlement of the circuitry (max. 65 μs). Bits CONTROL_3.IS[2:0] are used to select the output to be multiplexed to the current sense output.

If the current sense feature is used in combination with PWM control, the device will change the slew rate of the output signal to a faster slope. Also the blanking time is shortened to 5−10 μs.

The NCV7710 provides a sample−and−hold functionality for the current sense output to enable precise and simple load current diagnostics even during PWM operation of the respective output. While in active high−side output state, the current provided at ISOUT reflects a (low−pass−filtered) image of the actual output current, the IS−output current is sampled and held constant as soon as the HS output transistor is commanded off via PWM (low−side or high−impedant). In case no previous current information is available in the Sample−and−hold stage (current sense channel changed while actual channel is commanded off) the sample stage is reset so that it reflects zero output current.

Diagnostic Functions

All diagnostic functions (overcurrent, underload, power supply monitoring, thermal warning and thermal shutdown) are internally filtered. The failure condition has to be valid for the minimum specified filtering time (td_old, td_uld, td_uvov and td_tx) before the corresponding status bit in the status register is set. The filter function is used to improve the noise immunity of the device. The undercurrent and temperature warning functions are intended for information purpose and do not affect the state of the output drivers. An overcurrent condition disables the corresponding output driver while a thermal shutdown event disables all outputs into high impedance state. Depending on the setting of the overcurrent recovery bits in the input register, the driver can either perform an auto−retry or remain latched off until the microcontroller clears the corresponding status bits. Overtemperature shutdown is latch−off only, without auto−retry functionality.

Overvoltage / Undervoltage Shutdown

If the supply voltage Vs rises above the switch off voltage Vov_vs(off) or falls below Vuv_vs(off), all output transistors are switched to high−impedance state and the global status bit UOV_OC (multi information) is set. The status flag STATUS_2.VSOV, resp. STATUS_2.VSUV is set, too, to log the over−/under−voltage event. The bit CONTROL_3.OVUVR can be used to determine the recovery behavior once the Vs supply voltage gets back into the specified nominal operating range. OVUVR = 0 enables auto−recovery, with OVUVR = 1 the output stages remain in high impedance condition until the status flags have been cleared. Once set, STATUS2.VSOV / VSUV can only be reset by a read&clear access to the status register STATUS_2.

Thermal Warning and Overtemperature Shutdown

The device provides a dual−stage overtemperature protection. If the junction temperature rises above Tjtw_on, a temperature warning flag (TW) is set in the Global Status Byte and can be read via SPI. The control software can then react onto this overload condition by a controlled disable of individual outputs. If however the junction temperature reaches the second threshold Tjsd_on, the thermal shutdown bit TSD is set in the Global Status Byte and all output stages are switched into high impedance state to protect the device. The minimum shutdown delay for overtemperature is td_tx. The output channels can be re−enabled after the device cooled down and the TSD flag has been reset by the microcontroller by setting CONTROL_0.MODE = 0.

Openload (Underload) Detection

The openload detection monitors the load current in the output stage while the transistor is active. If the load current is below the openload detection threshold for at least td_uld, the corresponding bit (ULDx) is set in the status registers STATUS_1. The status of the output remains unchanged. Once set, ULDx remains set regardless of the actual load condition. It has to be reset by a read&write access to the corresponding status register.

Overload Detection

An overcurrent condition is indicated by the flag (UOV_OC) in the Global Status Byte after a filter time of at least td_old. The channel dependent overcurrent flags are set in the status registers (STATUS_0.OCx) and the corresponding driver is switched into high impedance state to protect the device. Each low−side and high−side driver stage provides its own overcurrent flag. Resetting this overcurrent flag automatically re−enables the respective output (provided it is still enabled thru the Control register). If the over current recovery function is enabled, the internal chip logic automatically resets the overcurrent flag after a fixed delay time, generating a PWM modulated current with a programmable duty cycle. Otherwise the status bits have to be cleared by the microcontroller by a read&clear access to the corresponding status register.

Cross−current Protection

The half−bridges are protected against cross−currents by internal circuitry. If one driver is turned off (LS or HS), the activation of the other driver of the same output will be automatically delayed by the cross current protection mechanism until the active driver is safely turned off.

Mode Control

Wake−up and Mode Control

Two different modes are available:

- Active mode
- Standby mode

After power−up of VCC the device starts in Standby mode. Pulling the chip−select signal CSB to low level causes the device to change into Active mode (analog part active).

After at least 10 μs delay, the first SPI communication is valid and bit CONTROL_0.MODE can be used to set the desired mode of operation. If bit MODE remains reset (0), the device returns to the Standby mode after an internal delay of max. 8 μs, clearing all register content and setting all output stages into high impedance state.

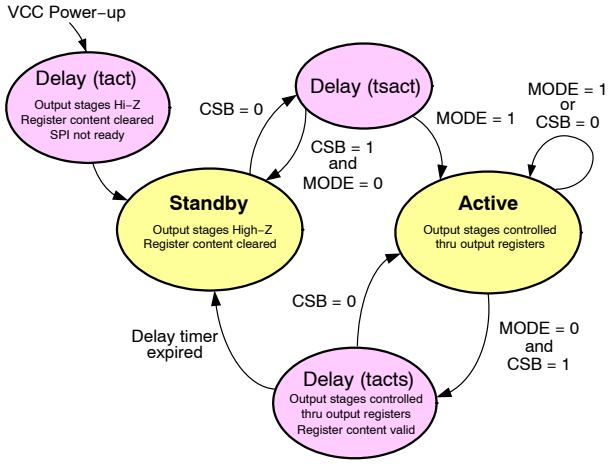


Figure 5. Mode Transitions Diagram

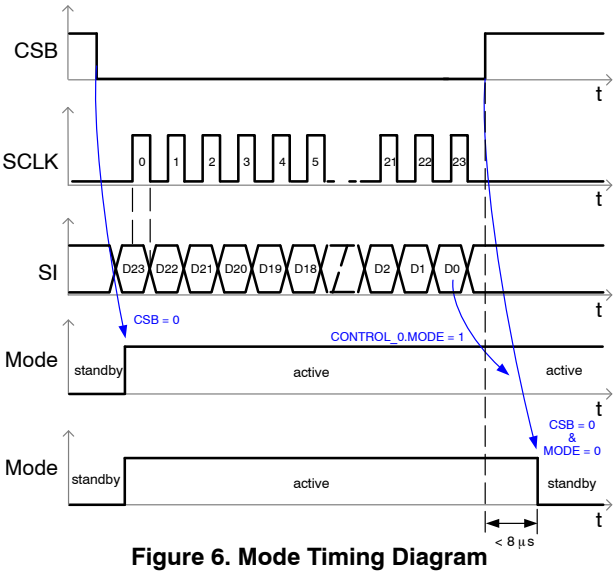


Figure 6. Mode Timing Diagram

SPI Control

General Description

The 4−wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7710 and the application's microcontroller. The NCV7710 always operates in slave mode whereas the controller provides the master function. A SPI access is performed by applying an active−low slave select signal at CSB. SI is the data input, SO the data output. The SPI master provides the clock to the NCV7710 via the SCLK input. The digital input data is sampled at the rising edge at SCLK. The data output SO is in high impedance state (tri−state) when CSB is high. To readout the global error flag without sending a complete SPI frame, SO indicates the corresponding value as soon as CSB is set to active. With the first rising edge at SCLK after the high−to−low transition of CSB, the content of the selected register is transferred into the output shift register.

The NCV7710 provides three control registers (CONTROL_0/2/3), three status registers (STATUS_0/1/2) and one general configuration register (CONFIG). Each of these register contains 16−bit data, together with the 8−bit frame header (access type, register address), the SPI frame length is therefore 24 bits. In addition to the read/write accessible registers, the NCV7710 provides five 8−bit ID registers (ID_HEADER, ID_VERSION, ID_CODE1/2 and ID_SPI−FRAME) with 8−bit data length. The content of these registers can still be read out by a 24−bit access, the data is then transferred in the MSB section of the data frame.

SPI Frame Format

Figure 7 shows the general format of the NCV7710 SPI frame.

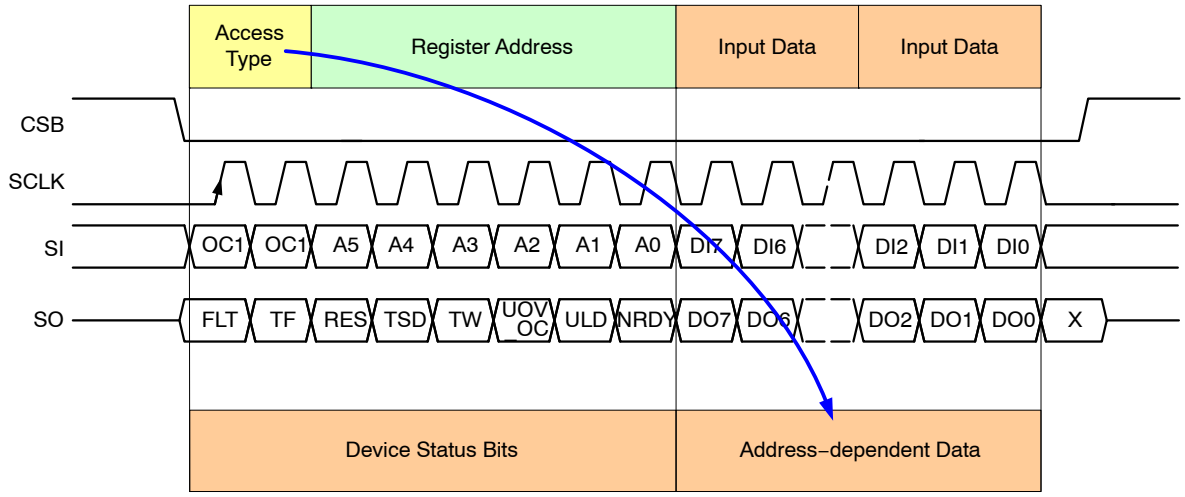


Figure 7. SPI Frame Format

24−bit SPI Interface

Both 24−bit input and output data are MSB first. Each SPI−input frame consists of a command byte followed by two data bytes. The data returned on SO within the same frame always starts with the global status byte. It provides general status information about the device. It is then followed by 2 data bytes (in−frame response) which content depends on the information transmitted in the command byte. For write access cycles, the global status byte is followed by the previous content of the addressed register.

Chip Select Bar (CSB)

CSB is the SPI input pin which controls the data transfer of the device. When CSB is high, no data transfer is possible and the output pin SO is set to high impedance. If CSB goes low, the serial data transfer is allowed and can be started. The communication ends when CSB goes high again.

Serial Clock (SCLK)

If CSB is set to low, the communication starts with the rising edge of the SCLK input pin. At each rising edge of SCLK, the data at the input pin Serial IN (SI) is latched. The data is shifted out thru the data output pin SO after the falling edges of SCLK. The clock SCLK must be active only within the frame time, means when CSB is low. The correct transmission is monitored by counting the number of clock pulses during the communication frame. If the number of SCLK pulses does not correspond to the frame width indicated in the SPI−frame−ID (Chip ID Register, address 3Eh) the frame will be ignored and the communication failure bit "TF" in the global status byte will be set. Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSB signal of the connected ICs is recommended.

Serial Data In (SI)

During the rising edges of SCLK (CSB is low), the data is transferred into the device thru the input pin SI in a serial way. The device features a stuck−at−one detection, thus upon detection of a command = FFFFFFh, the device will be forced into the Standby mode. All output drivers are switched off.

Serial Data Out (SO)

The SO data output driver is activated by a logical low level at the CSB input and will go from high impedance to a low or high level depending on the global status bit, FLT (Global Error Flag). The first rising edge of the SCLK input after a high to low transition of the CSB pin will transfer the content of the selected register into the data out shift register. Each subsequent falling edge of the SCLK will shift the next bit thru SO out of the device.

Command Byte / Global Status Byte

Each communication frame starts with a command byte (Table 3). It consists of an operation code (OP[1:0], Table 4) which specifies the type of operation (Read, Write, Read & Clear, Readout Device Information) and a six bit address (A[5:0], Table 5). If less than six address bits are required, the remaining bits are unused but are reserved. Both Write and Read mode allow access to the internal registers of the device. A “Read & Clear”−access is used to read a status register and subsequently clear its content. The “Read Device Information” allows to read out device related information such as ID−Header, Product Code, Silicon Version and Category and the SPI−frame ID. While receiving the command byte, the global status byte is transmitted to the microcontroller. It contains global fault information for the device, as shown in Table 7.

ID Register

Chip ID Information is stored in five special 8−bit ID registers (Table 6). The content can be read out at the beginning of the communication.

Table 3. COMMAND BYTE / GLOBAL STATUS BYTE STRUCTURE

Bit	Command Byte (IN) / Global Status Byte (OUT)							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NCV7710 IN	OP1	OP0	A5	A4	A3	A2	A1	A0
NCV7710 OUT	FLT	TF	RESB	TSD	TW	UOV_OC	ULD	NRDY
Reset Value	1	0	0	0	0	0	0	1

Table 4. COMMAND BYTE, ACCESS MODE

OP1	OP0	Description
0	0	Write Access (W)
0	1	Read Access (R)
1	0	Read and Clear Access (RC)
1	1	Read Device ID (RDID)

Table 5. COMMAND BYTE, REGISTER ADDRESS

A[5:0]	Access	Description	Content
00h	R/W	Control Register CONTROL_0	Device mode control, Bridge outputs control
02h	R/W	Control Register CONTROL_2	Bridge outputs recovery control, PWM enable
03h	R/W	Control Register CONTROL_3	Current Sense selection
10h	R/RC	Status Register STATUS_0	Bridge outputs Overcurrent diagnosis
11h	R/RC	Status Register STATUS_1	Bridge outputs Underload diagnosis
12h	R/RC	Status Register STATUS_2	Vs Over− and Undervoltage
3Fh	R/W	Configuration Register CONFIG	Mask bits for global fault bits, PWM mapping

Table 6. CHIP ID INFORMATION

A[5:0]	Access	Description	Content
00h	RDID	ID header	4300h
01h	RDID	Version	0000h
02h	RDID	Product Code 1	7700h
03h	RDID	Product Code 2	0A00h
3Eh	RDID	SPI−Frame ID	0200h

Table 7. GLOBAL STATUS BYTE CONTENT

FLT	**Global Fault Bit**	
0	No fault Condition	Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB inverted). It is reflected via the SO pin while CSB is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSB is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set. Signals TW and ULD can be masked.
1	Fault Condition	
TF	**SPI Transmission Error**	
0	No Error	If the number of clock pulses within the previous frame was unequal 0 (FLT polling) or 24. The frame was ignored and this flag was set.
1	Error	
RESB	**Reset Bar (Active low)**	
0	Reset	Bit is set to “0” after a Power−on−Reset or a stuck−at−1 fault at SI (SPI−input data = FFFFFFh) has been detected. All outputs are disabled.
1	Normal Operation	
TSD	**Overtemperature Shutdown**	
0	No Thermal Shutdown	Thermal Shutdown Status indication. In case of a Thermal Shutdown, all output drivers including the charge pump output are deactivated (high impedance). The TSD bit has to be cleared thru a SW reset to reactivate the output drivers and the chargepump output.
1	Thermal Shutdown	
TW	**Thermal Warning**	
0	No Thermal Warning	This bit indicates a pre−warning level of the junction temperature. It is maskable by the Configuration Register (CONFIG.NO_TW).
1	Thermal Warning	
UOV_OC	**VS Monitoring, Overcurrent Status**	
0	No Fault	This bit represents a logical OR combination of under−/overvoltage signals (VS) and overcurrent signals.
1	Fault	
ULD	**Underload**	
0	No Underload	This bit represents a logical OR combination of all underload signals. It is maskable by the Configuration Register (CONFIG.NO_ULDx).
1	Underload	
NRDY	**Not Ready**	
0	Device Ready	After transition from Standby to Active mode, an internal timer is started to allow the internal chargepump to settle before any outputs can be activated. This bit is cleared automatically after the startup is completed.
1	Device Not Ready	

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	RW	RW	RW	RW	–	–	–	–	–	RW
Bit name	0	0	0	0	0	0	HS1	LS1	HS2	LS2	0	0	0	0	0	MODE
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	HSx	LSx		Description	Remark
HS/LS Outputs Control	0	0	default	OUTx High impedance	If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_2 register, the HS output is activated if PWM1 (PWM2) input signal is high, LS is activated otherwise. Since OUT1 and OUT2 are half−bridge outputs, activating both HS and LS at the same time is prevented by internal logic.
	0	1		LSx enabled	
	1	0		HSx enabled	
	1	1		OUTx High impedance / LS or HS enabled in PWM	

	MODE		Description	Remark
Mode Control	0	default	Standby	If MODE is set, the device is switched to Active mode. Resetting MODE forces the device to transition into Standby mode, all internal memory is cleared, all output stages are switched into their default state (off).
	1		Active	

CONTROL_2 Register

Address: 02h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	RW	RW	–	–	–	–	–	–	RW	RW	–	–	–
Bit name	0	0	0	OCR1	OCR2	0	0	0	0	0	0	OUT1 PWM1	OUT2 PWM2	0	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCRx		Description	Remark
Overcurrent Recovery	0	default	Overcurrent Recovery disabled	During an overcurrent event the overcurrent status bit STATUS_0.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF).
	1		Overcurrent Recovery enabled	

	OUTx PWM		Description	Remark
PWM1/2 Selection	0	default	PWMx not selected	For the outputs it is possible to select the PWM input pins PWM1 or PWM2. In this case the dedicated output (selected in CONTROL_0 register) is on if the PWM input signal is high. By default, OUT2 is controlled by PWM2, OUT1 is controlled by PWM1. By setting CONFIG.PWM_SWAP bit, both outputs are mapped to PWM1
	1		PWMx selected	

CONTROL_3 Register

Address: 03h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	–	–	–	–	RW	RW	–	RW	RW	RW
Bit name	0	0	0	0	0	0	0	0	0	0	OCRF	OVUVR	0	IS2	IS1	IS0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCRF		Description	Remark
Overcurrent Recovery Frequency Selection	0	default	Slow Overcurrent recovery mode	If the overcurrent recovery bit is set, the output will be switched on automatically after a delay time.
	1		Fast Overcurrent recovery mode	

	OVUVR		Description	Remark
Over−/Under−voltage Recovery	0	default	Over− and undervoltage recovery function enabled	If the OV/UV recovery is disabled by setting OVUVR=1, the status register STATUS_2 bits VSOV or VSUV have to be cleared after an OV/UV event to reactivate the outputs.
	1		No over− and undervoltage recovery	

	IS2	IS1	IS0	Description	Remark
Current Sensing Selection	0	0	0	current sensing deactivated	The current in high−side power stages can be monitored at the bidirectional multifunctional pin ISOUT/PWM2. This pin is a multifunctional pin and can be activated as output by setting the current selection bits IS[2:0]. The selected high−side output will be multiplexed to the output ISOUT.
	0	0	1	current sensing deactivated	
	0	1	0	current sensing deactivated	
	0	1	1	OUT1	
	1	0	0	OUT2	
	1	0	1	current sensing deactivated	
	1	1	0	current sensing deactivated	
	1	1	1	current sensing deactivated	

STATUS_0 Register

Address: 10h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	R/RC	R/RC	R/RC	R/RC	–	–	–	–	–	–
Bit name	0	0	0	0	0	0	OC HS1	OC LS1	OC HS2	OC LS2	0	0	0	0	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCx	Description	Remark
Overcurrent Detection	0	No overcurrent detected	During an overcurrent event in one of the HS or LS, the belonging overcurrent status bit STATUS_0.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF). If the overcurrent recovery bit is not set the microcontroller has to clear the OC failure bit and to reactivate the output stage again.
	1	Overcurrent detected	

STATUS_1 Register

Address: 11h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	R/RC	R/RC	R/RC	R/RC	–	–	–	–	–	–
Bit name	0	0	0	0	0	0	ULD HS1	ULD LS1	ULD HS2	ULD LS2	0	0	0	0	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	ULDx	Description	Remark
Underload Detection	0	No underload detected	For each output stage an underload status bit ULD is available. The underload detection is done in “on−mode”. If the load current is below the undercurrent detection threshold for at least td_uld , the corresponding underload bit ULDx is set. If an ULD event occurs the global status bit ULD will be set. With setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general.
	1	Underload detected	

STATUS_2 Register

Address: 12h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	–	–	–	–	–	–	R/RC	R/RC	–	–
Bit name	0	0	0	0	0	0	0	0	0	0	0	0	VSUV	VSOV	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	VSUV	Description	Remark
Vs Undervoltage	0	No undervoltage detected	In case of an Vs undervoltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set. By default the output stages will be reactivated automatically after Vs is recovered unless the control bit CONTROL_3.OVUVR is set. If this is the case (OVUVR=1) the bit VSUV has to be cleared after an UV event.
	1	Undervoltage detected	

	VSOV	Description	Remark
Vs Overvoltage	0	No overvoltage detected	In case of an Vs overvoltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set. By default the output stages will be reactivated automatically after Vs is recovered unless the control bit CONTROL_3.OVUVR is set. If this is the case (OVUVR=1) the bit VSOV has to be cleared after an OV event.
	1	Overvoltage detected	

CONFIG Register

Address: 3Fh

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	–	–	–	–	–	–	–	–	RW	–	RW	RW
Bit name	0	0	0	0	0	0	0	0	0	0	0	0	NO_TW	0	NO_ULD OUTn	PWM SWAP
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	NO_TW		Description	Remark
No Thermal Warning Flag	0	default	Thermal warning flag active	The global thermal warning bit TW can be deactivated.
	1		No thermal warning flag active	

	NO_ULD OUTn		Description	Remark
Global Undeload Flag OUTn	0	default	Global underload flag active	By setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general.
	1		No global underload flag active	

	PWM_SWAP		Description	Remark
OUT2 PWM Mapping	0	default	OUT2 mapped to PWM2	By setting PWM_SWAP bit, both outputs are mapped to PWM1
	1		OUT2 mapped to PWM1	

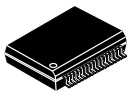
ORDERING INFORMATION

Device	Package	Shipping†
NCV7710DQR2G	SSOP36−EP (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

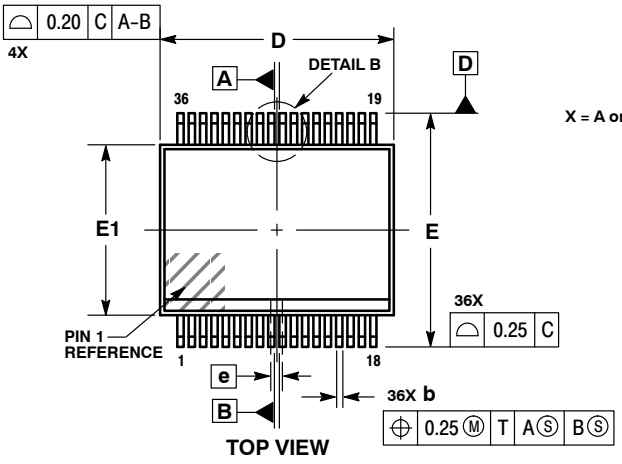
ON Semiconductor®

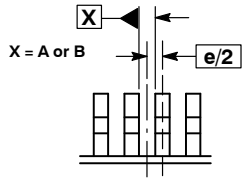


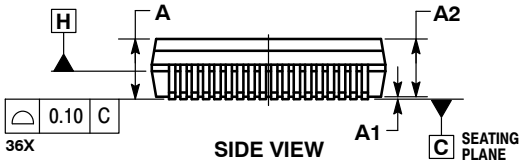
SCALE 1:1

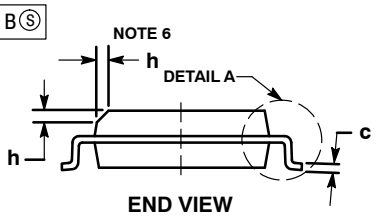
SSOP36 EP
CASE 940AB
ISSUE A

DATE 19 JAN 2016



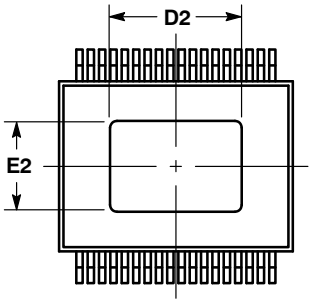


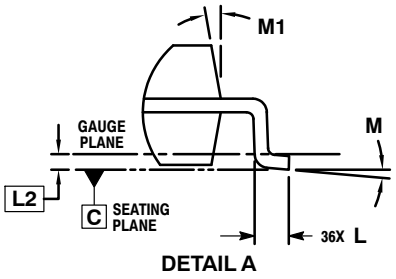




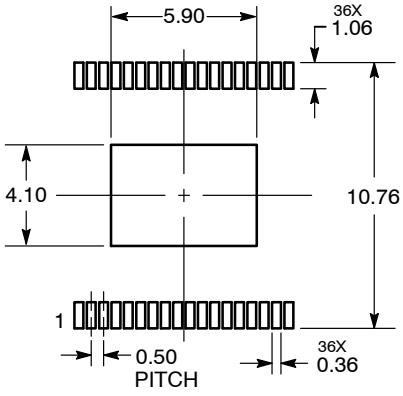
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.15	2.60
b	0.18	0.30
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°



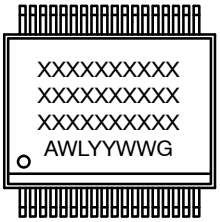


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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DESCRIPTION:	**SSOP36 EXPOSED PAD**		**PAGE 1 OF 1**

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