Octal High-Side Driver

NCV7755

The NCV7755 is an automotive grade integrated driver with eight high−side switches. The device provides drive capability up to 700 mA per channel and is protected for overload and overtemperature conditions. All the channels have integrated output clamps for switching inductive loads, multiple start pulses for bulbs, and can be mapped to two internal PWM generators for LED loads. The output control and diagnostic reporting is via SPI. Additionally, INx pins can be mapped to any of the outputs for direct control.

A dedicated limp−home mode enables operational control of two high−side drivers via logic input pins.

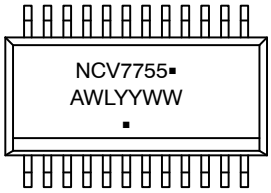
The NCV7755 is available in a SSOP−24 exposed pad package for optimal thermal performance.

Features

- 8 High−Side Channels
  - For Relays (Flyback Clamps)
  - Bulbs (Multiple Pulse in−rush Scheme)
  - LEDs (Internal PWM Generator)
  - 2.3 A Peak Current (Max)
  - $R_{DS(on)}$ 0.9 Ω (Typ), 1.8 Ω (Max)
  - Paralleling of Two Output Pair is Allowed
- SPI Control (16 Bit)
  - Frame Error Detection (16 Bits + 8*n Bits)
  - Daisy Chain Capable
- Two Input Pins with Mapping for PWM Operation
- Low Quiescent Current in Sleep Mode
- Limp Home Mode with Auto−retry
- Supports Cranking Voltage of 3 V Minimum on VS
- 3.3 V & 5 V Compatible Digital Input Supply Range
- Fault Reporting
  - Openload (OFF or ON)
  - Overload
  - Overtemperature
  - Power Supply Fail (VS, VDD Undervoltage)
  - Output Short to GND and Battery
- Reverse Polarity Protection
- Loss of Ground Protection
- Power−on Reset (VDD)
- SSOP−24 with an Exposed Pad
- NCV Prefix for Automotive
  - Site and Change Control
  - AEC−Q100 Qualified

SSOP24 NB EP
CASE 940AK

MARKING DIAGRAM



NCV7755 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

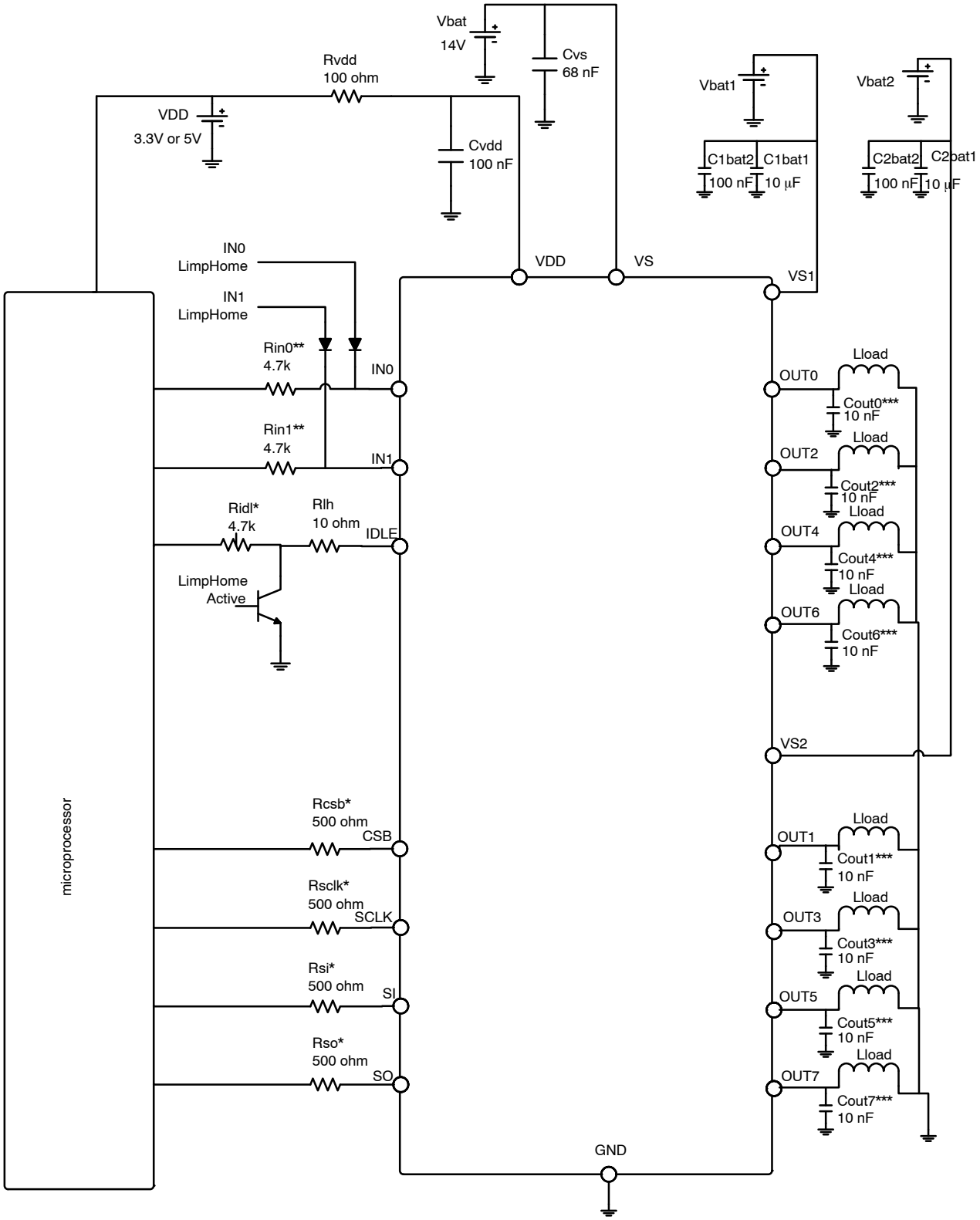
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NCV7755DQR2G	SSOP24−EP (Pb−Free)	2500 Units/Rail

Applications

- Automotive Body Control Unit
- Automotive Engine Control Unit
- Relay Drive
- Bulb Drive
- LED Drive



* Required for Reverse Polarity protection.
** Required for Reverse Polarity and Loss of Ground protection.
*** Required for EMC.

Figure 1. Application Diagram

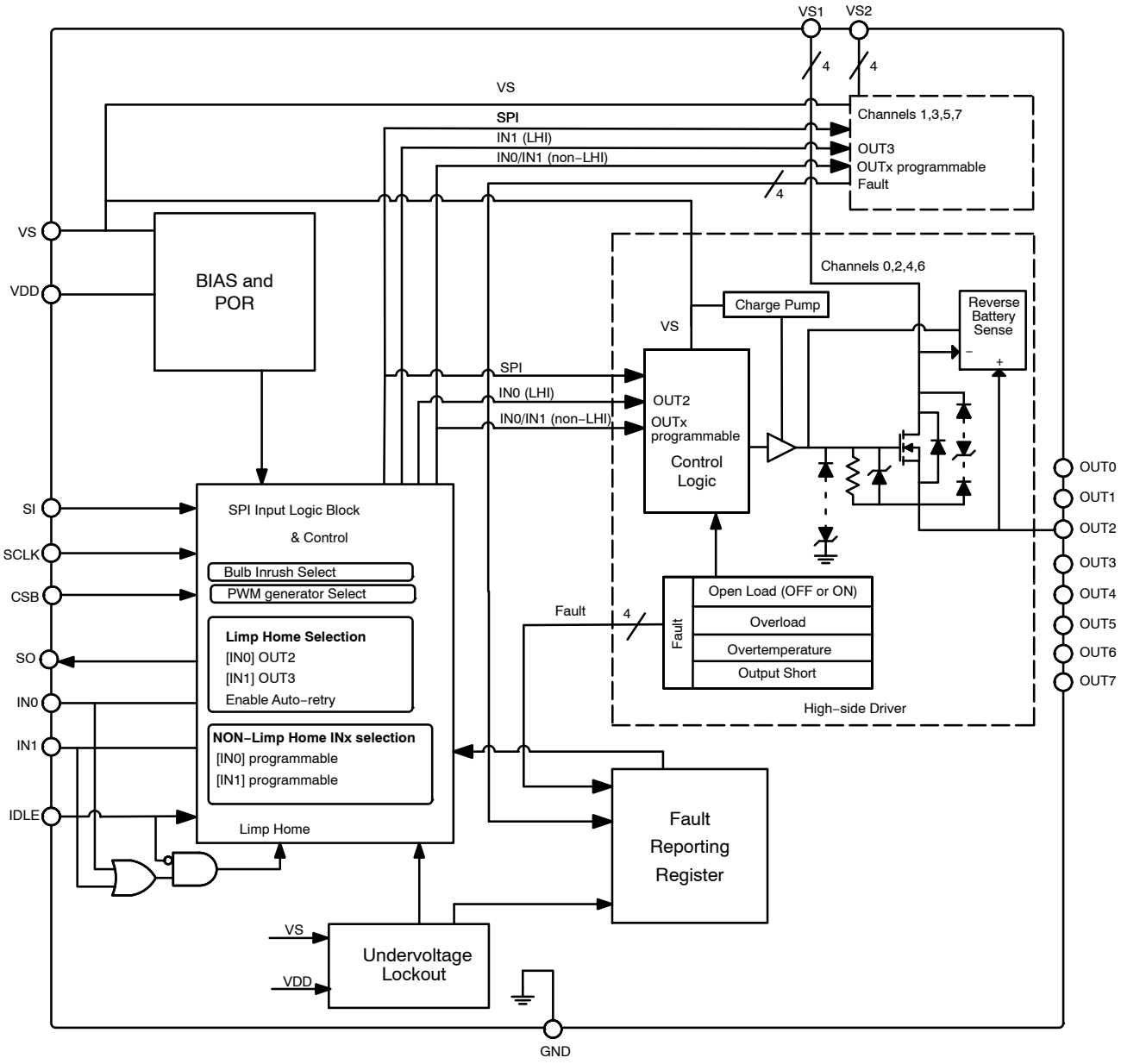


Figure 2. Block Diagram

PACKAGE PIN DESCRIPTION

SSOP−24 EPAD	Symbol	Description
1	CSB	SPI Chip Select “Bar” (120 kΩ pull−up resistor to VDD)
2	SCLK	SPI Clock (120 kΩ pull−down resistor)
3	SI	SPI Serial Data Input (120 kΩ pull−down resistor)
4	SO	SPI Serial Data Output. Tri−state when CSB is high
5	GND	Ground
6	OUT0	High−side driver output. Requires an external pull−down component for operation
7	NC	No connection. Internally not bonded
8	OUT2	High−side driver output. Requires an external pull−down component for operation
9	VS1	Power supply input for High−side drivers channels 0, 2, 4, and 6
10	OUT4	High−side driver output. Requires an external pull−down component for operation
11	OUT6	High−side driver output. Requires an external pull−down component for operation
12	NC	No connection. Internally not bonded
13	NC	No connection. Internally not bonded
14	OUT7	High−side driver output. Requires an external pull−down component for operation
15	OUT5	High−side driver output. Requires an external pull−down component for operation
16	VS2	Power supply input for High−side drivers channels 1, 3, 5, and 7
17	OUT3	High−side driver output. Requires an external pull−down component for operation
18	NC	No connection. Internally not bonded
19	OUT1	High−side driver output. Requires an external pull−down component for operation
20	VS	Power supply input for output power switches gate control
21	IDLE	High activates low Iq Idle mode (120 kΩ pull−down resistor) Low with IN0 = IN1 = low puts device in sleep mode. Low puts all SPI registers in reset Low with INx = high puts device in limp home mode
22	IN1*	Input pin 1. Controls channel 3 (default) and in Limp Home Mode (with IDLE = low). Outputs can be mapped to this pin. (120 kΩ pull−down resistor)
23	IN0*	Input pin 0. Controls channel 2 (default) and in Limp Home Mode (with IDLE = low). Outputs can be mapped to this pin. (120 kΩ pull−down resistor)
24	VDD	Digital power supply input for SPI and support interface to VS
EPAD	Exposed Pad	Connect to GND for best thermal performance or leave unconnected. Internally, the EPAD is isolated from the GND signal

*Ground if not used for best EMI performance.
Alternatively keep open and internal pull−down will hold the input low through a 120 kΩ pull down resistor.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Battery supply input voltage (VS) DC Positive Transient input supply voltage (Note 1)	 VsMax VsacMax	 −0.3 –	 36 42	 V V
Battery supply input voltage (VS1, VS2) DC input supply voltage with short circuit Positive Transient input supply voltage (Note 1)	 VsdcscMax VsxacMax	 0 –	 36 42	 V V
Logic Supply Input Voltage (VDD) DC	 VddMax	 −0.3	 5.5	 V
Output Voltage (OUTx)	VoutMax	−25	VSx+0.3	V
Output Current (OUTx) Specified is the maximum overload detection threshold.	 IoutMax	 –	 2.3	 A
Digital I/O pin voltage (IDLE, IN0, IN1, CSB, SCLK, SI,) (SO)	 VioMax ViosoMax	 −0.3 −0.3	 5.5 VDD+0.3V	 V V
Digital I/O input current (IDLE, IN0, IN1, CSB, SCLK, SI, SO)	 IioMax	 −10.0	 2.0	 mA
Clamping Energy Maximum (single pulse) (Tj = 25°C, Iout = 440 mA) (Tj = 150°C, Iout = 400 mA) Repetitive (multiple pulse)	 VclpDc25Max VclpDc150Max VclpAcMax	 – – –	 50 25 Note 2	 mJ mJ mJ
Operating Junction Temperature Range	Tj	−40	150	°C
Storage Temperature Range	Tstr	−65	150	°C
ESD Capability (AEC−Q100−002, AEC−Q100−011) Human body model (100 pF, 1.5 kΩ) (VSx, OUTx pins) Human body model (100 pF, 1.5 kΩ) (all other pins) Charged Device Model (corner pins) Charged Device Model (all other pins)	 Vesd4k Vesd2k Vesd750 Vesd500	 −4000 −2000 −750 −500	 4000 2000 750 500	 V V V V
AECQ10x−12 Short Circuit Reliability Characterization	AECQ10x	Grade A	–	

1. Ton = 400 ms; ton/toff = 10%, 100 pulse limit.
2. 2 M pulses (triangular), VS = 15 V, 63 Ω, 390 mH, T_A = 25°C.

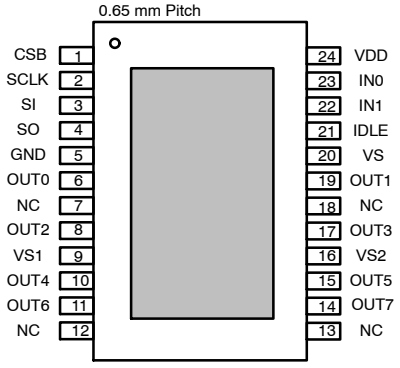


Figure 3. Pin−out

PACKAGE

Moisture Sensitivity Level	MSL	2		−−
Lead Temperature Soldering: SMD style only, Reflow (Note 3) Lead − Free Part 60 − 150 sec above 217°C, 40 sec max at peak	Treflow		265 peak	°C
Package Thermal Resistance and Characterization Parameter SSOP−24 EPAD Junction−to−Ambient (Note 4) Junction−to−pin (exposed pad)	 $R_{\theta JA}$ Ψ_{JB}	 	 35.1 24.3	 °C/W °C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. For additional information, see or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8083/D.
4. Per JEDEC JESD51−7 at natural convection on FR4 2s2p board (76.2 mm x 114.3 mm x 1.5 mm) with 2 inner copper layers.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value		Unit
		Min	Max	
Digital Supply Input Voltage (VDD)	VDDRec	3.00	5.5	V
Battery Supply Input Voltage (VS, VS1, VS2)	VSRec	7.0*	18**	V
DC Output Current (OUTx), (T_A = 85°C, all channels)	IoutRec	−−−	330	mA
Junction Temperature	T_J	−40	150	°C

*Extended operation down to 3 V with possible parameter shift. **Extended operation up to 28 V with possible parameter shift.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
VS CURRENTS						
Operating Current (VS) Active Mode	Set to Active Mode via SPI HWCR.ACT (bit 7) = 1 IDLE = CSB = VDD SCLK=0V No Open Circuit Diag Current					
Channels Off	7 V < VS < 18 V, IN0 = IN1 = 0	VSactOFF1	−	−	7.7	mA
	VS < VDD−1 V, IN0 = IN1 = 0	VSactOFF2	−	−	5.0	mA
Channels On	7 V < VS < 18 V, IN0 = IN1 = VDD	VSactON1	−	−	8.7	mA
	VS < VDD−1 V, IN0 = IN1 = VDD	VSactON2	−	2.3	5.0	mA
Operating Current (VS) Idle Mode	IDLE = CSB = VDD IN0 = IN1 = SCLK = 0 V All Channels Off					
	7 V < VS < 18 V	VSidl1	−	−	2.2	mA
	VS < VDD−1 V	VSidl2	−	−	0.3	mA
Operating Current (VS) Sleep Mode	CSB = VDD IDLE = IN0 = IN1 = 0 V					
	T_J = 85°C	VSslp85	−	0.1	3	μA
	T_J = 150°C	VSslp150	−	0.1	20	μA

ELECTRICAL CHARACTERISTICS (continued)(−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
VDD CURRENTS						
Operating Current (VDD) Active Mode	Set to Active Mode via SPI HWCR.ACT (bit 7) = 1 IDLE = CSB = VDD SCLK = 0 V No Open Circuit DIAG current					
Channels Off	7 V < VS < 18 V, IN0 = IN1 = 0	VDDactOFF1	–	–	0.3	mA
	VS < VDD−1 V, IN0 = IN1 = 0	VDDactOFF2	–	–	2.7	mA
Channels On	7 V < VS <18 V, IN0 = IN1 = VDD	VDDactON1	–	–	0.3	mA
	VS < VDD−1 V, IN0 = IN1 = VDD	VDDactON2	–	–	3.5	mA
Operating Current (VDD) Idle Mode	IDLE = CSB = VDD, IN0 = IN1 = SCLK = 0 V All Channels Off					
	7 V < VS < 18 V	VDDidl1	–	–	0.3	mA
	VS < VDD−1 V	VDDidl2	–	–	2.2	mA
Operating Current (VDD) Sleep Mode	CSB = VDD IDLE = IN0 = IN1 = 0 V					
	T_J = 85°C	VDDslp85	–	0.1	2.5	μA
	T_J = 150°C	VDDslp150	–	–	10	μA
TOTAL CURRENTS						
Total Sleep Current (VS + VDD)	CSB=VDD IDLE=IN0=IN1=0V					
	Tj=85°C	Slp85	–	–	5	μA
	Tj=150°C	Slp150	–	–	30	μA
Total Idle Mode Current Consumption (VS + VDD)	IDLE=CSB=VDD IN0=IN1=SCLK=0V All Channels Off	VSVDDidl	–	–	2.5	mA
Total Active Mode Current Consumption (VS + VDD)	Set to Active Mode via SPI HWCR.ACT (bit 7) = 1 IDLE = CSB = VDD, SCLK = 0 V					
Channels Off	All outputs off	VSVDDactOFF	–	–	8	mA
Channels On	All outputs on	VSVDDactON	–	–	9	mA
VS OPERATING RANGE						
VS Undervoltage Shutdown	VS falling OUTx = ON RL = 50 Ω	VSUVLO	1.5	2.7	3.0	V
VS Undervoltage Shutdown Hysteresis		VSUVLOhys	–	1	–	V
VS Minimum Operating Voltage	VS rising OUTx = ON RL = 50 Ω	VSmin	–	–	4.0	V
VDD OPERATING RANGE						
VDD Lower Operating Voltage		VDDLOP	3.0	–	4.5	V

ELECTRICAL CHARACTERISTICS (continued)(−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
VDD OPERATING RANGE						
VDD Undervoltage Shutdown	VDD falling SI = SCLK = CSB = 0 V SO from low to high impedance	VDDUVLO	1.0	2.7	3.0	V
THERMAL PERFORMANCE						
Thermal Shutdown	Note 11	TSD	150	175	200	°C
Thermal Hysteresis	Note 11	TSDhys	10	25	–	°C
OUTPUT DRIVER						
Output Transistor RDSon	IOUT = 220 mA T_J = 25°C T_J = 150°C	 Rdson25 Rdson150	 – –	 0.9 1.6	 – 1.8	 Ω Ω
Reverse Polarity ON Resistance	VSx = −16 V IOUT = 220 mA Tj = 25°C Tj = 150°C	 Revpol25 Revpol150	 – –	 0.9 1.6	 – –	 Ω Ω
Overload Detection Current 1st threshold (OVL0) 2nd threshold (OVL1)		 ILovl0 ILovl1	 1.30 0.70	 1.80 1.05	 2.30 1.30	 A A
Overload Shutdown Delay Time	Active Mode including Bulb Inrush Mode Individual channel operation BIM.OUTn = HWCR.PAR = 0_B	tOVLO	4	7	11	µs
Output Leakage	VS = VDD = 0 V VOUT = 0 V VDS = 28 V Tj = 85°C Tj = 150°C	 Leak85 Leak150	 – –	 0.01 0.1	 0.5 5.0	 µA µA
Output Current During Loss of Ground	RL = 50 Ω VS = VS1 = VS2	LOG	−2.0	–	–	mA
Dropout Voltage	RL = 50 Ω VS = VS1 = VS2 = 4 V	Drop	–	–	1	V
Output Drain/Source Clamp	IL = 20 mA VS = VS1 = VS2 = 36 V	clampDS	42	46	54	V
Output Source/GND Clamp	IL = 20 mA VS = VS1 = VS2 = 7 V	clampSG	−25	–	−16	V
MODE DELAY TIMES						
Sleep to Idle Delay	IDLE pin going high (50%) To TER+INST register = 8680_H	Slp2idl	–	200	400	µs
Sleep to Limp Home Delay	INx going high To VDS = 10%VS	Slp2lh	–	300	600	µs
Idle to Sleep Delay	IDLE pin going low (50%) To Standard Diagnostics clearing = 0000_H	Idl2slp	–	100	200	µs
Idle to Active Delay	INx going high to MODE = 10_B From CSB going high To MODE = 10_B	Idl2actINx Idl2actCSB	– –	100 100	200 200	µs µs
Limp Home to Sleep Delay	INx going low To Standard Diagnostics clearing = 0000_H	Lh2slp	–	200	400	µs
Limp Home to Active Delay	IDLE going high To MODE=10_B	Lh2act	–	50	100	µs

ELECTRICAL CHARACTERISTICS (continued)(−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
MODE DELAY TIMES						
Active to Idle Delay	INx going low to MODE = 11_B	Act2idlINx	–	100	200	μs
	From CSB going high To MODE = 11_B	Act2idlCSB		100	200	μs
Active to Limp Home Delay	IDLE going low To TER + INST register= 8683_H (IN0 = VDD, IN1 = VDD)or 8682_H (IN0 = GND, IN1 = VDD)or 8681_H (IN0 = VDD, IN1 = GND)	Act2lh	–	50	100	μs
Active to Sleep Delay	IDLE going low To Standard Diagnostics clearing = 0000_H Rload = 10K to GND	Act2slp	–	50	100	μs
OUTPUT TIMING SPECIFICATION						
Turn On Delay	VS = VS1 = VS2 = 13.5 V, RL = 50 Ω					
Active Mode	INx to 10% VOUT	tONactINx10	1	4	8	μs
	CSB rising edge to 10% VOUT	tONactCSB10	1	4	8	μs
Limp Home Mode	INx to 10% VOUT	tONlh10	1	4	8	μs
Turn Off Delay	VS = VS1 = VS2 = 13.5 V, RL = 50 Ω					
Active Mode	INx to 90% VOUT	tOFFactINx90	1	6	12	μs
	CSB rising edge to 90% VOUT	tOFFactCSB90	1	6	12	μs
Limp Home Mode	INx to 90% VOUT	tOFFlh90	1	6	12	μs
Turn On / Turn Off Matching						
Active Mode	VS = VS1 = VS2 = 13.5 V, RL = 50 Ω	tMatchACT	−10	0	10	μs
Limp Home Mode		tMatchLH	−10	0	10	μs
Rise Time						
Active Mode	VS = VS1 = VS2 = 13.5 V, RL = 50 Ω	tRiseAct	2.4	5.25	7.7	μs
Limp Home Mode	30% to 70% VS	tRiselh	2.4	5.25	7.7	μs
Fall Time						
Active Mode	VS = VS1 = VS2 = 13.5 V, RL = 50 Ω	tFallAct	2.8	5.25	7.7	μs
Limp Home Mode	70% to 30% VS	tFalllh	2.8	5.25	7.7	μs
LIMP HOME TIMING						
Limp Home Auto−Retry Times						
Limp Home Mode 0		tRSTlh0	7	10	13	ms
Limp Home Mode 1		tRSTlh1	14	20	26	ms
Limp Home Mode 2		tRSTlh2	28	40	52	ms
Limp Home Mode 3		tRSTlh3	56	80	104	ms
BULB INRUSH TIMING						
Restart Time Bulb Inrush Mode		tRSTbim	–	–	40	μs
Overload Current Switch Threshold Delay Time		tOVLIN	110	185	260	μs
Reset Time Bulb Inrush Mode		tBIM	–	40	–	ms

ELECTRICAL CHARACTERISTICS (continued)(−40°C < T_J < 150°C, 3.0 V < VDD < 5.5 V, 7 V < VS = VS1 = VS2 < 18 V, IDLE = high unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
PWM GENERATOR						
Internal Frequency	HWCR_PWM.ADJ = 1000_B	fINT	80	102	125	kHz
Internal Frequency Variation between Generator 0 and Generator 1		fVAR	−15	–	15	%
Internal Frequency Synchronization Time (Note 5)	HWCR_PWM.ADJ = 1000_B	tSYNC	–	5	10	μs
OPEN LOAD OUTPUT STATUS MONITOR						
Output Status Monitor Comparator Settling Time		OpenT	–	–	20	μs
Output Status Monitor Threshold Voltage		OpenV	3.0	3.3	3.6	V
Output Status Monitor Diagnostic Source Current		OpenI	25	50	100	μA
Open Load equivalent resistance		OpenR	30	–	300	kΩ
OPEN LOAD AT ON						
Open Load ON Wait for Diagnostic (Note 6)		tDIAGwait	6	15	35	μs
Open Load ON Waiting Time before mux activation (Note 7)		tMUXopnON	40	58	76	μs
Open Load ON Settling Time (Note 8)		tSETopnON	–	20	40	μs
Open Load ON Channel Switching Time(Note 9)		tSWTopnON	–	10	20	μs
Open Load ON Threshold Current		IopnON	1	6	10	mA

5. Basis in timing requirements for
   i) Reset Overload Current Thresholds.
   ii) Auto−retry timing reset in limp home mode.
   iii) Open Load at ON multiplex operation (but not direct channel diagnostic).
6. Time required to wait before programming for Open Load ON Diagnostic Control.
7. Delay from PWM generator going high to fault recognized in DIAG_OLON.OUT.
8. Delay from Open Load ON Diagnostic Control (with system fault) bit set to fault recognized in DIAG_OLON.OUT.
9. Delay time between Open Load at ON event and to fault recognized in DIAG_OLON.OUT.

DIGITAL INTERFACE CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Digital Input Threshold (IDLE, IN0, IN1, CSB, SCLK, SI)		VthIn	0.8	1.4	2.0	V
Digital Input Hysteresis (IDLE, IN0, IN1, CSB, SCLK, SI)		VhysIn	50	175	300	mV
Input Pull−down Resistance (IDLE, IN0, IN1, SI, SCLK)	IDLE = IN0 = IN1 = SI = SCLK = VDD	Rpdx	50	120	190	kΩ
Input Pull−up Resistance (CSB)	CSB = 0 V	RpdCSBx	50	120	190	kΩ
CSB Leakage to VDD	CSB = 5 V, VDD = 0 V	$IlkgCSBV_{DD}$	–	–	100	μA

DIGITAL INTERFACE CHARACTERISTICS (continued)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
SO – Output High	I(out) = 1.5 mA	VsoH	VDD–0.4	–	VDD	V
SO – Output Low	I(out) = –2.0 mA	VsoL	–	–	0.4	V
SO Tri–state Leakage	CSB = VDD, 0 V < SO < VDD	IlkzSOtstate	–1	–	1	μA
SPI TIMING (VDD = 4.5 V and VS > 7 V)						
SCLK Frequency		Fclk	–	–	5	MHz
SCLK Clock Period		TpClk	200	–	–	ns
SCLK High Time		TCLKH	85	–	–	ns
SCLK Low Time		TCLKL	85	–	–	ns
SCLK Setup Time To CSB going low	Falling SCLK to falling CSB	TCLKSU1	85	–	–	ns
SCLK Setup Time To CSB going high	Falling SCLK to rising CSB	TCLKSU2	85	–	–	ns
SI Setup Time		TISU	50	–	–	ns
SI Hold Time		TIHT	50	–	–	ns
CSB Setup Time		TCSBSU1	100	–	–	ns
CSB Setup Time		TCSBSU2	100	–	–	ns
CSB High Time	(Note 10)	TCSBHT	5.0	–	–	μs
SO enable after CSB falling edge		TSOCSBF	–	–	200	ns
SO disable After CSB rising edge		TSOCSBR	–	–	200	ns
SO Rise Time	Cload = 40 pF (Note 11)	TSOrise	–	10	25	ns
SO Fall Time	Cload = 40 pF (Note 11)	TSOfall	–	10	25	ns
SO Valid Time	Cload 40 pF (Note 11) SCLK rising 80% to SO 50%	TSOV	–	50	100	ns

10. This is the minimum time the user must wait between SPI commands.
11. Not production tested.

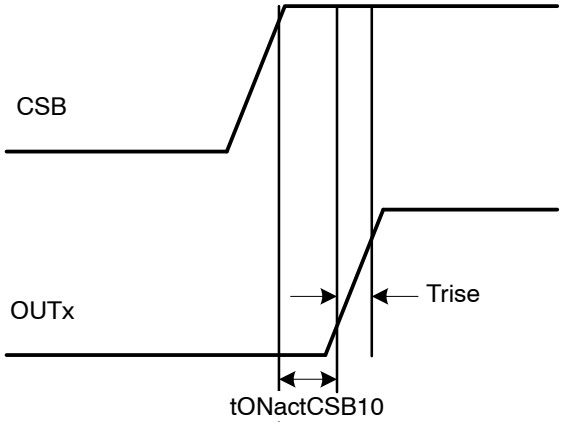


Figure 4. Serial Turn On

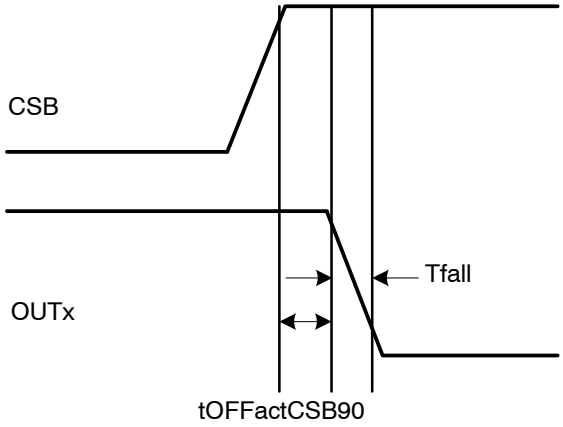


Figure 5. Serial Turn Off

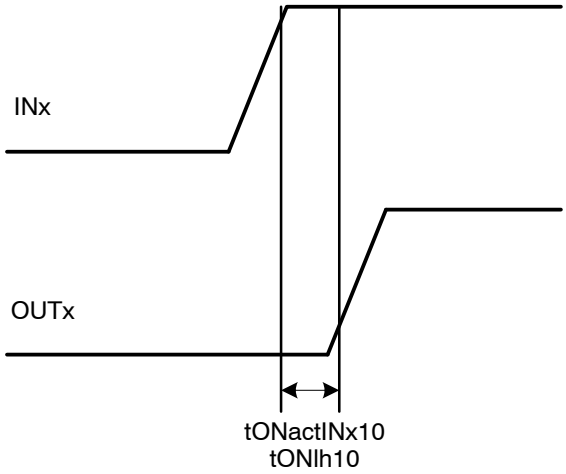


Figure 6. INx Control Turn On

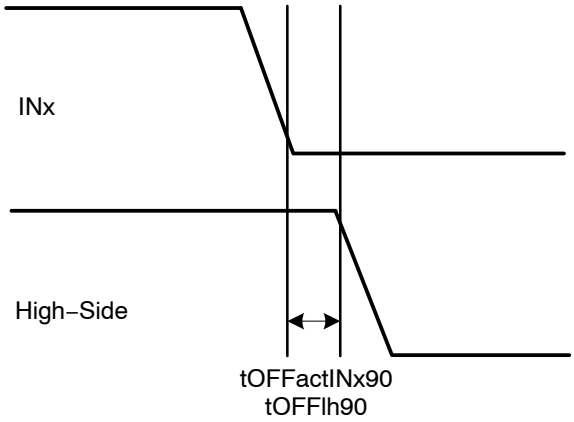


Figure 7. INx Control Turn Off

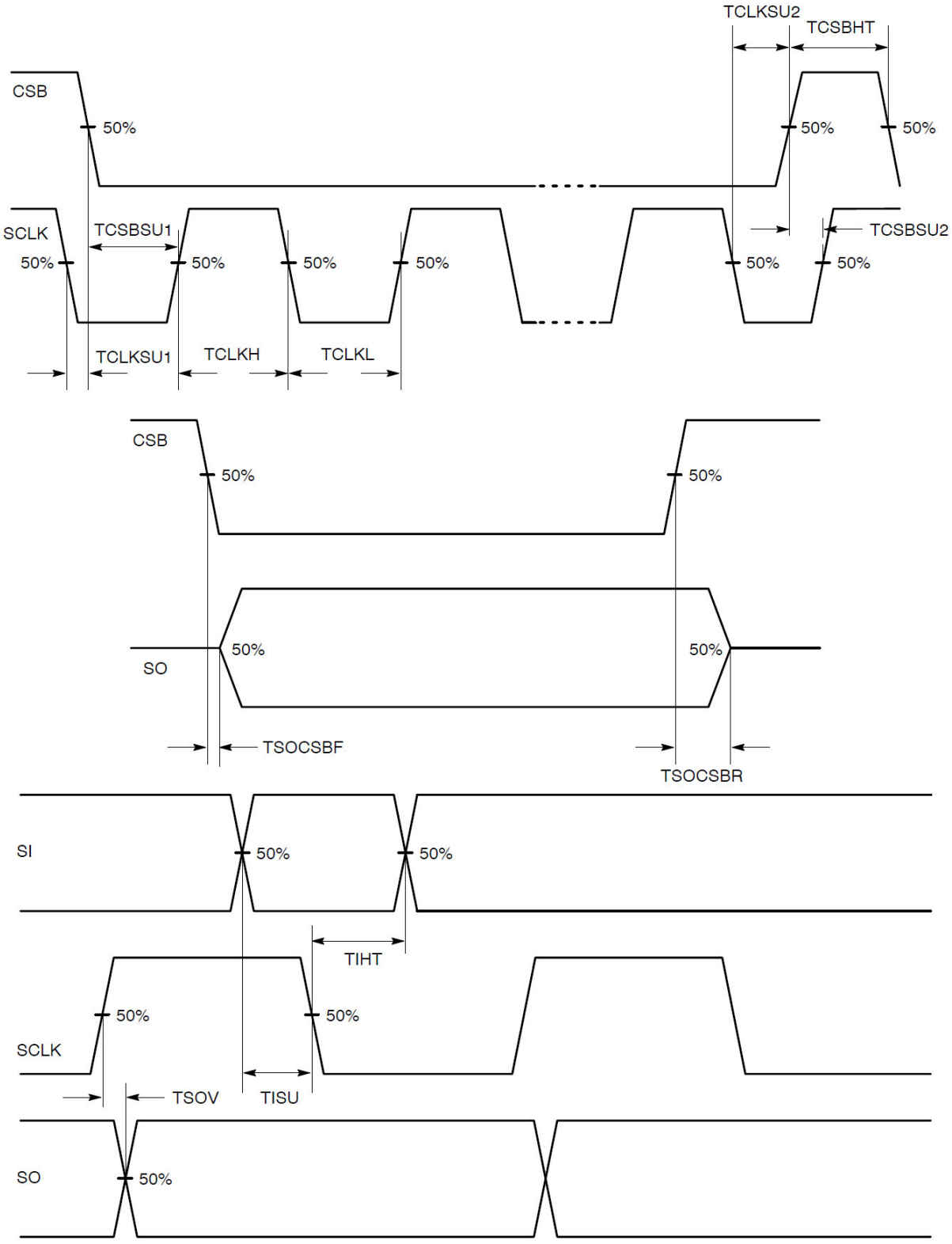


Figure 8. Serial Peripheral Interface Detailed Timing

TYPICAL PERFORMANCE GRAPHS

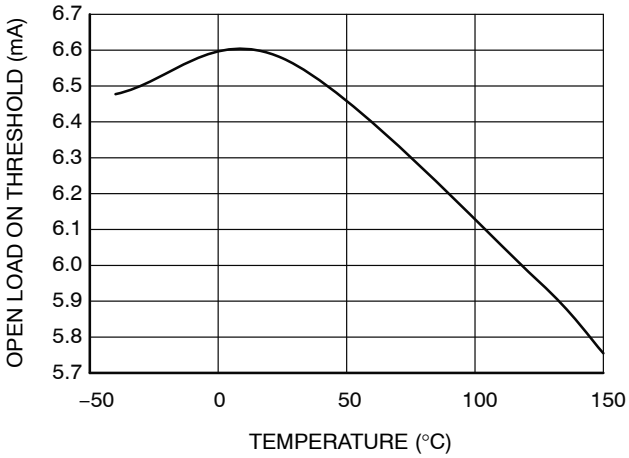


Figure 9. Open Load On Threshold vs. Temperature

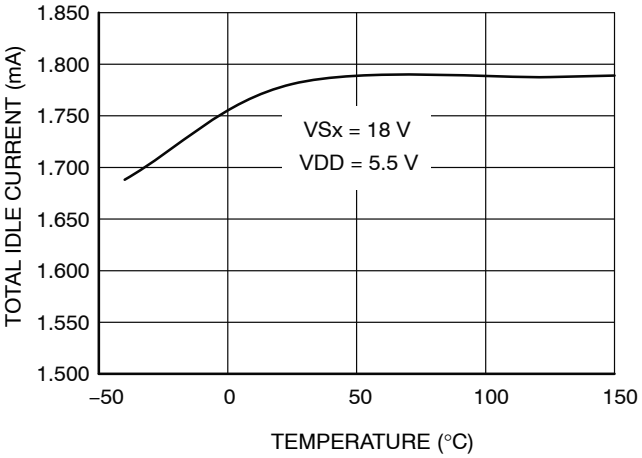


Figure 10. Total Idle Current vs. Temperature

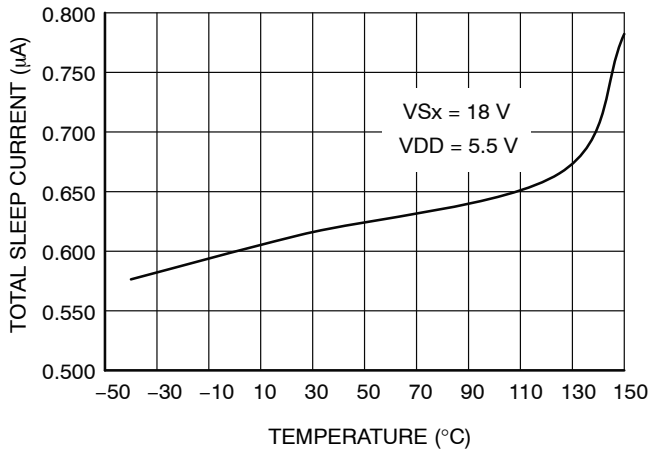


Figure 11. Total Sleep Current vs. Temperature

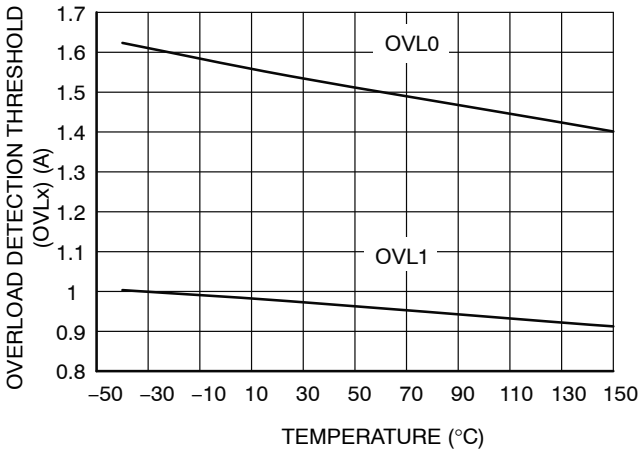


Figure 12. Overload Threshold vs. Temperature

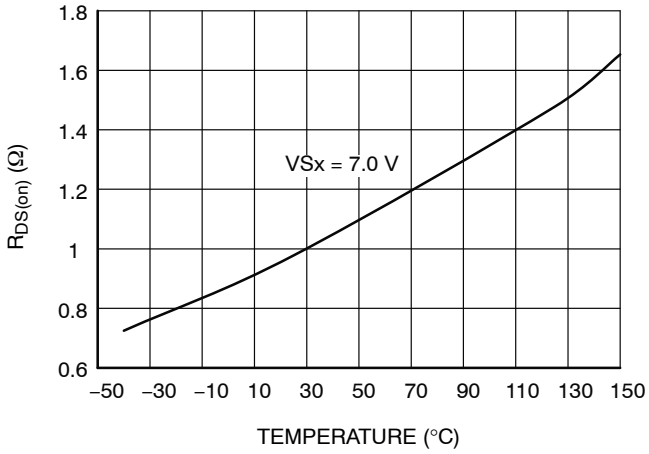


Figure 13. $R_{DS(on)}$ vs. Temperature

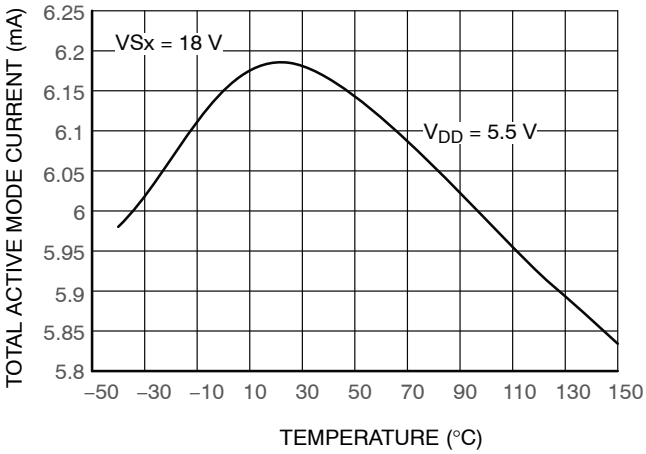


Figure 14. Total Active Mode Current vs. Temperature

DETAILED OPERATING DESCRIPTION

General Overview

The NCV7755 is comprised of eight DMOS high−side power drivers. There are two connection pins (VS1, VS2) for the drain of each output driver with 4 common drivers per pin. Communication to the device is through a 16−bit SPI port for output control, programming, and fault reporting. The device also features a limp home mode with an IDLE control pin for limp home entry and two input control pins (IN0 & IN1) for output engagement.

Output loads can be varied from inductive loads, bulb loads, or LED loads. Special features for each load type include output clamps, in−rush design considerations, and two on−chip PWM generators.

The NCV7755 allows independent mapping of the INx pins to the outputs and independent mapping of the two PWM generators to the outputs.

The device is capable of running down to VS = 3 V for automotive cranking events.

Power Supply

There are four power supply input requirements. The descriptions of their internal connections are listed below.

- VS – Analog Supply Input – Battery input for all internal analog circuitry. The maximum current drain is 8.7 mA over temperature
- VS1 – Output Driver Drain connection for OUT0, OUT2, OUT4, OUT6. The maximum current is internally limited by the maximum overload detection threshold of 2.3 A (each channel)
- VS2 – Output Driver Drain connection for OUT1, OUT3, OUT5, OUT7. The maximum current is internally limited by the maximum overload detection threshold of 2.3 A (each channel)
- VDD – Digital Supply Input – Internal logic supply input. Runs from 3.3 V input or 5 V input. The maximum current drain is 3.5 mA over temperature

It's important to note the maximum combined current drain of both VS and VDD is specified at 9 mA with the channels on.

Sleep mode current for VS is 3 μA at 85°C and the maximum combination of VS+VDD is 5 μA at 85°C.

The exposed pad connection should be connected to ground with as large a pc board metal connection as possible for best thermal performance and EMC considerations. However this is not a ground connection for IC ground currents.

Load Dump – During a peak transient event such as automotive load dump the outputs maintain their operation up to the maximum rating for Positive Transient input supply voltage of 42 V as programmed via SPI or the input control pins IN0 and IN1.

Cranking Conditions – Automotive cranking conditions can cause the battery (aka VS) to dip to low levels. In order to maintain circuit operation down to the lowest possible levels the battery connection is OR'd with the logic supply voltage (VDD). Diodes D1 and D2 provide the OR'd condition into the voltage regulator. The reduction or removal of current into D1 from VS will cause the current into D2 from VDD to increase to keep the voltage regulator alive. Additional current can also come from SO.

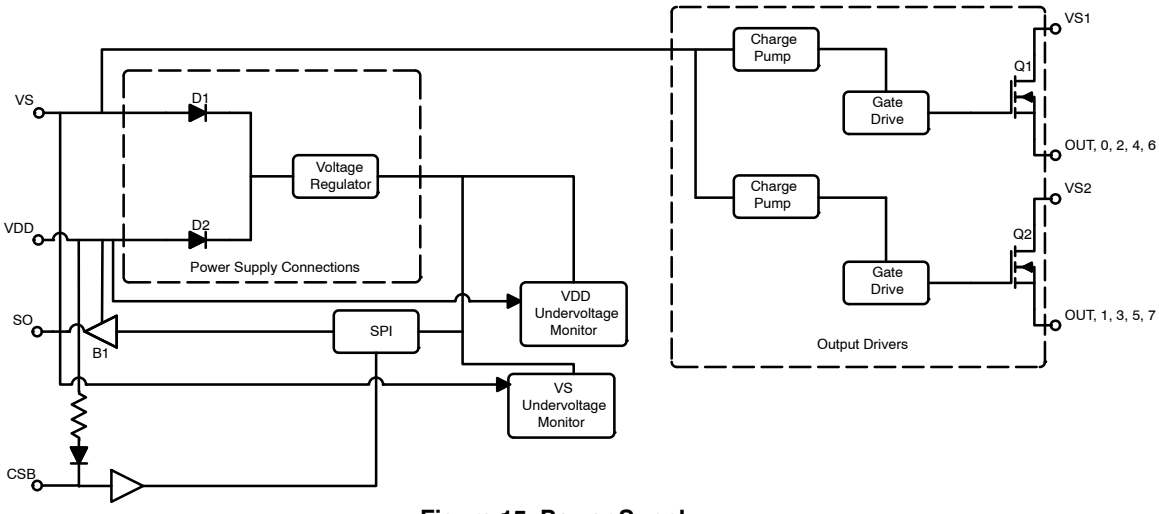


Figure 15. Power Supply

Power−Up/Power−Down Control

VDD and VS each has their own Power−On reset monitors which serve to hold off proper operation until sufficient voltage is present to control the output device. The device powers up with sufficient voltage on either or both VDD or VS, and INx or IDLE pin are high. The Standard Diagnostic Register initially reports both VS Undervoltage (Monitor) and VDD Lower Operating Range (Monitor).

SPI communication is present with sufficient voltage on VDD. An undervoltage on VDD resets all the registers to their default values and no SPI communication is available, although memory of Overload / Overtemperature conditions is maintained in ERR of the Standard Diagnostics Register and can be retrieved when VDD is present. If VS is present with VDD undervoltage, Limp Home mode control is possible.

Sufficient voltage on VS allows for output turn−on. During cranking conditions as VS dips, the diode OR'd circuit described in the previous section allows for the IC to maintain current into the logic solely from VDD. All channels which are on keep their state during cranking unless commanded to turn off. Channel turn−on may not be possible during cranking.

VDD Low Operation Voltage – VDD is monitored and its status is reported in the Diagnostic Register as bit 13 (LOPVDD). The default value is set to a "1" during power up and is continuously monitored for the electrical parameter VDD Lower Operating Voltage (between 3.0 V and 4.5 V). Because of this threshold, operation for VDD with a 3.3 V supply will continuously report a "1" in this register. The LOPVDD bit can only be reset by reading the Standard Diagnostic Register.

DIAGNOSTIC REGISTER (Default listing after Power−up or Reset)

Field	State	Description
UVRVS	1	There was an undervoltage condition on VS
LOPVDD	1	VDD was previously below 4.5 V
MODE	11	Idle Mode (2 bits)
TER	1	Previous transmission failed
OLON	0	No open load ON detected
OLOFF	0	No open load OFF detected
ERR	0	No Failure detected

INST REGISTER (This is the 1st Register Read back after a Logic Reset)

Field	State	Description
INST	TER = 1 INx = 0	Previous transmission failed. Input pins are set low

DEFAULT LISTING AFTER LOGIC RESET

Field	Description
OUT	Output is off
BIM	Output latches off with overload
MAPIN0	IN0 is mapped to OUT2
MAPIN1	IN1 is mapped to OUT3
INST	Previous transmission failed. Input pins are set low
DIAG_IOL	Diagnostic current is not enabled
DIAG_OSM	Voutx is less than the Output Monitor Threshold
DIAG_OLON	Normal operation
DIAG_OLONEN	Open Load ON not active
HWCR	Normal operation, no reset command, no parallel combinations
HWCR_OCL	Normal operation, no latch clear
HWCR_PWM	PWM generator 1 not active. PWM generator 0 not active
PWM_CR0	Generator 0 Base Frequency Internal clock divided by 1024
PWM_CR1	Generator 1 Base Frequency Internal clock divided by 1024
PWM_OUT	The selected output is not driven by a PWM generator
PWM_MAP	The selected output is connected to PWM Generator 0

Table 1. DEVICE CAPABILITY AS A FUNCTION OF VS AND VDD

	VDD < VDDUVLO (Note 15)	**VDD = VDDLOP** (Note 16)	**VDD > VDDLOP** (Note 17)
VS < 3.0 V (Note 12)	Channels – Cannot be controlled	Channels – Cannot be controlled	Channels – Cannot be controlled
	SPI registers – Reset	SPI registers – Available	SPI registers – Available
	SPI communication – Not available	SPI communication – Possible (fsclk = 1 MHz)	SPI communication – Possible (fsclk = 5 MHz)
	Limp Home Mode – Not available	Limp Home Mode – Available (channels are off)	Limp Home Mode – Available (channels are off)
3.0 V < VS < VSmin (Note 13)	Channels – Cannot be controlled by SPI	Channels – Can be controlled by SPI (Rdson deviations possible).	Channels – Can be controlled by SPI (Rdson deviations possible).
	SPI registers – Reset	SPI registers – Available	SPI registers – Available
	SPI communication – Not available	SPI communication – Possible (fsclk = 1 MHz)	SPI communication – Possible (fsclk = 5 MHz)
	Limp Home Mode – Available (Rdson deviations possible)	Limp Home Mode – Available (Rdson deviations possible)	Limp Home Mode – Available (Rdson deviations possible)
VS > VSmin (Note 14)	Channels – Cannot be controlled by SPI	Channels – Can be controlled by SPI (Rdson deviations possible).	Channels – Can be controlled by SPI (Rdson deviations possible).
	SPI registers – Reset	SPI registers – Available	SPI registers – Available
	SPI communication – Not available	SPI communication – Possible (fsclk = 5 MHz)	SPI communication – Possible (fsclk = 5 MHz)
	Limp Home Mode – Available (Rdson deviations possible with VS < 7 V)	Limp Home Mode – Available (Rdson deviations possible with VS < 7 V)	Limp Home Mode – Available (Rdson deviations possible with VS < 7 V)

12. (Undervoltage Shutdown max specification VUVLO = 3 V)
13. VSmin = (Minimum Operating Voltage)
14. VSmin = (Minimum Operating Voltage)
15. VDDUVLO = VDD Undervoltage Shutdown
16. VDDLOP = VDD Lower Operating Voltage
17. VDDLOP = VDD Lower Operating Voltage

Modes of Operation

There are 4 modes of operation. Each is presented in the state diagram below.

1. Sleep Mode
2. Idle Mode
3. Active Mode
4. Limp Home Mode

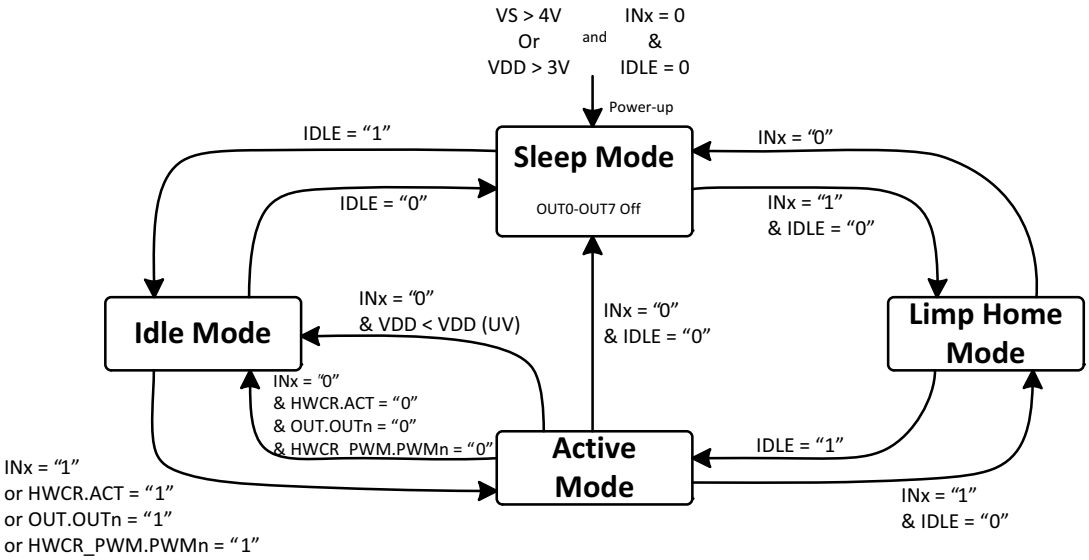


Figure 16. Modes of Operation

TABLE 2. DEVICE FUNCTION VERSUS VS AND VDD VOLTAGES

Operation Mode	Function	VS Undervoltage VDD<VDDUVLO	VS Undervoltage VDD > VDDUVLO	VS no Undervoltage VDD<VDDUVLO	VS no Undervoltage VDD > VDDUVLO
Sleep	Channels	Channels not available no SPI communication SPI Register Reset	Channels not available no SPI communication SPI Register Reset		
	SPI Communication				
	SPI Registers				
Idle	Channels		x	✓	x
	SPI Communication		✓	x	✓
	SPI Registers		✓	reset	✓
Active	Channels		x	✓ (INx pins only)	✓
	SPI Communication		✓	x	✓
	SPI Registers		✓	reset	✓
Limp Home	Channels		x	✓ (INx pins only)	✓ (INx pins only)
	SPI Communication		✓ (read only)	x	✓ (read only)
	SPI Registers		✓ (read only)	reset	✓ (read only)

Power−up

The power−up condition for the NCV7755 is an OR'd condition between the VS battery input and the VDD logic input. Either of the supplies exceeding their minimum operative voltage (4.0 V max for VS) or (3.0 V for VDD) will initiate the internal power−on sequence. In addition to these low voltage attributes, the device will maintain its state with battery voltages down to VS = 3 V such as during cranking. For SPI communication, the digital power supply must also be maintained at > 3 V.

Sleep Mode

The NCV7755 enters sleep mode when pins IDLE and IN0 and IN1 are all low. All outputs are off and all SPI registers are reset. Operating current is at a minimum (3 μA max at 85°C).

Idle Mode

The device enters Idle Mode when the IDLE pin is brought high with IN0 and IN1 low. All channels are off and Open Load Diagnostic Current is off. The internal regulator powers on and SPI registers and communication become active with a proper logic supply voltage (VDD). Overload / Overtemperature bits are not cleared when entering Idle mode from active mode for safety reasons.

Active Mode

The normal operational mode for the device is Active Mode. The high−side drivers can be activated, loads can be driven, device output status can be retrieved, and device attributes can be programmed. The device enters active mode with any of the following commands.

- IDLE is high and IN0 or IN1 is set to a one
- IDLE is high and the Hardware Configuration Register (HWCR.ACT) is set to a 1_B via a SPI command
- IDLE is high and the Power Output Control Register (OUT.OUTn) is set to a 1_B for one or more of the outputs via a SPI command
- IDLE is high and a PWM Configuration Register (HWCR.PWM.PWMn) is set active via a SPI command

Any transition into Active Mode institutes a communication link between IN0, IN1 and OUT2, OUT3.

DIGITAL MODE CHART

MODE	IDLE	IN0	IN1
Sleep	0	0	0
IDLE	1	0	0
Active*	1	1 and/or	1
Limp Home	0	1 and/or	1

*Additionally, Active Mode can be entered via SPI control.

Hardware Configuration Register − HWCR.ACT = 1
Power Output Control Register − OUT.OUT = 1
PWM Configuration Register − HWCR_PWM.PWMn = 1

Limp Home Mode

Only Channel 2 and 3 are controlled (via IN0 and IN1) during Limp Home Mode. Limp Home mode requires only VS and VSx for driver turn−on. VDD is not required. The device enters Limp Home Mode when the IDLE pin is low and IN0 and/or IN1 are high. When IN0 is high, channel 2 turns on. When IN1 is high, channel 3 turns on. These two input control pins and corresponding channels are also active after a power up condition.

SPI communication is active (with VDD>VDDUVLO) in read−only mode only and reports Overload and Overtemperature faults, and will also continue to monitor for Output Status Monitor conditions (on all channels), but Open Load Diagnostic Current is inactive (on all channels).

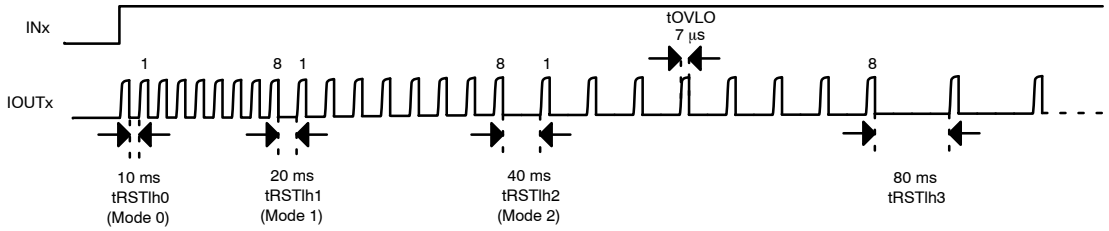
When entering Limp Home Mode, the Undervoltage Monitor (UVRVS) and Lower Operating Range Monitor (LOPVDD) bits are set to 1_B while the Open Load ON (OLON) State and Open Load OFF (OLOFF) State are set to 0_B. The Transmission Error bit (TER) is set to “1” for the first SPI command which is sent back with the INST register returned with the first SPI command, and will act normally afterwards.

The NCV7755 incorporates an auto−retry function for highly capacitive loads in Limp Home Mode. In normal operation (Active Mode), the device can compensate for capacitive loads (in case of Overload, Short Circuit or Overtemperature) with the external microprocessor drive control time, but when in Limp Home Mode this is not possible. Attempted tries to turn on an output with a constant input high control when exposed to Overload (Ilovl0), Short Circuit or Overtemperature will occur with the following characteristics.

- 10 ms (8 retries)
- 20 ms (8 retries)
- 40 ms (8 retries)
- 80 ms (continuously)

It is important to note the 8 counts do not include the initial turn−on attempt of the device.

A reset to the initial 8 retries at 10 ms can be realized with a low on the input of 2 times the Internal Frequency Synchronization Time (typically 2 x 5 μs).



*Ilovl0 − This is the higher current threshold used in Active Mode.

Figure 17.

Output Control

The 8 outputs can be controlled via 4 ways which are listed below.

1. Output Control via SPI. Commands to turn a device on are input through the SPI interface.
2. Output Control via IN0 and/or IN1. To activate this, a SPI command must be sent to map the control to either IN0 (MAPIN0) or IN1 (MAPIN1). By default, mapping of IN0 and IN1 are set to OUT2 (IN0) and OUT3 (IN1) after power−up.
3. Limp Home Mode – A low on IDLE will allow control of OUT2 (IN0) and OUT3 (IN1).
4. PWM Control – A SPI command can connect any of the outputs to either of 2 PWM generators whose properties for frequency and duty cycle are programmable.

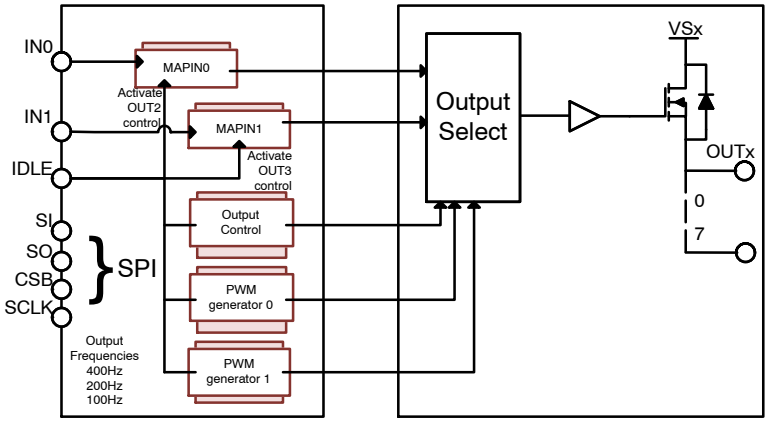


Figure 18. Output Control

OUTPUTS

The 8 outputs of the NCV7755 are designed to work with multiple types of loads and with the capability of paralleling two paired channels.

Resistive Loads

Resistive loads are primarily concerned with output current, switching delays, and slew rates. The NCV7755 has two overload thresholds. The 1st overload threshold is 1.3 A (min) and has an overload current switch threshold delay time (tOVLIN) of 110 μs (min) triggered by OUT.OUTn. Once this delay time has been exceeded, the overload threshold reduces to 0.7 A (min). Turn−on delay time is 8 us (max) and turn−off delay time is 12 μs (max). Rise and fall times are both 2.8 μs (min).

A turn off time longer than 2 x Internal Frequency Synchronization Time will reset the overload threshold back to the 1st level.

Relays

Relay loads are supported using an internal inductive clamp on the output driver to protect the driver. The negative transients seen when turning off an inductive load are internally limited on the output drivers with a clamp voltage minimum of −25 V. Paired output drivers are permissible with the use of the paired channel synchronization handling of overload and overtemperature conditions.

Bulbs

The NCV7755 is designed to drive 2 W lamps or 5 W lamps (using two channels in parallel) with its Bulb Inrush feature. Incandescent bulb in−rush characteristics are exhibited as a high current event due to the bulb filament initial low resistance. As the bulb heats up the resistance increases. Initial high currents could trigger an overload condition latching off the output. Setting a bit in the Bulb Inrush Mode register (BIM) allows the device to latch off (and report ERRn during that time [tRSTbim]) and automatically restart after the Bulb Inrush Mode Restart Time of 40 μs (max). Overtemperature conditions can also trigger a latch off event and auto−restart. The auto−restart helps to increase the bulb resistance putting the overload threshold out of range. Bulb Inrush Mode continues until the bulb is illuminated (not in overload) or the Bulb Inrush Mode reset time is reached (typically 40 ms). Dual Overload Detection Current thresholds continue to be valid in Bulb Inrush Mode.

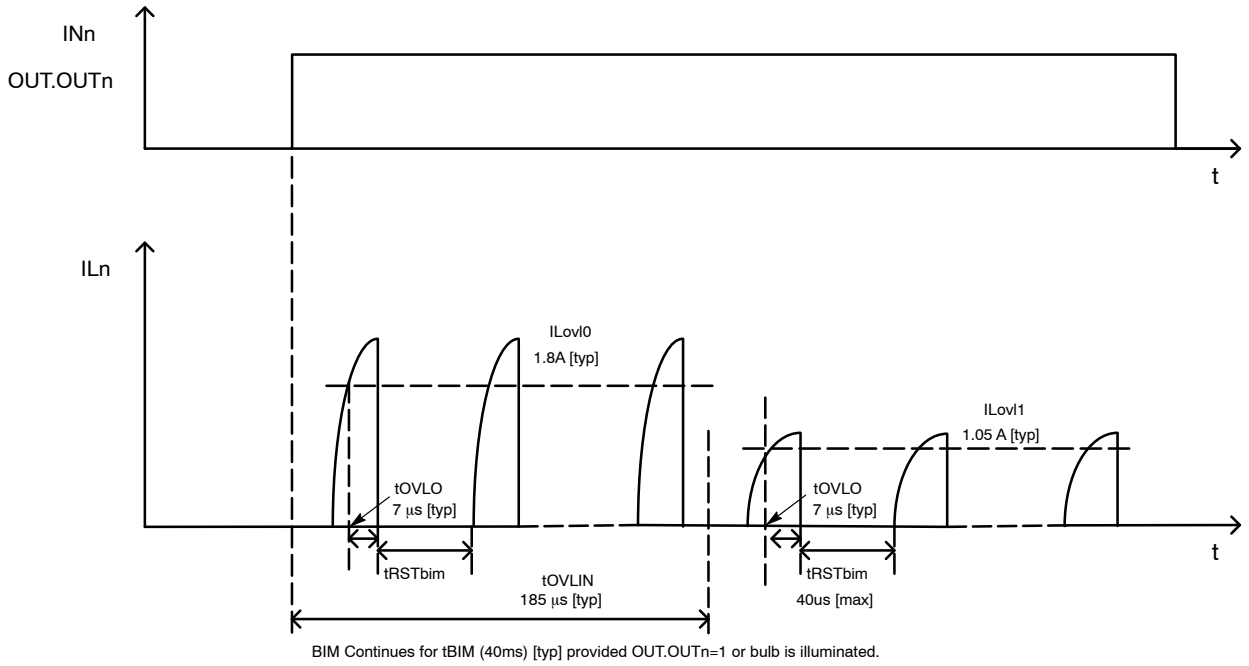


Figure 19. Bulb In−rush Mode

Output Clamping

Internal protection is provided for the output drivers for the maximum drain to source voltage and the absolute maximum voltage from the output to negative voltages which occurs on OUTx when inductive loads are turned off.

Protection for Q1 drain to source is provided by D1, D2, and Rgs.

Protection for negative clamp voltages is provided by Rgs, D3, and D4.

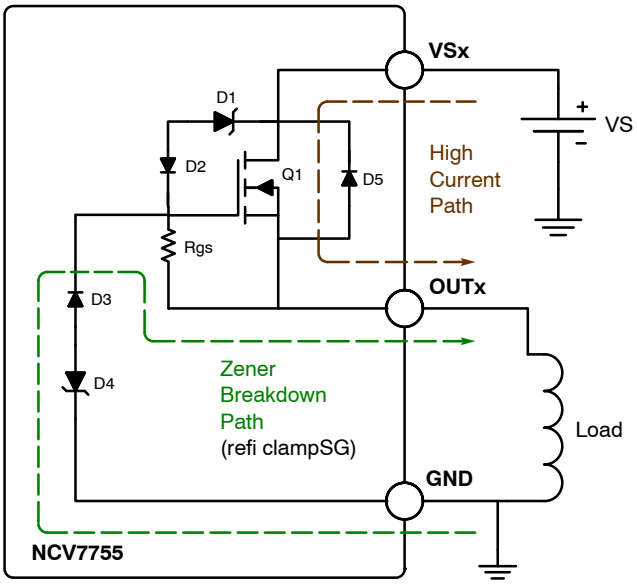


Figure 20. Output Clamp (Normal Operation)

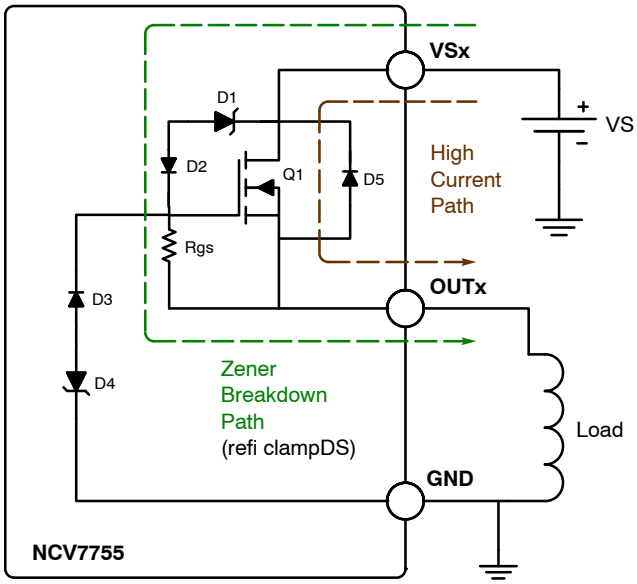


Figure 21. Output Clamp (at High Voltage)

Outputs in Parallel

The NCV7755 was designed for operation with the capability to parallel some of the outputs for increased current handling for an individual load. This is not recommended for most other integrated circuits due to the asynchronous turn−off of paralleled outputs causing undo stress to the last channel on. The channels in the list below are allowed to run in parallel by programming the Hardware Configuration Register (HWCR.PAR) which can deactivate both channels synchronously during an overload or overtemperature event.

Please note during Limp Home Mode only Channel 2 and Channel 3 are active. Because a parallel combination of channels 2 and 3 is not allowed, there is no provision for parallel outputs during Limp Home Mode.

Parallel Combination		
Channel Number	Channel Number	HWCR.PAR Bit address
0	2	0
1	3	1
4	6	2
5	7	3

Fault Detection

Overload

Two overload current thresholds (ILovl0 & ILovl1) triggered by a turn−on command support the designer in driving highly capacitive loads. A higher initial current threshold (ILovl0) ignores potential in−rush events caused by high capacitance. The 2nd level supports maintenance of lower IC temperature levels during any shorted events while still providing proper operation.

This multi−level threshold strategy is implemented whenever the driver is active on. When operating in Bulb−Inrush mode (BIM), the auto−restart feature will also be active.

Overload detection conditions are latched off and require a SPI command to reactivate the effected output.

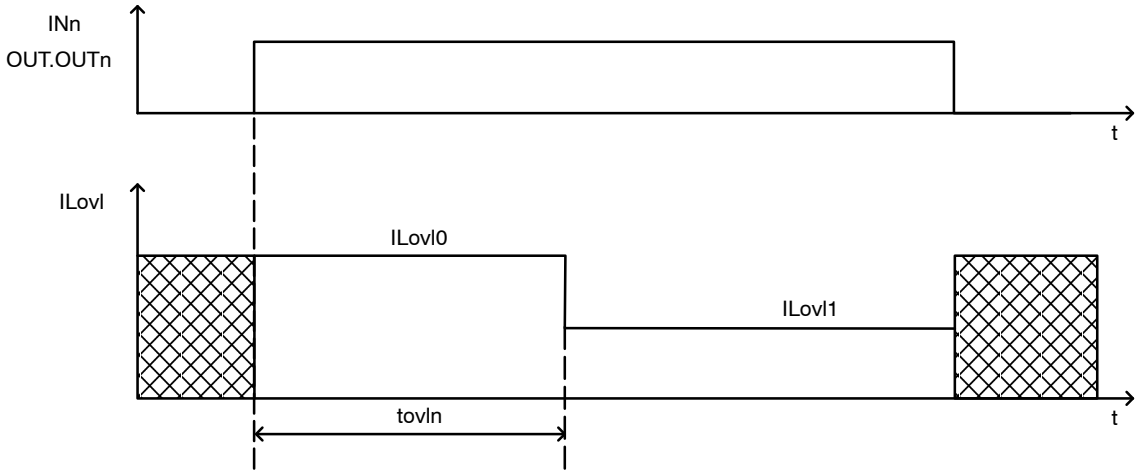


Figure 22.

Thermal Shutdown − Individual thermal sensors are provided for each channel. A breach of the thermal shutdown threshold will latch the channel off and set the diagnostic bit ERRn for the channel. Clearing the error bit is done by setting the corresponding HWCR_OCL.OUTn bit to “1”. HWCR_OCL.OUTn is cleared after the error bit is cleared and the channel will accept commands to turn on.

During Bulb Inrush Mode, the output is “latched” off when the thermal threshold is breached, and will auto−restart once the thermal sensor no longer detects a fault.

FAULT REPORTING

ERRn, Overload & Overtemperature

Short to Ground – Overload conditions or Overtemperature conditions latch off the affected channel and the diagnostic bit ERRn is set. Reactivation must be via the SPI commands in normal operation using HWCR_OCL.OUTn. The logic inputs will not reset the latch. Limp Home Mode however utilizes an output restart time.

After a breach of the ILovl0 or Ilovl1 level the channel is latched off and an error diagnostic bit is set (ERRn). Clearing the error bit is done by setting the corresponding HWCR_OCL.OUTn bit to "1". HWCR_OCL.OUTn is cleared after the error bit is cleared and the channel will accept commands to turn on.

Short to Battery – An output shorted to battery will be detected with the Open Load output off circuitry. When the device is off, the expectation is for the load to hold the output pin low. If a short to battery exists, the pin will be pulled high and an open circuit will be reported.

- OverLoad – Reference the Fault Detection section
- Open Load – Reference the Fault Detection section
- Thermal Shutdown – Reference the Fault Detection section

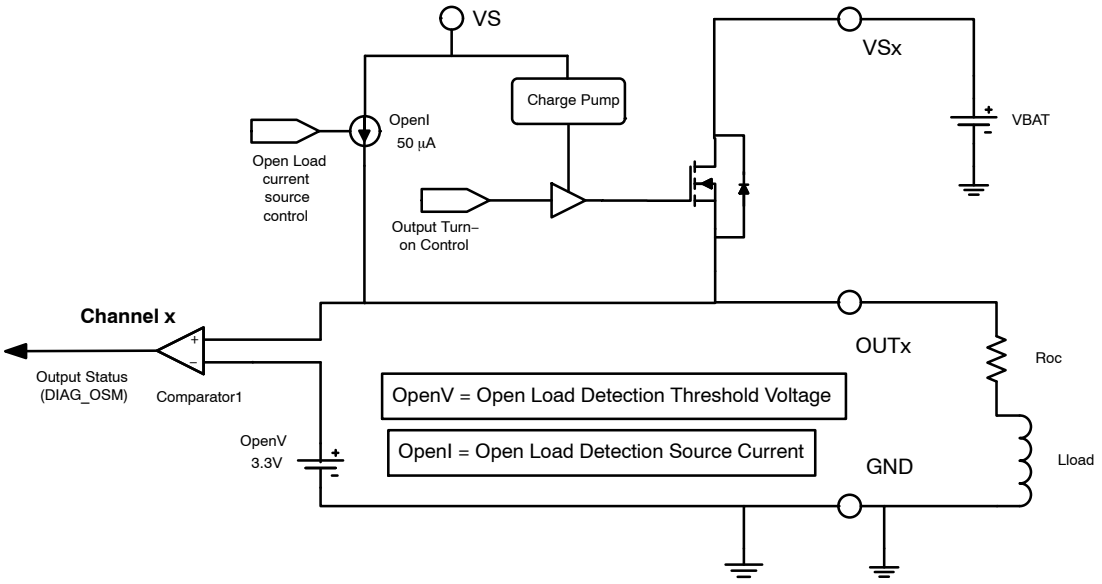


Figure 23. Open Load at OFF

Open Load

Open Load diagnostics are active for an open load in the on state or open load in the off state.

On State – Open load at on is detected if the output current is less than 6 mA (typ) and 10 mA over the temperature range.

Off State – Utilizes an internal current source for detection and is reported as a state condition in the Output Status Monitor. The output with a load present in the off state should be low. If the OpenI current source pulls OUTX high when enabled by DIAG_IOL.OUTn, an open circuit condition is reported.

Open Load at OFF

Open load detection is often a system requirement for reporting a malfunction to the host controller. Board level deviations such as dendrites between traces can effect this measurement. A dendrite between the output pin and ground will reference a voltage into the Output Status Voltage Threshold Monitor from the Output Status Monitor diagnostic Source Current during an open load off diagnostic event (with an open load) from the dendrite impedance.

An impedance range is established with the extremes of the threshold voltage (OpenV) and the current source (OpenI) to eliminate false opens or failure to report an open.

$$\text{Open Load Impedance} = \frac{\text{OpenV}}{\text{OpenI}} \quad \text{Impedance min} = \frac{3.0\ \text{V}}{100\ \mu\text{A}} = 30\ \text{k}\Omega \quad \text{Impedance max} = \frac{3.6\ \text{V}}{25\ \mu\text{A}} = 144\ \text{k}\Omega$$

Open Loads will be detected between the 30 kΩ and 144 kΩ range.

Acceptable loads will be < 30 kΩ.

Acceptable impedances between printed circuit board traces will be > 144 kΩ.

In normal operation, when OpenI is active, the current is low and should not be high enough to trip an open circuit flag. OUTx should be held close to ground via Roc + Lload. If Roc + Lload are missing, OpenI will pull OUTx above the OpenV threshold and signal an open load.

Open Load at ON

Open Load at ON is controlled by the DIAG_OLONEN.MUX bits in the DIAG_OLONEN register. The default setting after reset is not active. DIAG_OLON.OUTn is set and mirrored into the Standard Diagnostic (bit OLON) if the output current is less than the Open Load ON Threshold Current. This is synonymous to an under load condition.

DIAG_OLONEN.MUX can be commanded on for a direct channel diagnostic or a diagnostic loop. Direct Channel diagnostic uses direct drive and is defined as control via SPI (Power output control register or control is mapped to IN0 (MAPIN0.outn) or IN1 (MAPIN1.outn). Diagnostic loop is programmed via SPI to the DIAG_OLONEN register (DIAG_OLONEN.MUX = 1010_B).

When operating in a direct channel mode, a detected open load will set the corresponding DIAG_OLON.OUTn bit and reset all the other bits in the DIAG_OLON register. Bits are updated upon register reading.

For operation in a diagnostic loop, DIAG_OLEN.MUX should be programmed with the value 1010_B. All channels are checked for Open Load at ON when operating in this mode. DIAG_OLON.OUTn is updated upon completion of each channel diagnostic. Value 1111_B (default) is set back in DIAG_OLONEN after the last channel is evaluated.

Direct Channel Diagnostic

For Direct Channel Diagnostic, the device requires:

1. Time for the Internal Frequency Sync (10 μs [max]) (t_{SYNC})
2. Time for the output to turn on (tDIAGwait) (35 μs [max]). ($t_{DIAGwait}$) Open Load Monitor is now active.
3. Programming time for Open Load ON Diagnostic Control (DIAG_OLONEN.mux). (Time not specified here as this involves external control times)
4. Once step #3 is performed some Settling Time (tSETopnON) is required for the Open Load at ON Monitor (DIAG_OLON.OUT) to be available (40 μs [max] ($t_{SETopnON}$)

Once available, an Open Load at ON corresponding to a channel in the Open Load at ON Diagnostic Control Register (DIAG_OLONEN.MUX) will be reported upon request. Only one channel is available at a time. All other channels will report “0”.

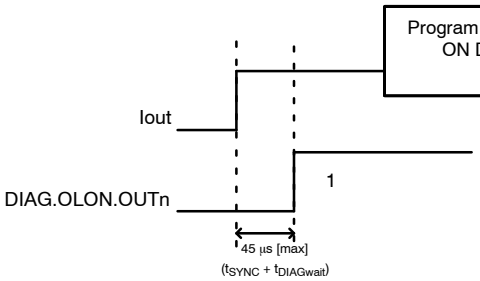


Figure 24. Direct Channel Time for Monitor Active

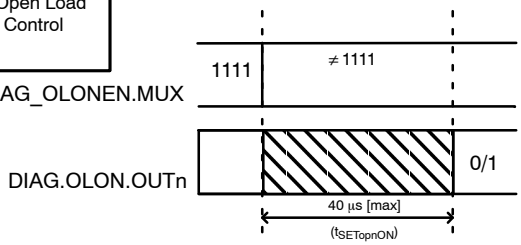


Figure 25. Open Load ON Diagnostic Control Settling Time

When operated with the output previously commanded on, the time delay from fault occurrence to report in the register is the Open Load ON Channel Switching Time (20 μs [max]) ($t_{SWTopnON}$).

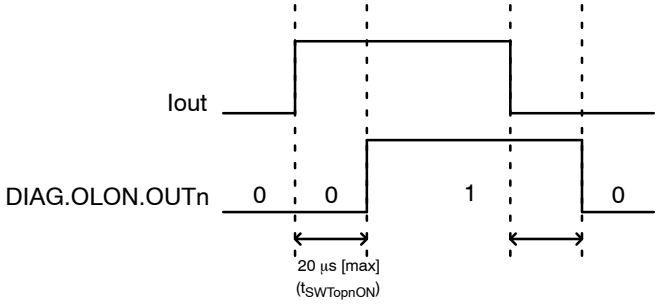


Figure 26. Direct Channel Event Delay Time

Diagnostic Loop

A diagnostic loop systematically tests all channels for Open Load at ON when 1010_B is programmed into the Open Load at ON diagnostic control (DIAG.OLONEN.MUX).

1. Direct Channels are tested first.
   Channels are checked in numerical sequence with off channels set to “0” after diagnostic.

   The timing for completion of the 1st diagnostic is different than the rest. This includes the internal synchronization time (t_{SYNC}) and the Settling Time ($t_{SETopnON}$) (50 μs [max])

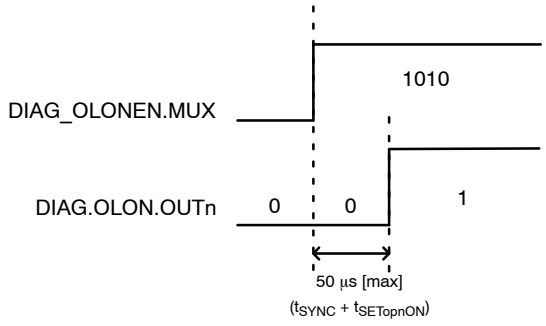


Figure 27. First Direct Channel Diagnostic Completion Timing

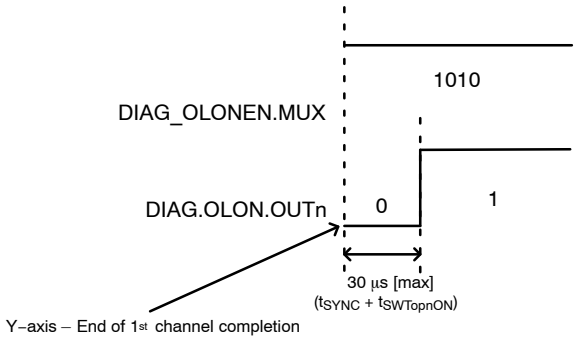


Figure 28. Subsequent Channel Loop Delay Times

Subsequent delay times after the 1st diagnostic are triggered by the internal synchronization time (t_{SYNC}) plus the Channel Switching Time ($t_{SWTopnON}$) (30 μs [max]). This sequence is repeated until all channel are evaluated.

2. Channels configured for PWM operation are tested second with PWM Generator 0 tested first followed by PWM Generator 1

The timing for completion of the 1st diagnostic is triggered by the channel activation ON state from the PWM Generator. Timing includes Settling Time for the trigger event ($t_{SETopnON}$) (40 μs [max]) plus any possible OFF state programmed by the user in the PWM generator (tPWM) as a low duty cycle event.

Once the PWM generator goes high there is a time delay for Waiting Time before mux activation ($t_{MUXopnON}$) (76 μs [max]) plus Channel Switching Time ($t_{SWTopnON}$) (20 μs [max]).

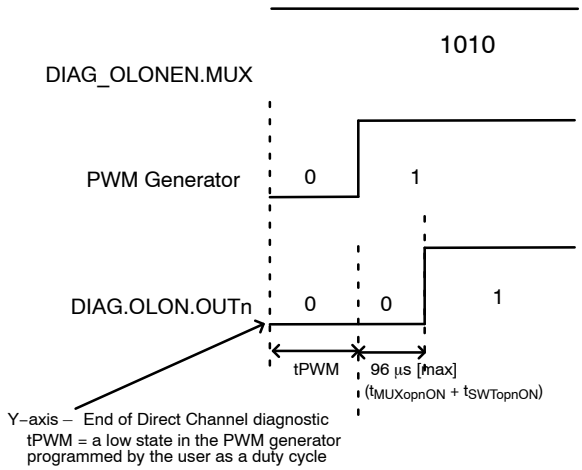


Figure 29. First MUX Channel diagnostic Completion Timing

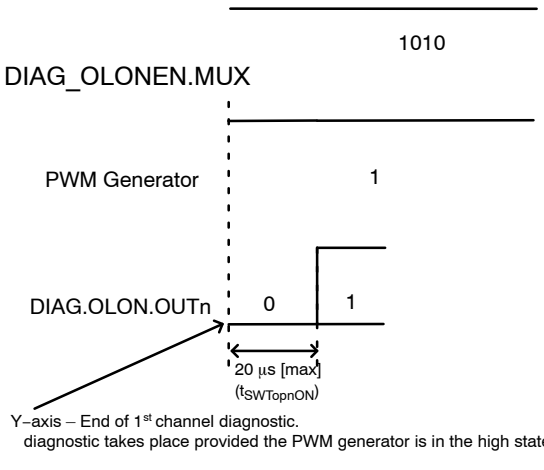


Figure 30. Subsequent Channel Delay Times

Channel Switching Delays ($t_{SWTopnON}$) (20 μs [max]) are linked to all the subsequent channel diagnostic for Open Load at ON. The PWM Generator must be in its high state for diagnostic.

A channel in its off state must wait as per the first channel diagnostic which includes the delay for Waiting Time before mux activation ($t_{MUXopnON}$) (76 μs [max]) plus Channel Switching Time ($t_{SWTopnON}$) (20 μs [max]). This is the minimum on time for a reliable diagnosis. Operation at low duty cycle in PWM mode may not meet this requirement. The user must insure the minimum on time is met for an accurate Open Load at ON reading.

If subsequent channels do not have the PWM generator high, the 1st mux Channel diagnostic Completion Timing applies.

Table 3. OLON BIT IN THE STANDARD DIAGNOSTICS REGISTER

DIAG_OLON.MUX	OLON Bit Description
$0000_B \rightarrow 0111_B$	Displays the Open Load at ON status for requested channel.
1010_B	"OR" combination of all bits in the DIAG_OLON register while loop is running.
1111_B	Show the latest diagnostic results
1000_B , 1001_B , 1011_B , 1100_B , 1101_B , 1100_B	Reserved – Should not be used. OLON Bit will set to "0".

FAULT HANDLING CHART

Fault	Driver Condition during Fault	Driver Condition after Parameters within Specified Limits	Fault Reporting	Output Register Clearing Requirements
Overload	Channel Latch Off	OUTn is off	ERRn is set	SPI clearing with HWCR_OCL.OUTn. Set to "1". After cleared, the output will immediately turn on if OUT.OUTn = 1
Overload (BIM Mode)	Autorestart for 40 ms	Normal Operation	ERRn is reported periodically in Bulb In−Rush restart time	No register reporting if bulb starts within 40 ms. Else wise reference "Overload" Fault
Open Load Off State	Per setting	Normal Operation	OLOFF is set DIAG_OSM is set	Load re−connected. or transition to the ON state.
Open Load On State	Per setting	Normal Operation	OLON is set	Load re−connected.
Thermal Shutdown	Channel Latch Off	OUTn is off.	ERRn is set	SPI clearing with HWCR_OCL.OUTn. Set to "1". After cleared, the output will immediately turn on if OUT.OUTn = 1.
VS Undervoltage	With VDD = Undervoltage outputs are off	All Outputs off	UVRVS is set	Reading the Standard Diagnostic Register
	With VDD > Undervoltage outputs are per setting	Outputs per setting	UVRVS is set	Reading the Standard Diagnostic Register
VDD Low Operating Voltage	Per setting	Per setting	LOPVDD is set	Reading the Standard Diagnostic Register
Transmission Error	Previous state	Per command	TER is set	CSB low until 1st low−to−high transition on SCLK

Reverse Protection

In reverse polarity (OUTx > VSx), each channel will be on at nearly the forward Rdson for both VS operational (Figure 31 when commanded on) and at ground (Figure 32) or will conduct through the body diode (Figure 31 when commanded off).

VS Powered

Parametric deviations, but no functional deviations of unaffected channels are possible during the reverse polarity event with VS Powered.

The reverse polarity channel stays in the ON (output = Rdson) or OFF (output = body diode) state as programmed before reverse polarity with VS powered (Figure 31). ON / OFF state (Rdson or body diode) is still programmable while in reverse polarity. Current in the output channels is limited by only the external loads. Limiting for VDD and logic pins (IDLE, IN0, IN1, CSB, SCLK, SI, SO) require their own external protection (external series resistors) typically 100 ohms for VDD, 500 ohms for the SPI pins (CSB, SCLK, SI, SO), 4.7 kohms for IN0 & IN1, and (4.7 kohms + 10 ohms) for IDLE in the application.

Thermal Shutdown with VS Powered

A thermal shutdown event will be sensed whenever VS is powered and set the appropriate ERRn bit during inverse current. The IC will control (turn off) the output transistor during thermal shutdown as the gate drive is active with VS powered. The system effect will be the output transistor will conduct at nearly the forward Rdson (when commanded on) or the output will conduct through the body diode between OUTx and VSx (when commanded off) prior to a thermal shutdown event. When a thermal event is sensed, the output transistor will be commanded off and the output will conduct through the body diode of the output transistor.

Overcurrent with VS Powered

Overcurrent is not active during inverse current with VS powered.

VS at Ground

In reverse polarity with VS also at ground, (Figure 32) the device will automatically sense the condition and turn on with Rdson comparable to the forward Rdson characteristic. No on/off control is present. There is no other IC functionality with VS at ground including thermal shutdown or overload.

REVERSE PROTECTION TABLE

VS	ON / OFF Control* (Rdson or body diode)	Output Transistor State	Protection Mechanism (thermal shutdown)	Thermal Shutdown Detection ERR bit	Protection Mechanism (overload detection)
Powered	yes	As commanded (Rdson or body diode)	yes	yes	no
Ground	no	Rdson	no	no	no

* with sufficient VS voltage

Overcurrent with VS at Ground

Overcurrent is not active during inverse current with VS at Ground.

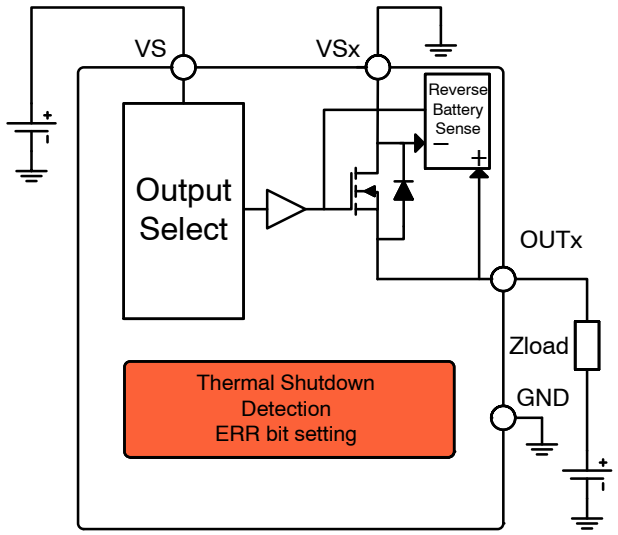


Figure 31. Reverse Polarity Control

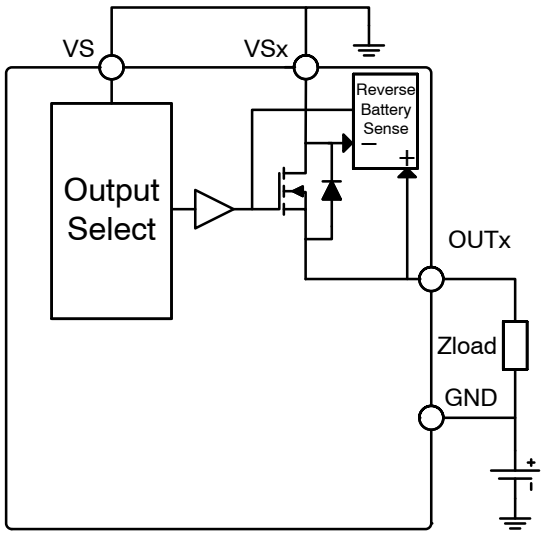


Figure 32. Reverse Polarity Turn−On

Loss of Ground

All channels are guaranteed off during a loss of ground event to insure unwanted activation of external loads with a missing ground connection to the module. Output Current is tested to be less than 2 mA during a loss of ground event.

Logic Inputs

IN0 and IN1 provide logic input control for the outputs for both normal mode and Limp Home Mode. Control is maintained with or without the digital supply input voltage. The NCV7755 mapping function allows for input control for any single output or any multiple outputs. A single output can be controlled by both IN0 and IN1 as an OR'd condition.

Mapping

There are two mapping functions allowed in the NCV7755. The first is for mapping of IN0 and IN1 to any assigned outputs. The second is for mapping the two PWM generators to any assigned outputs.

Mapping of IN0 and IN1

IN0 and IN1 are designed to control two outputs (by default) when in Limp Home Mode (or after POR). IN0 controls channel 2 and IN1 controls channel 3 as an OR'd function between the INx controls, the OUT register and the PWM Generator. The mapping function of the NCV7755 allows connection to other outputs as well as to assign multiple outputs to the same input pin in active mode. The two mapping registers (MAPIN0 & MAPIN1) allow the flexibility for this. The Status Monitor Register (INST) can be monitored to display the logic level of the input pins (also in limp home mode) provided VDD is present. IN0 and IN1 can be controlled with or without VDD present making this ideal for Limp Home applications.

PWM Control

In addition to the two input pins (IN0 and IN1) which provide the capability for PWM control, the NCV7755 also includes two internal independent PWM generators which can be assigned to one or more channels.

The duty cycle and frequency of the internal PWM generators can be adjusted with the PWM Configuration Register (HWCR.PWM, PWM.CR0, and PWM.CR1). The base frequency can be adjusted (−35%, +35%) from the Base Frequency of 102 kHz. The Duty Cycle is adjusted with the PWM Generator 0/1 Configuration Register (with 0.39% resolution) and has 4 options, 100% duty cycle, Base Frequency/256 (corresponding f = 400 Hz), Base Frequency/512 (corresponding f = 200 Hz), Base Frequency/1024 (corresponding f = 100 Hz).

The PWM generator will complete a cycle if commanded to change via the SPI.

Mapping the PWM Generators

Channel mapping of the PWM generator is accomplished via the PWM mapping registers (PWM_OUT and PWM_MAP). PWM_OUT selects which outputs are to be driven by the PWM generator. PWM_MAP selects which of the two generators is connected to the outputs which are to be driven by the PWM generator.

Daisy Chain

The NCV7755 is capable of being daisy chain connected using the SPI connectivity. While the NCV7755 is a 16−bit device, it can be coupled with other 8−bit SPI devices. It is important to note compatible SPI devices must clock data in on the negative edge of the clock. Reference the SPI diagram.

Serial Connection

Daisy chain setups are possible with the NCV7755. The serial setup shown in Figure 33 highlights the NCV7755 along with any 16 bit device using a similar SPI protocol. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be as per the SPI Protocol table. Additional programming bits should be clocked in which follow this. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.

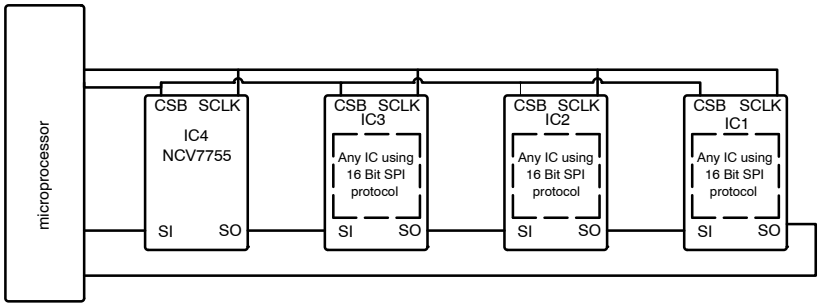


Figure 33. Serial Daisy Chain

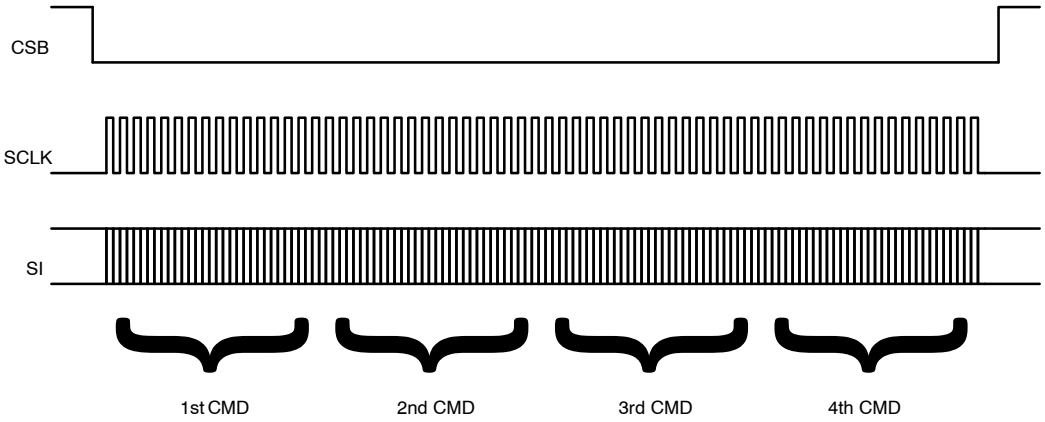


Figure 34. Serial Daisy Chain Timing Diagram

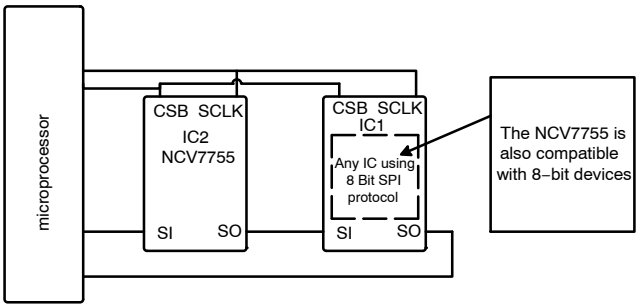
Table 4. SERIAL DAISY CHAIN DATA PATTERN

	CLK = 16 bits	CLK = 32 bits	CLK = 48 bits	CLK = 64 bits
IC4	1st CMD	2nd CMD	3rd CMD	4th CMD
IC3	IC4 DIAG	1st CMD	2nd CMD	3rd CMD
IC2	IC3 DIAG	IC4 DIAG	1st CMD	2nd CMD
IC1	IC2 DIAG	IC3 DIAG	IC4 DIAG	1st CMD
microprocessor	IC1 DIAG	IC2 DIAG	IC3 DIAG	IC4 DIAG

Table 4 refers to the transition of data over time of the Serial Daisy Chain setup of Figure 33 as word bits are shifted through the system. 64 bits are needed for complete transport of data in the example system. Each column of the table displays the status after transmittal of each word (in 16 bit increments) and the location of each word packet along the way.

8−bit Devices

The NCV7755 is also compatible with 8 bit devices due to the features of the frame detection circuitry. The internal bit counter of the NCV7755 starts counting clock pulses when CSB goes low. The 1st valid word consists of 16 bits and each subsequent word must be comprised of just 8−bits (reference the Frame Detection Section).



NOTE: *Compatibility* Note the SCLK timing requirements of the NCV7755. Data is sampled from SI on the falling edge of SCLK. Data is shifted out of SO on the rising edge of SCLK. Devices with similar characteristics are required for operation in a daisy chain setup.

Figure 35. Serial Daisy Chain with 8−bit Devices

Input Parallel Connection of ICs in a Daisy Chain Configuration

A more efficient way (time focused) to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. The Figure below shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a serial daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel control setup eliminates that requirement, but at the cost of additional control pins from the microprocessor for each individual CSB (chip select bar) pin for each controllable device. Serial data is only recognized by the device that is activated through its respective CSB pin. The Figure below shows the waveforms for typical operation when addressing IC1.

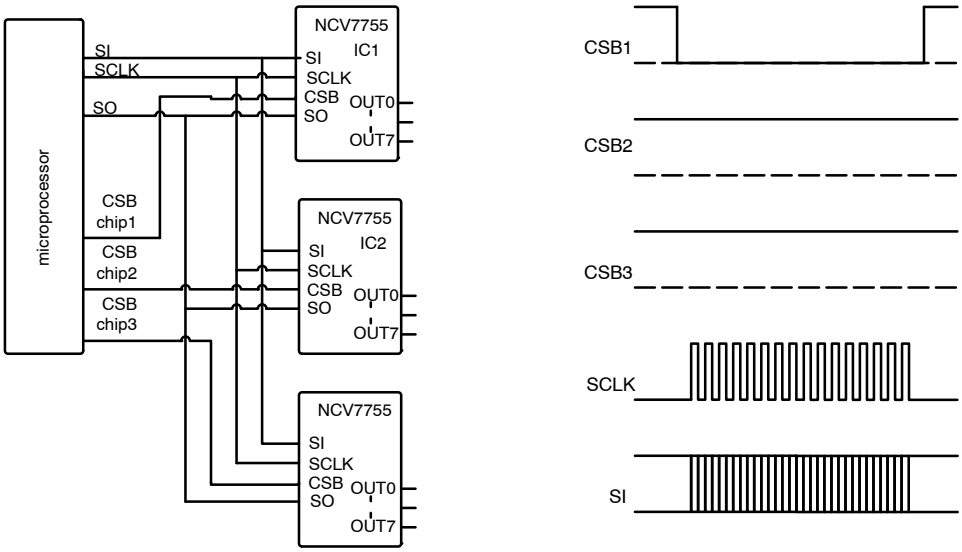


Figure 36.

SPI Communication

The SPI protocol works in conjunction with the 4 SPI pins, CSB, SCLK, SI, & SO.

- CSB – Chip Select Bar
  A high to low transition signals the IC that data is about to be clocked into the IC. Data is then clocked in via the SCLK and SI pins. Data completion is signaled by a low to high transition on the CSB pin
- SCLK – Serial clock input pin. Data bits from SI are shifted into the IC on the falling edge of SCLK. Data bits are shifted out of SO at the same time data bits are shifted into the IC. SCLK must be low when CSB makes a transition
- SI – Serial input pin. Data is shifted into the IC via the SI pin with the SCLK pin. The MSB (most significant pin) data is shifted in first. The Register Structure is composed of address and data bits with read/write designators
- SO – Serial output pin. The Diagnostics Register is clocked out of SO at the same time SI is input into the SI pin. The exception here is when operating in a daisy chain configuration when the 16−bit word clocked out the intended data for the next serial device

SPI Diagnostics

All 16 bit words from the SPI Diagnostics are read only bits. The SPI Diagnostics are returned following a received command.

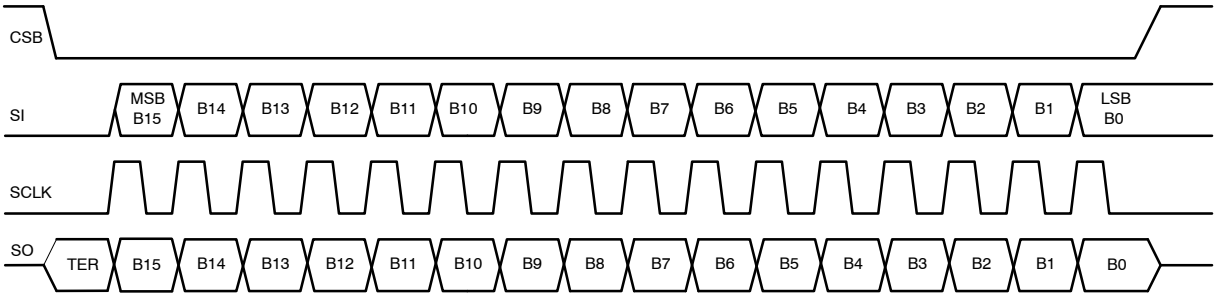


Figure 37. Serial Peripheral Interface

The timing diagram highlighted above shows the SPI interface communication.

TER information retrieval is as simple as bringing CSB high−to−low. No clock signals are required although SI must be low when reading TER.

NOTES:

1. The MSB (most significant bit) is the first transmitted bit
2. Data is sampled from SI on the falling edge of SCLK
3. Data is shifted out from SO on the rising edge of SCLK
4. SCLK should be in a low state when CSB makes a transition
5. SI should be in a low state during TER retrieval time

SPI Operation

SPI operation works by sending the previous response frame back when a new frame has been clocked in unless

1. There was a transmission error in the previous frame
   a. The response is the Standard diagnostic with the TER
2. Coming out of VDD POR.
   a. The response is the INST register with the TER (8680h)
3. There is a syntax error.
   a. The response to “11” MSB is the Standard diagnostic
   b. The response to “00” MSB is the Standard diagnostic
   c. The response to “reserved” or “not used” registers is the Standard diagnostic.

   reference the
   Register Structure for 2 bit designators
   write commands = “10” MSB
   read commands = “01” MSB

SPI PROTOCOL

	SI	SO
Communication	Frame A	Previous response
	Frame B	Response to Frame A
	Frame C	Response to Frame B
Register Content Sent back to the microprocessor	Write Register A	Previous response
	Read Register A	Standard Diagnostic
	New command	Register A content
Response after a transmission error	Frame A (error in transmission)	Previous response
	New command	Standard Diagnostic +TER
Response with VDD < POR	Frame A	SO = hi impedance
Response after VDD POR	Frame B	INST Register +TER (8680h)
	Frame C	Response to Frame B
Response after Command Syntax or addressing Error	Frame A (error)	Previous Response
	New command	Standard Diagnostic

SPI Register Reset

The following will reset the SPI registers.

Device transitions to Sleep Mode.

This includes both of the conditions:

a. INx and IDLE are all = “0”

b. Both VDD and VS are in undervoltage

NOTE: Execution of a reset command (HWCR.RST = “1”) will clear (turn off) the outputs, but the ERR bits will not be cleared for safety reasons.

Frame Detection Transmission Error (TER)

The NCV7755 detects the number of bits transmitted after CSB goes low for verification of word integrity. Bit counts not a multiple of 8 (16 bit minimum) are reported as a fault on the TER bit. The transmission error information (TER) is available on SO after CSB goes low until the first rising SCLK edge in the INST register, and the Standard Diagnostics Register.

In addition to unqualified bit counts setting TER = 1, the bit will also be set by

1. Coming out of UVLO for VDD
2. Transitioning from Limp Home Mode to Active Mode
3. Transitioning from Sleep Mode to Idle Mode

The TER bit is cleared by sending any valid SPI command.

The TER bit is multiplexed with the SPI SO data and OR’d with the SI input to allow for reporting in a serial daisy chain configuration. A TER error bit as a “1” automatically propagates through the serial daisy chain circuitry from the SO output of one device to the SI input of the next.

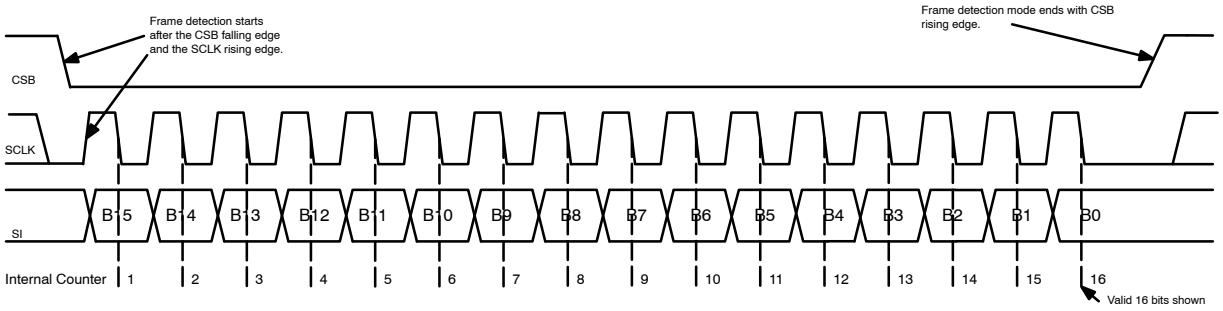
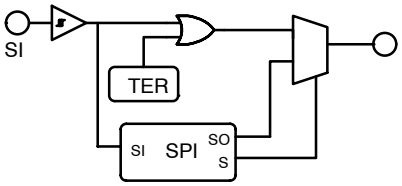


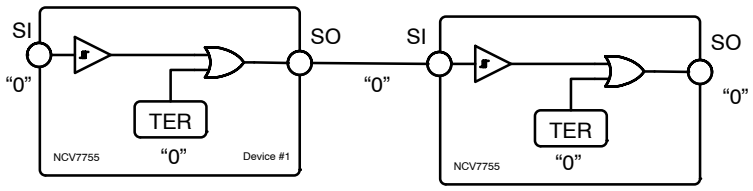
Figure 38. Frame Detection

TER False Reporting

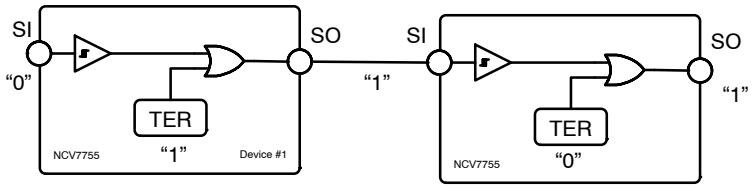
SI should be in a low state during TER status retrieval (from CSB going low to the 1st rising edge of the clock pulse) reporting the previous transmission status. Figure 39 demonstrates what could happen if SI is a one during TER status retrieval. In this situation a "1" on SI propagates to SO regardless of the state of TER. Hence a transmission error (TER) could be reported when it is not true.



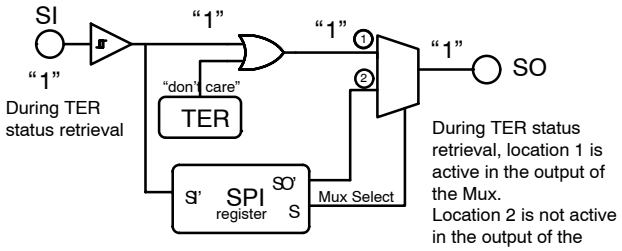
TER SPI Link



TER (no error)



TER Error Propagation



TER False Reporting

NOTE: TER is valid from CSB going low until the 1st low−to−high transition of SCLK to allow for propagation of the SI signal. For proper TER status retrieval, SI should be in a low state.

Figure 39.

REGISTERS

STANDARD DIAGNOSTICS REGISTER (LISTING SUMMARY)

		Description
VS Undervoltage Monitor	UVRVS	Reports undervoltage condition for VS.
VDD Lower Operating Range Monitor	LOPVDD	Reports VDD between 3 V and 4.5 V.
Operative Mode Monitor	MODE	Displays Active, Idle, and Limp modes
Transmission Error	TER	Reports error from modulo 8/16 counter
Open Load ON State Diagnostics	OLON	Reports open load when requested in On mode
Open Load OFF State Diagnostics	OLOFF	Reports open load when requested in Off mode
Overload / Overtemperature Diagnostics	ERRn	Reports Overload or Overtemperature conditions

REGISTERS (LISTING SUMMARY)

Register Name	Bits	Function
Power output control register	OUT.OUTn	Output control On or Off
Bulb Inrush Mode	BIM.OUTn	Sets latchoff or auto restart mode
Mapping IN0	MAPIN0.OUTn	Mapping of IN0 to OUTx
Mapping IN1	MAPIN1.OUTn	Mapping of IN1 to OUTx
Input Status Monitor	INST	Reports transmission bit errors Reports INx input pin status
Open Load Diagnostic Current Control	DIAG_IOL.OUTn	Enables diagnostic current
Output Status Monitor	DIAG_OSM.OUTn	Reports open circuit conditions in OFF state. This reporting is synonymous with short to battery (shorted output FET) conditions Also reports output status in the ON state
Open Load On Monitor	DIAG_OLON.OUTn	Reports open circuit conditions in ON state
Open Load On Diagnostic Control	DIAG_OLONEN.MUX	Sets open load On monitoring
Hardware Configuration Register	HWCR.ACT HWCR.RST HWCR.PAR	Active Mode transitions SPI register reset Sets parallel channel operation
Output Clear Latch	HWCR_OCL.OUTn	Clears the error latch for the selected output
PWM Configuration Register	HWCR_PWM.ADJ HWCR_PWM.PWM1 HWCR_PWM.PWM0	Base PWM frequency adjust PWM Generator 1 activation PWM Generator 0 activation
PWM Generator Configuration 0	PWM_CR0.FREQ	Sets internal divide by clock of PWM generator for Generator 0
	PWM_CR0.DC	Sets PWM Generator 0 duty cycle
PWM Generator Configuration 1	PWM_CR1.FREQ	Sets internal divide by clock of PWM generator for Generator 1
	PWM_CR1.DC	Sets PWM Generator 1 duty cycle
PWM Generator Output Control	PWM_OUTn	Selects active the PWM generator for OUTx
PWM Generator Output Mapping	PWM_MAP.OUTn	Selects one of the two PWM generators

SPI COMMAND SUMMARY

Requested Operation	Frame Sent (SI Pin)	Frame Out (from SO Pin) with the Next Command
Read Standard Diagnostics	$0xxxxxxxxxxxxx01_B$	$0ddddddddddddddd_B$
Write 8−bit register	$10aaaabbcccccccc_B$	$0ddddddddddddddd_B$
Read 8−bit register	$01aaaabbxxxxxx10_B$	$10aaaabbcccccccc_B$
Write 10−bit register	$10aaaaccccccccc_B$	$0ddddddddddddddd_B$
Read 10−bit register	$01aaaaxxxxxxxx10_B$	$10aaaaccccccccc_B$

x = don't care
a = ADDR0 field
b = ADDR1 field
c = register content
d = diagnostic bit

HEX SPI COMMAND QUICK LIST

Register	Read Command	Write Command	Content Written
OUT	4002_H	$80XX_H$	$XX_H = xxxxxxxx_B$
BIM	4102_H	$81XX_H$	$XX_H = xxxxxxxx_B$
MAPIN0	4402_H	$84XX_H$	$XX_H = xxxxxxxx_B$
MAPIN1	4502_H	$85XX_H$	$XX_H = xxxxxxxx_B$
INST	4602_H	(read only)	−
DIAG_IOL	4802_H	$88XX_H$	$XX_H = xxxxxxxx_B$
DIAG_OSM	4902_H	(read only)	$XX_H = xxxxxxxx_B$
DIAG_OLON	$4A02_H$	$8AXX_H$	−
DIAG_OLONEN	$4B02_H$	$8BXX_H$	$XX_H = xxxxxxxx_B$
HWCR	$4C02_H$	$8CXX_H$	$XX_H = xxxxxxxx_B$
HWCR_OCL	$4D02_H$	$8DXX_H$	$XX_H = xxxxxxxx_B$
HWCR_PWM	$4E02_H$	$8EXX_H$	$XX_H = xxxxxxxx_B$
PWM_CR0	5002_H	$90XX_H$ $91XX_H$ $92XX_H$ $93XX_H$	$0XX_H = 00xxxxxxx_B$ $1XX_H = 01xxxxxxx_B$ $2XX_H = 10xxxxxxx_B$ $3XX_H = 11xxxxxxx_B$
PWM_CR1	5402_H	$94XX_H$ $95XX_H$ $96XX_H$ $97XX_H$	$0XX_H = 00xxxxxxx_B$ $1XX_H = 01xxxxxxx_B$ $2XX_H = 10xxxxxxx_B$ $3XX_H = 11xxxxxxx_B$
PWM_OUT	6402_H	$A4XX_H$	$XX_H = xxxxxxxx_B$
PWM_MAP	6502_H	$A5XX_H$	$XX_H = xxxxxxxx_B$

SPI STANDARD DIAGNOSTICS

A Read Standard diagnostics command provides a response with a snapshot of the status of all the monitored faults on the IC. Further fault details (channel fault number etc…) can be reviewed in the subsequent register structure banks.

All 16 bit words from the SPI Diagnostics are read only bits. The SPI Diagnostics are returned with the next command after a *Read Standard Diagnostics Command* $0xxxxxxxxxxxx01_B$ where x = don't care.

Table 5. SPI DIAGNOSTIC TABLE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UVRVS	LOPVDD	MODE		TER	OLON	OLOFF	ERR							

Default after power up or reset is the INST register including TER = 1_B. The TER bit will afterward display the proper transmission state.

Table 6. DETAILED DIAGNOSTICS REGISTER DESCRIPTION

Field	Bits	Description
UVRVS	14	VS Undervoltage Monitor 0_B No undervoltage condition on VS 1_B (default) There was an undervoltage VS condition since the last Standard Diagnostics request
LOPVDD	13	VDD Lower Operating Range Monitor 0_B VDD is above 4.5 V 1_B (default) VDD was below 4.5 V since the last Standard Diagnostics request (Note 19)
MODE	12,11	Operative Mode Monitor 00_B (reserved) 01_B Limp Home Mode 10_B Active Mode 11_B (default) Idle Mode
TER	10	Transmission Error 0_B Previous transmission was successful. (modulo 16 + n*8 where n = 0,1,2…) 1_B (default after reset) Previous transmission failed The first frame after a reset is the INST register with TER = 1_B The second frame (when the Standard Diagnostics Register is requested) is the Standard Diagnostics register with TER = 0_B provided the previous transmission was good
OLON	9	Open Load On State Diagnostics 0_B (default) No Open Load ON detected 1_B Open Load On detected
OLOFF	8	Open Load Off State Diagnostics 0_B (default) No Open Load Off detected 1_B Open Load Off detected
ERR	0–7	Overload / Overtemperature Diagnostics 0_B (default) No failure detected 1_B Overload or Overtemperature was detected

REGISTER STRUCTURE (all registers except PWM_CR0/1)(8 bit DATA register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R= 0 W=1	R=1 W=0	ADDR0				ADDR1		DATA							

18. Read and Write designators require two bits (14 and 15)(r = read, w = write).
19. This bit will be continuously set when operating with a standard 3.3 V supply on VDD.

REGISTER STRUCTURE (PWM_CR0/1 registers)(10 bit DATA register)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R=0 W=1	R=1 W=0	ADDR0				DATA									

20. Read and Write designators require two bits (14 and 15)(r = read, w = write).

Table 7. DETAILED REGISTER STRUCTURE

Register Name	ADDR0	ADDR1	Type	Purpose
OUT	0000_B	00_B	r/w	Power Output Control Register bits (OUT.OUT.n) 0_B (default) Output is Off 1_B Output is On DATA = Channel number 7 to 0 (7:0)
BIM	0000_B	01_B	r/w	Bulb Inrush Mode bits (BIM.OUTn) 0_B (default) Output latches off with overload 1_B Output restarts with overload DATA = Channel number 7 to 0 (7:0)
MAPIN0	0001_B	00_B	r/w	Input Mapping (IN0) bits (MAPIN0.OUTn) 0_B (default) No connection to input pin 1_B Output is connected to the input pin DATA = Channel number 7 to 0 (7:0) Note – Channel 2 has the corresponding bit set to “1” by default
MAPIN1	0001_B	01_B	r/w	Input Mapping (IN1) bits (MAPIN1.OUTn) 0_B (default) No connection to input pin 1_B Output is connected to the input pin DATA = Channel number 7 to 0 (7:0) Note – Channel 3 has the corresponding bit set to “1” by default
INST	0001_B	10_B	r	Input Status Monitor
				TER bit bit (TER) (7) 0_B Previous transmission was successful 1_B (default) Previous transmission failed
				Inx Bit bits (INST.RES) (6:2) – reserved, bits (INST.INn) (1:0) 0_B (default) The input pin is set low 1_B The input pin is set high
DIAG_IOL	0010_B	00_B	r/w	Open Load Diagnostic Current Control bits (DIAG_IOL.OUTn) 0_B (default) Diagnostic current is not enabled 1_B Diagnostic current is enabled DATA = Channel number 7 to 0 (7:0)
DIAG_OSM	0010_B	01_B	r	Output Status Monitor bits (DIAG_OSM.OUTn) 0_B (default) Voutx is less than the Output Status Monitor Threshold Voltage 3.3 V (typ) 1_B Voutx is more than the Output Status Monitor Threshold Voltage 3.3 V (typ) DATA = Channel number 7 to 0 (7:0)
DIAG_OLON	0010_B	10_B	r	Open Load On Monitor bits (DIAG_OLON.OUTn) 0_B (default) Normal operation or diagnostic performed with channel off 1_B Open load On detected DATA = Channel number 7 to 0 (7:0)

Table 7. DETAILED REGISTER STRUCTURE

Register Name	ADDR0	ADDR1	Type	Purpose
DIAG_OLONEN	0010_B	11_B	r/w	Open Load On Diagnostic Control bits (7:4) – reserved, bits 1000_B , 1001_B , 1011_B , 1100_B , 1101_B , 1100_B – reserved bits (DIAG_OLONEN.MUX) (3:0) 0000_B Open Load ON active channel 0 0001_B Open Load ON active channel 1 0010_B Open Load ON active channel 2 0011_B Open Load ON active channel 3 0100_B Open Load ON active channel 4 0101_B Open Load ON active channel 5 0110_B Open Load ON active channel 6 0111_B Open Load ON active channel 7 1010_B Open Load ON Diagnostic Loop Start 1111_B (default) Open Load ON not active
HWCR	0011_B	00_B	r/w	Hardware Configuration Register bits (5:4) – reserved
				Active Mode bits (HWCR.ACT) (7) 0_B (default) Normal operation or device leaves Active Mode 1_B Device enters Active Mode
				SPI Register Reset bits (HWCR.RST) (6) 0_B (default) Normal operation 1_B Reset command executed ERRn bits are not cleared by a reset command for safety reasons
				Channels Operating in Parallel bits (HWCR.PAR) (3:0) 0_B (default) Normal operation 1_B Two neighboring channels have overload and overtemperature synchronized. See section “Outputs in Parallel” for output combinations
HWCR_OCL	0011_B	01_B	w	Output Latch (ERRn) Clear bits (HWCR_OCL.OUTn) 0_B (default) Normal operation 1_B Clear the error latch for the selected output The HWCR_OCL.OUTn bit is set back to “0” internally after de−latching the channel DATA = 7 to 0 (7:0)
HWCR_PWM	0011_B	10_B	r/w	PWM Configuration Register (HWCR_PWM.RES) (3:2) (reserved)
				PWM Adjustment bits (HWCR_PWM.ADJ) (7:4) HWCR_PWM.ADJ Bit **Absolute delta for fINT** **Relative delta between steps** 0000B (reserved) 0001B Base Frequency −35.0% −35.0% (66.3 kHz[typ]) 0010B Base Frequency −30.0% 0011B Base Frequency −25.0% 0100B Base Frequency −20.0% 0101B Base Frequency −15.0% 0110B Base Frequency −10.0% 0111B Base Frequency −5.0% 1000B Base Frequency fINT (102 kHz [typ]) (default) 1001B Base Frequency +5.0% 1010B Base Frequency +10.0% 1011B Base Frequency +15.0% 1100B Base Frequency +20.0% 1101B Base Frequency +25.0% 1110B Base Frequency +30.0% 1111B Base Frequency +35.0% +35.0 (137.7 kHz[typ])

Table 7. DETAILED REGISTER STRUCTURE

Register Name	ADDR0	ADDR1	Type	Purpose
				PWM1 Active bits (HWCR_PWM.PWM1) (1) 0_B (default) PWM Generator 1 not active 1_B PWM Generator 1 active
				PWM0 Active (HWCR_PWM.PWM0) (0) 0_B (default) PWM Generator 0 not active 1_B PWM Generator 0 active
PWM_CR0	0100_B	–––	r/w	PWM Generator 0 Configuration
				CR0 Frequency (PWM_CR0.FREQ) (9:8) 00_B Internal clock divided by 1024 (100 Hz) (default) 01_B Internal clock divided by 512 (200 Hz) 10_B Internal clock divided by 256 (400 Hz) 11_B 100% Duty Cycle.
				CR0 generator on/off control (PWM_CRO.DC) (7:0) 00000000_B PWM generator is off. (default) 11111111_B PWM generator is On (99.61% DC).
PWM_CR1	0101_B	–––	r/w	PWM Generator 1 Configuration
				CR1 Frequency(PWM_CR1.FREQ) (9:8) 00_B Internal clock divided by 1024 (100Hz) (default) 01_B Internal clock divided by 512 (200 Hz) 10_B Internal clock divided by 256 (400 Hz) 11_B 100% Duty Cycle
				CR1 generator on/off control (PWM_CR1.DC) (7:0) 00000000_B PWM generator is off. (default) 11111111_B PWM generator is On (99.61% DC)
PWM_OUT	1001_B	00_B	r/w	PWM Generator Output Control (PWM_OUT.OUTn) 0_B (default) The selected ouput is not driven by one of the two PWM generators 1_B The selected output is connected to a PWM generator DATA = Channel number 0 to 7
PWM_MAP	1001_B	01_B	r/w	PWM Generator Output Mapping (PWM_MAP.OUTn) 0_B (default) The selected output is connected to PWM Generator 0 1_B The selected output is connected to PWM Generator 1 DATA = Channel number 0 to 7 Works in conjunction with PWM_OUT

THERMAL PERFORMANCE ESTIMATES

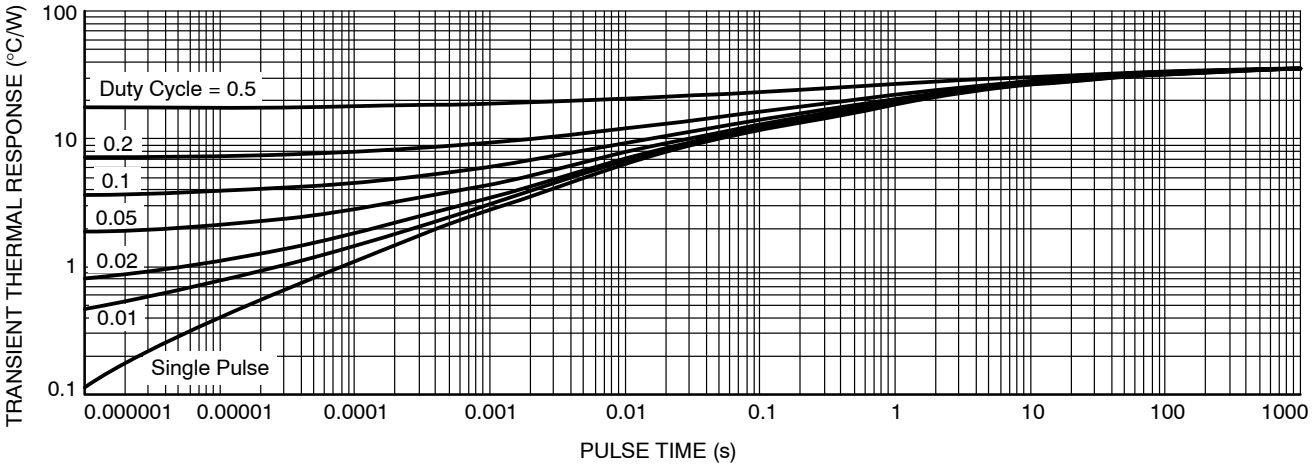
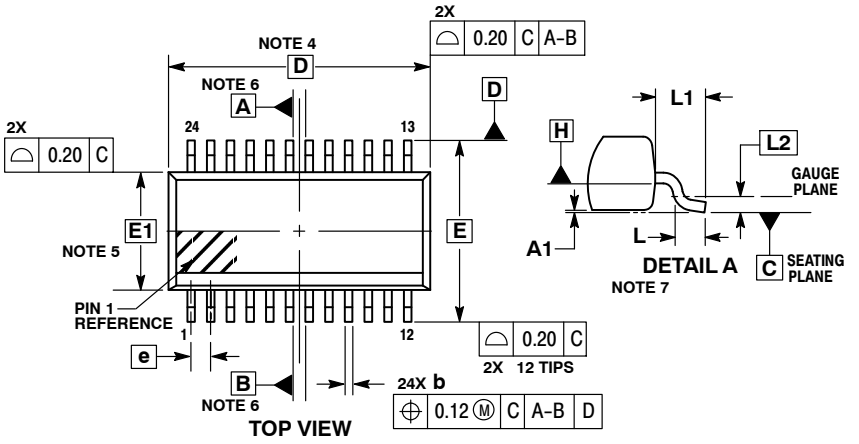
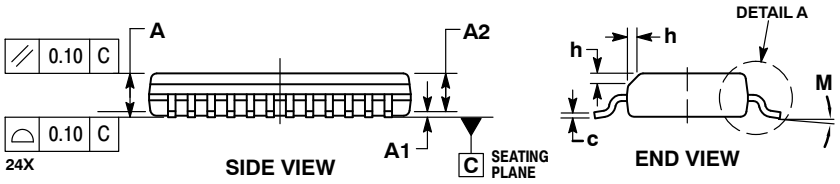


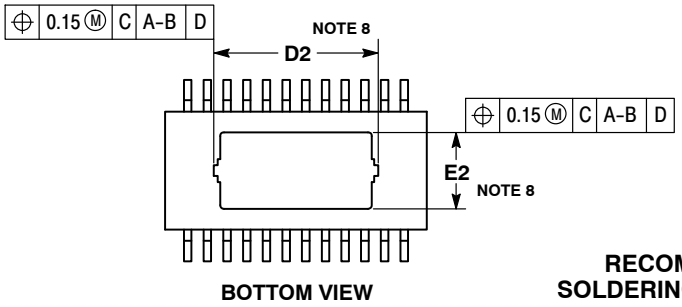
Figure 40. Transient R(t) vs. Pulse Time (JESD51−7, 600 mm^2)

PACKAGE DIMENSIONS

SSOP24 NB EP
CASE 940AK
ISSUE O



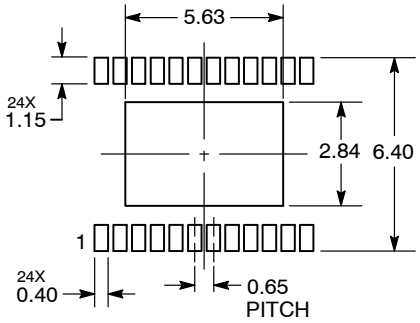




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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