ON Semiconductor

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Low Noise, Audio Dual Operational Amplifier

LM833, NCV833

The LM833 is a standard low−cost monolithic dual general−purpose operational amplifier employing Bipolar technology with innovative high−performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise ($4.5\ nV/\sqrt{Hz}$), 15 MHz gain bandwidth product, 7.0 V/μs slew rate, 0.3 mV input offset voltage with 2.0 μV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no dead−band crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

For an improved performance dual/quad version, see the MC33079 family.

Features

- Low Voltage Noise: $4.5\ nV/\sqrt{Hz}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/μs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	30	V
Input Voltage Range (Note 1)	V_{IR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
ESD Protection at any Pin − Human Body Model − Machine Model	V_{esd}	 600 200	V
Maximum Power Dissipation (Notes 2 and 3)	P_D	500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic).
3. Maximum value at $T_A \leq 85°C$.

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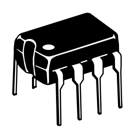
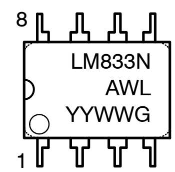
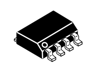
MARKING DIAGRAMS



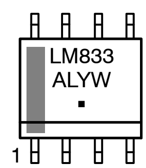
PDIP−8
N SUFFIX
CASE 626



LM833N = Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

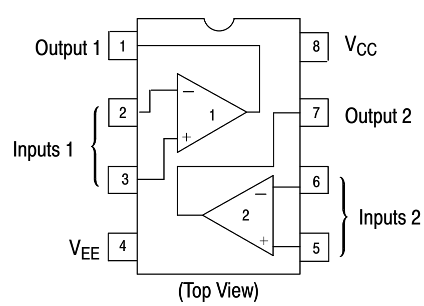


SOIC−8
D SUFFIX
CASE 751



LM833 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_O = 0 V)	V_{IO}	–	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	–	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}	–	10	200	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	–	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	– −12	+14 −14	+12 –	V
Large Signal Voltage Gain (R_L = 2.0 kΩ, V_O = ±10 V)	A_{VOL}	90	110	–	dB
Output Voltage Swing: R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V	 V_{O+} V_{O-} V_{O+} V_{O-}	 10 – 12 –	 13.7 −14.1 13.9 −14.7	 – −10 – −12	V
Common Mode Rejection (V_{in} = ±12 V)	CMR	80	100	–	dB
Power Supply Rejection (V_S = 15 V to 5.0 V, −15 V to −5.0 V)	PSR	80	115	–	dB
Power Supply Current (V_O = 0 V, Both Amplifiers)	I_D	–	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, A_V = +1.0)	S_R	5.0	7.0	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	15	–	MHz
Unity Gain Frequency (Open Loop)	f_U	–	9.0	–	MHz
Unity Gain Phase Margin (Open Loop)	θ_m	–	60	–	°
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	–	4.5	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	–	0.5	–	$pA/\sqrt{Hz}$
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BWP	–	120	–	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	–	0.002	–	%
Channel Separation (f = 20 Hz to 20 kHz)	C_S	–	−120	–	dB

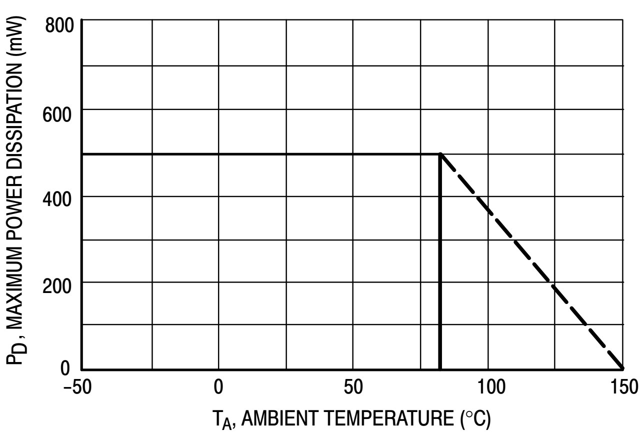


Figure 1. Maximum Power Dissipation versus Temperature

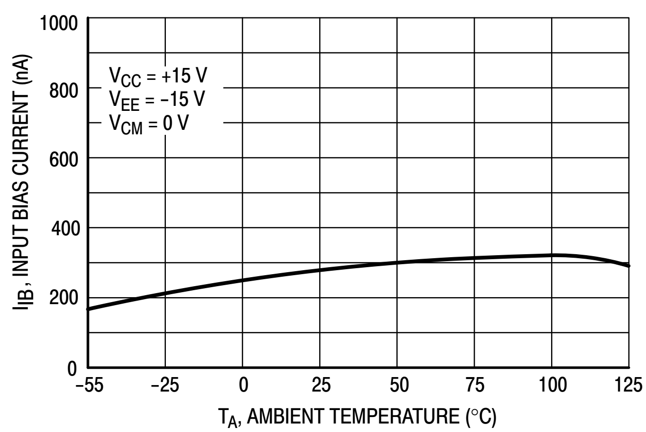


Figure 2. Input Bias Current versus Temperature

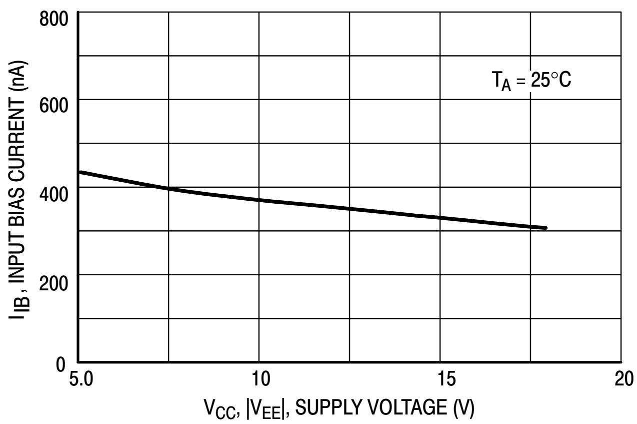


Figure 3. Input Bias Current versus Supply Voltage

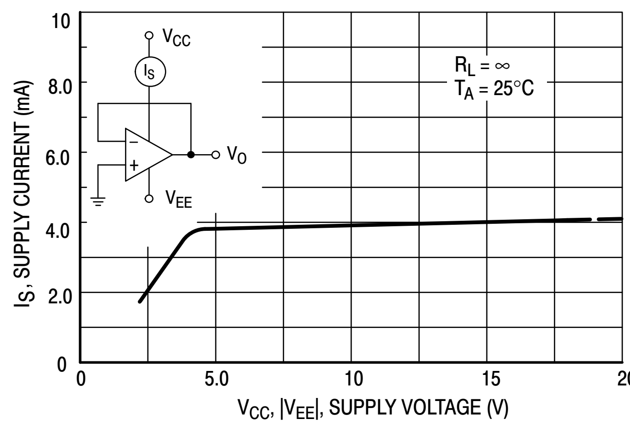


Figure 4. Supply Current versus Supply Voltage

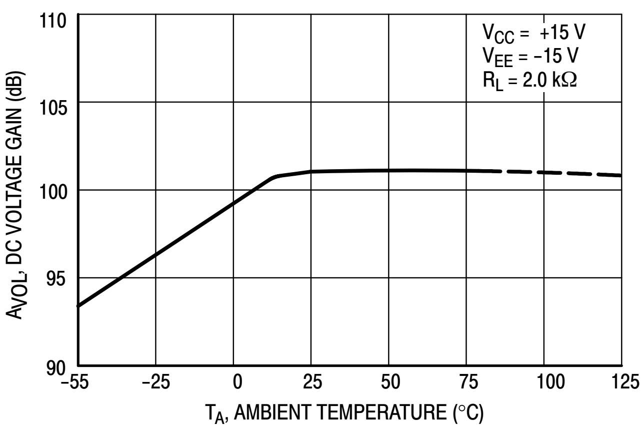


Figure 5. DC Voltage Gain versus Temperature

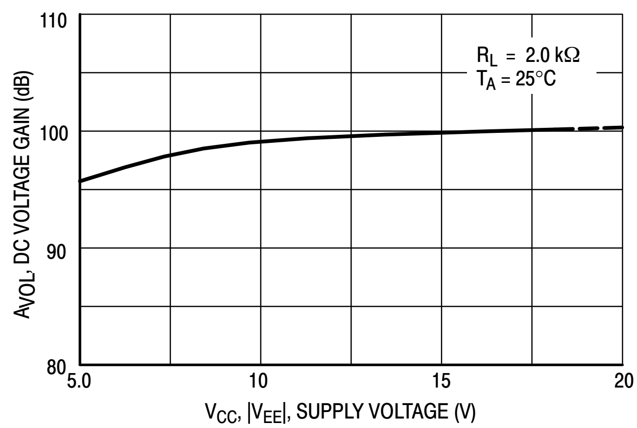


Figure 6. DC Voltage Gain versus Supply Voltage

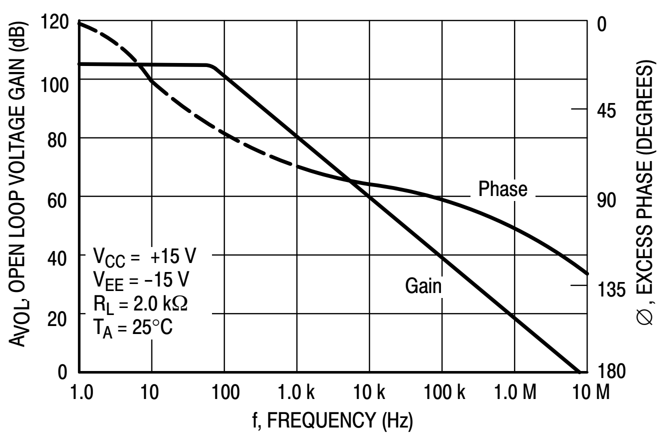


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

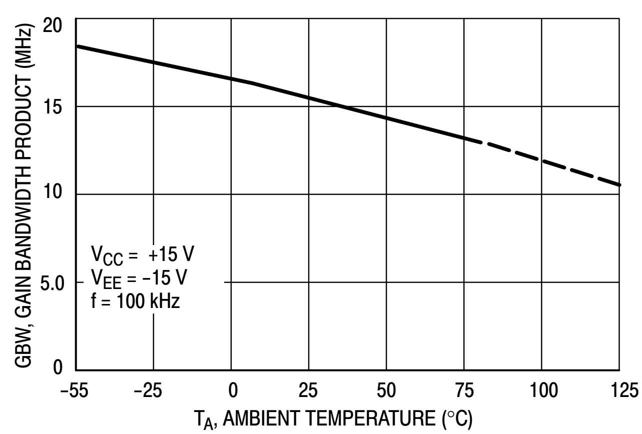


Figure 8. Gain Bandwidth Product versus Temperature

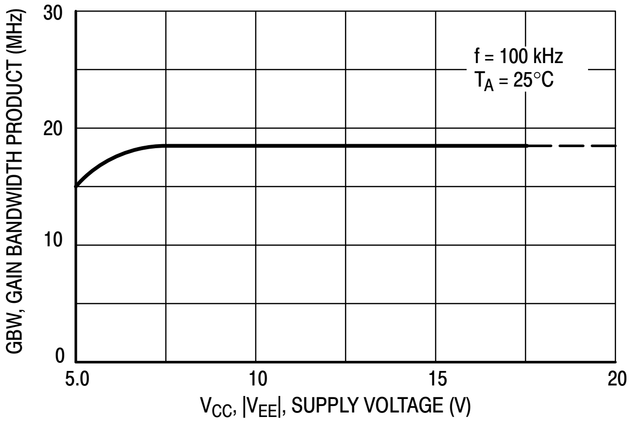


Figure 9. Gain Bandwidth Product versus Supply Voltage

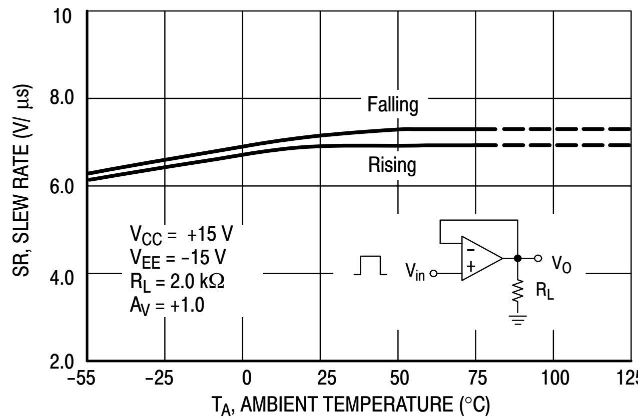


Figure 10. Slew Rate versus Temperature

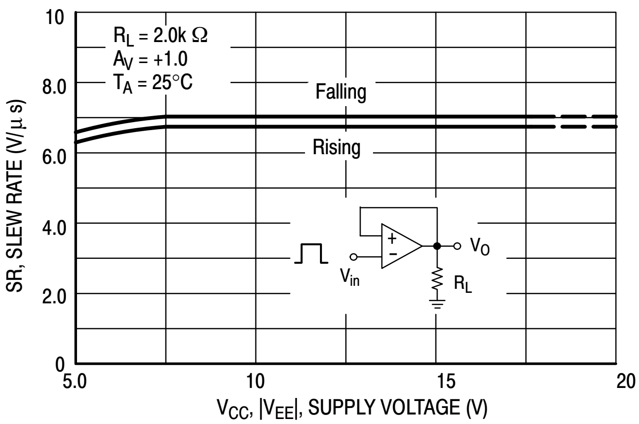


Figure 11. Slew Rate versus Supply Voltage

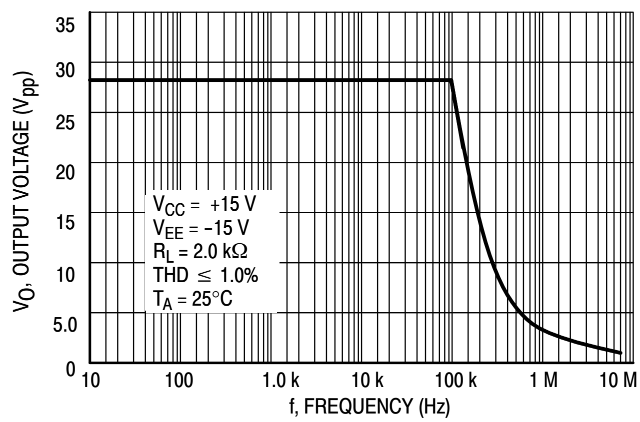


Figure 12. Output Voltage versus Frequency

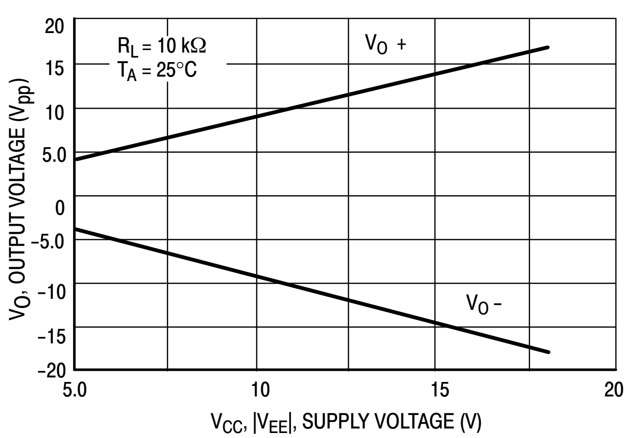


Figure 13. Maximum Output Voltage versus Supply Voltage

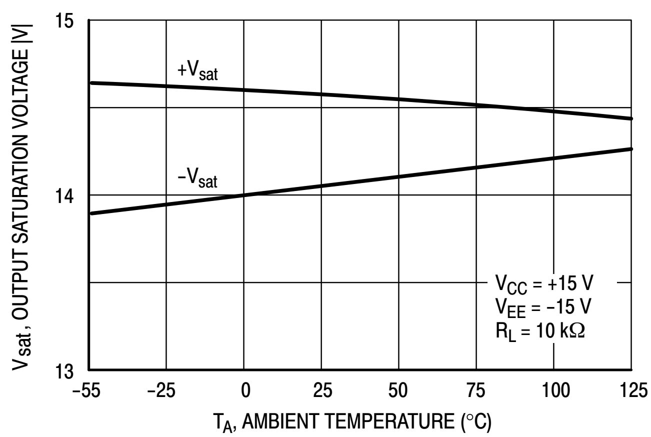


Figure 14. Output Saturation Voltage versus Temperature

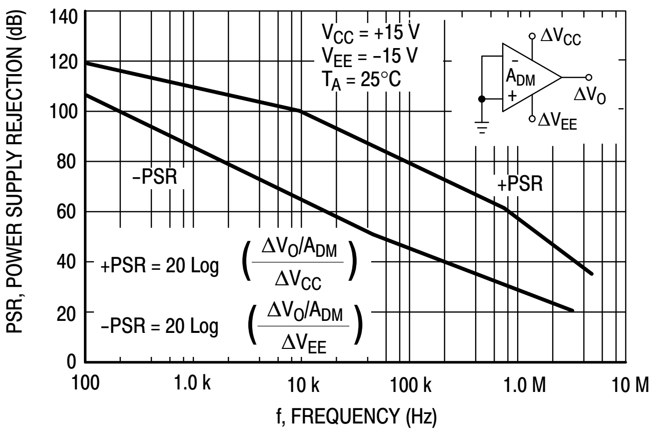


Figure 15. Power Supply Rejection versus Frequency

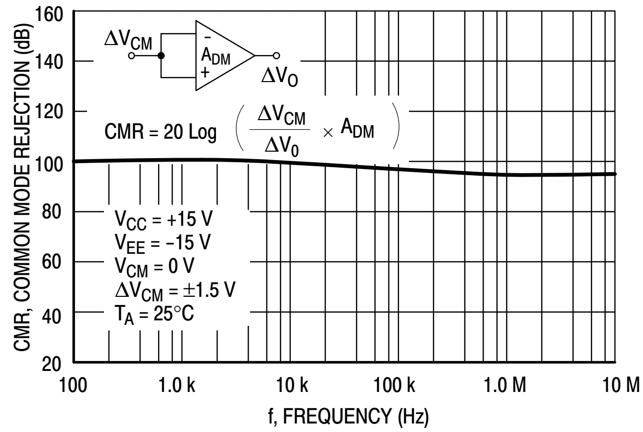


Figure 16. Common Mode Rejection versus Frequency

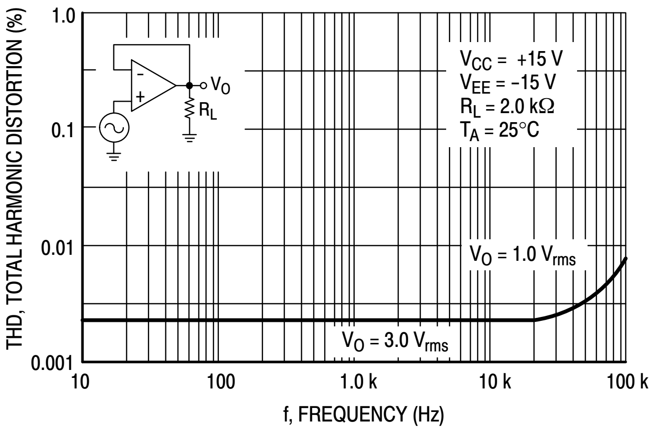


Figure 17. Total Harmonic Distortion versus Frequency

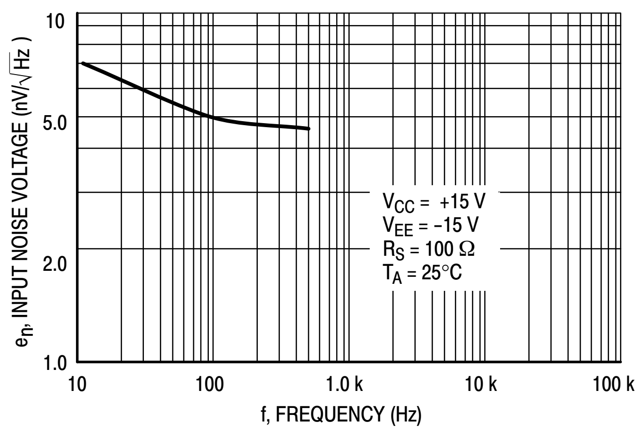


Figure 18. Input Referred Noise Voltage versus Frequency

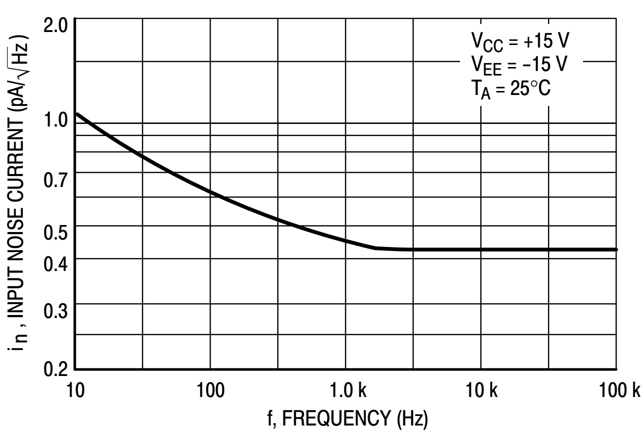


Figure 19. Input Referred Noise Current versus Frequency

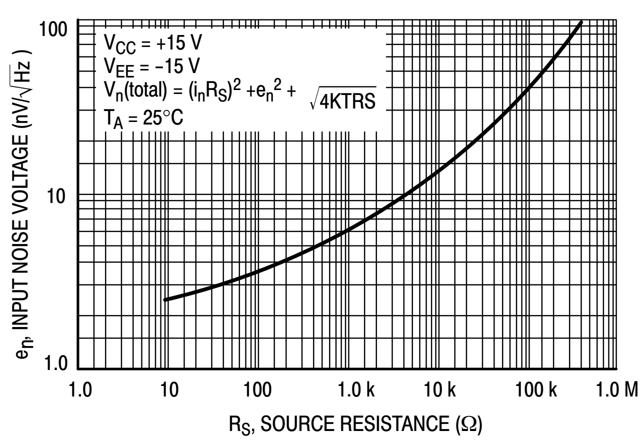


Figure 20. Input Referred Noise Voltage versus Source Resistance

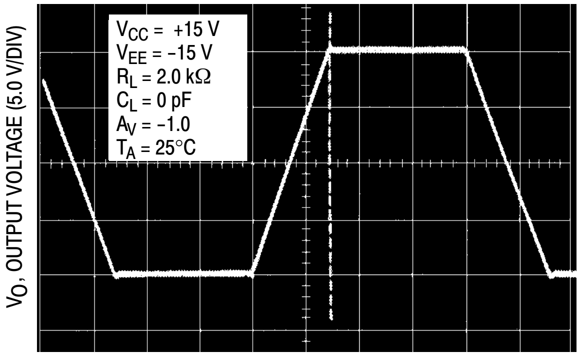


Figure 21. Inverting Amplifier

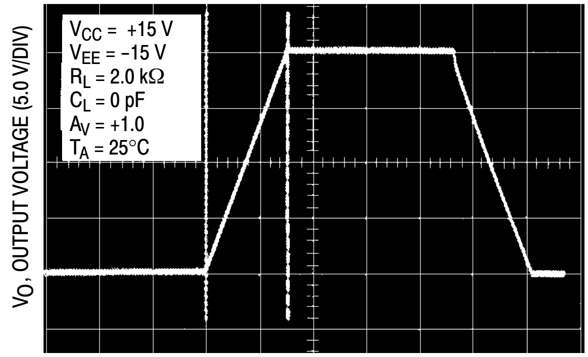


Figure 22. Noninverting Amplifier Slew Rate

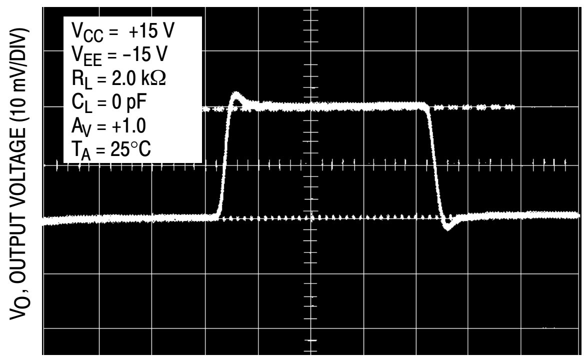


Figure 23. Noninverting Amplifier Overshoot

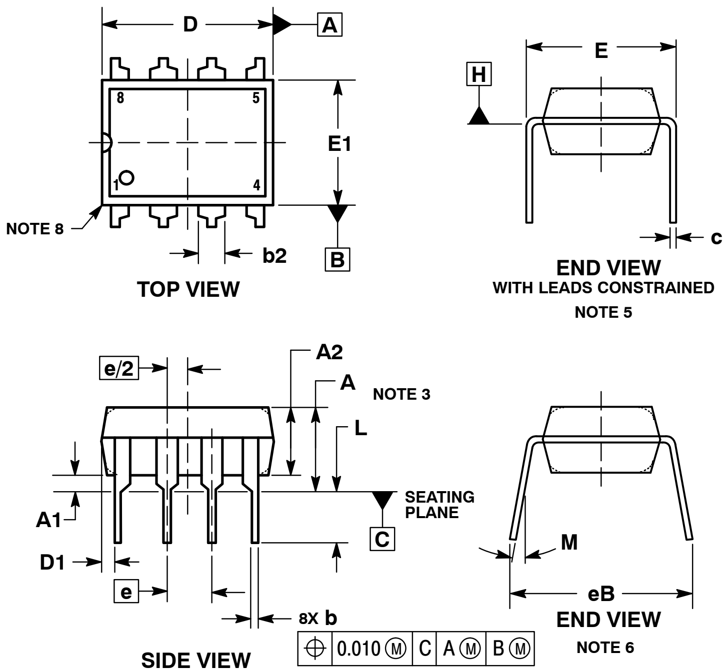
ORDERING INFORMATION

Device	Package	Shipping†
LM833NG	PDIP−8 (Pb−Free)	50 Units / Rail
LM833DG	SOIC−8 (Pb−Free)	98 Units / Rail
LM833DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV833DR2G*	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV prefix indicates qualified for automotive use.

PACKAGE DIMENSIONS

PDIP−8
N SUFFIX
CASE 626−05
ISSUE M

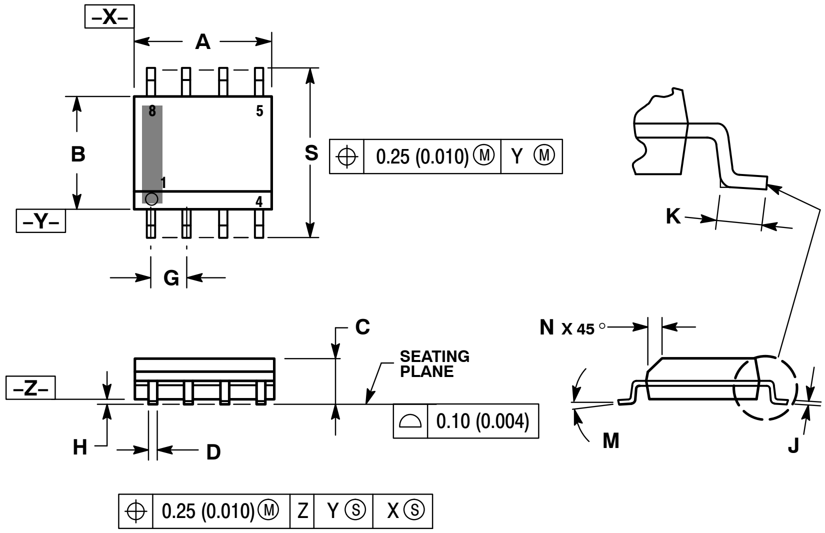


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

PACKAGE DIMENSIONS

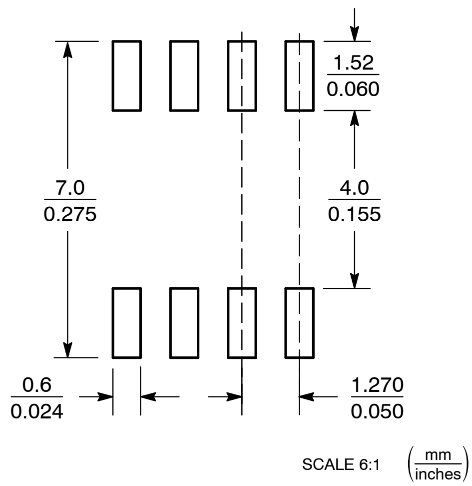
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative