NCV8401A, NCV8401B

Self-Protected Low Side Driver with Temperature and Current Limit

NCV8401A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
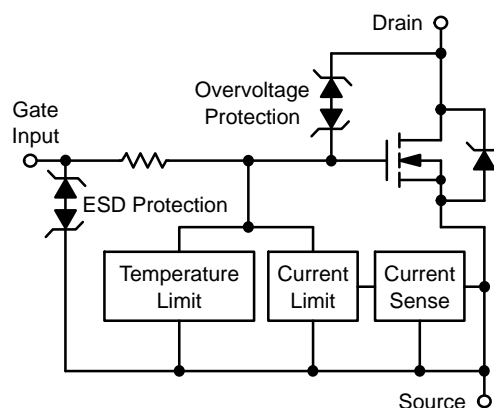- Automotive / Industrial

ON Semiconductor®

V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
42 V	23 mΩ @ 10 V	33 A*

*Max current may be limited below this value depending on input conditions.

DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM

1	YWW
2	NCV
3	xxxxxG
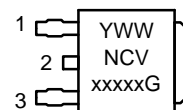
Y = Year
WW = Work Week
xxxxx = 8401A or 8401B
G = Pb−Free Package

1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping†
NCV8401ADTRKG	DPAK (Pb−Free)	2500/Tape & Reel
NCV8401BDTRKG	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
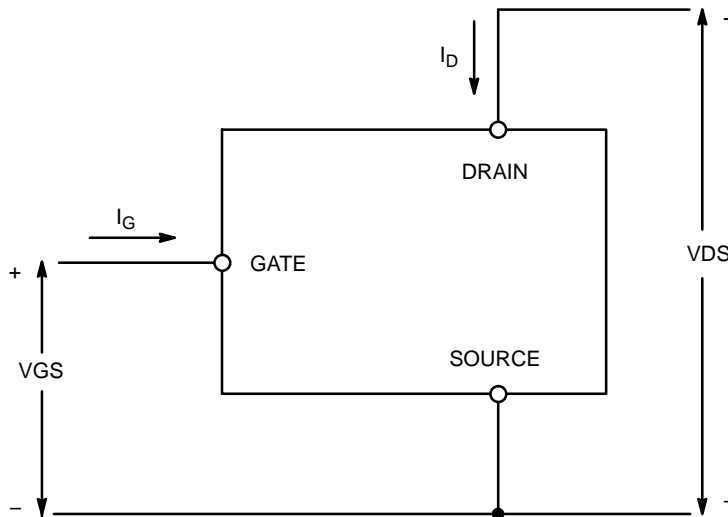
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped		V_{DSS}	42	V
Drain−to−Gate Voltage Internally Clamped	(R_{GS} = 1.0 MΩ)	V_{DGR}	42	V
Gate−to−Source Voltage		V_{GS}	±14	V
Drain Current − Continuous		I_D	Internally Limited	

Total Power Dissipation
    @ T_A = 25°C (Note 1)
    @ T_A = 25°C (Note 2)
		P_D	1.1
			2.0
				W

Thermal Resistance,   Junction−to−Case
          Junction−to−Ambient (Note 1)
          Junction−to−Ambient (Note 2)
		$R_{\theta JC}$
		$R_{\theta JA}$
		$R_{\theta JA}$
			1.6
			110
			60
				°C/W

Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 3.65 Apk, L = 120 mH, R_G = 25 Ω, T_{Jstart} = 150°C) (Note 3)		E_{AS}	800	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2.0 Ω, R_L = 3.0 Ω, t_d = 400 ms)		V_{LD}	65	V
Operating Junction Temperature		T_J	−40 to 150	°C
Storage Temperature		T_{stg}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2″ square FR4 board
    (1″ square, 2 oz. Cu 0.06″ thick single−sided, t = steady state).
3. Not subject to production testing.

Figure 1. Voltage and Current Convention

**MOSFET ELECTRICAL CHARACTERISTICS** (T_J = 25°C unless otherwise noted)

| Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = 150°C) (Note 4)		$V_{(BR)DSS}$	42 42	46 44	50 50	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 4)		I_{DSS}		1.5 6.5	5.0	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)		I_{GSSF}		50	100	μAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient		$V_{GS(th)}$	1.0	1.8 5.0	2.0	Vdc –mV/°C
Static Drain–to–Source On–Resistance (Note 5) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 150°C) (Note 4)		$R_{DS(on)}$		23 43	29 55	mΩ
Static Drain–to–Source On–Resistance (Note 5) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 150°C) (Note 4)		$R_{DS(on)}$		28 50	34 60	mΩ
Source–Drain Forward On Voltage (I_S = 5 A, V_{GS} = 0 V)		V_{SD}		0.80	1.1	V
SWITCHING CHARACTERISTICS (Note 4)						
Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 5 V, V_{DD} = 25 V I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		41	50	μs
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		129	150	
Turn–ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 10 V, V_{DD} = 25 V, I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		16	25	
Turn–OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		164	180	
Slew–Rate ON (80% V_{DS} to 50% V_{DS})	V_{in} = 0 to 10 V, V_{DD} = 12 V, R_L = 4.7 Ω	$-dV_{DS}/dt_{ON}$		1.27	2.0	V/μs
Slew–Rate OFF (50% V_{DS} to 80% V_{DS})		dV_{DS}/dt_{OFF}		0.36	0.75	
SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)						
Current Limit	V_{GS} = 5.0 V, V_{DS} = 10 V V_{GS} = 5.0 V, T_J = 150°C (Note 4)	I_{LIM}	25 11	30 16	35 21	Adc
	V_{GS} = 10 V, V_{DS} = 10 V V_{GS} = 10 V, T_J = 150°C (Note 4)		30 18	35 25	40 28	
Temperature Limit (Turn–off)	V_{GS} = 5.0 V (Note 4)	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V_{GS} = 5.0 V	$\Delta T_{LIM(on)}$		15		°C
Temperature Limit (Turn–off)	V_{GS} = 10 V (Note 4)	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V_{GS} = 10 V	$\Delta T_{LIM(on)}$		15		°C
GATE INPUT CHARACTERISTICS (Note 4)						
Device ON Gate Input Current	V_{GS} = 5 V I_D = 1.0 A	I_{GON}		50	100	μA
	V_{GS} = 10 V I_D = 1.0 A			400	700	
Current Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GCL}		0.1	0.5	mA
	V_{GS} = 10 V, V_{DS} = 10 V			0.7	1.0	
Thermal Limit Fault Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GTL}		0.6	1.0	mA
	V_{GS} = 10 V, V_{DS} = 10 V			2.0	4.0	
ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)						
Electro–Static Discharge Capability Human Body Model (HBM) Machine Model (MM)		ESD	4000 400			V

4. Not subject to production testing.
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
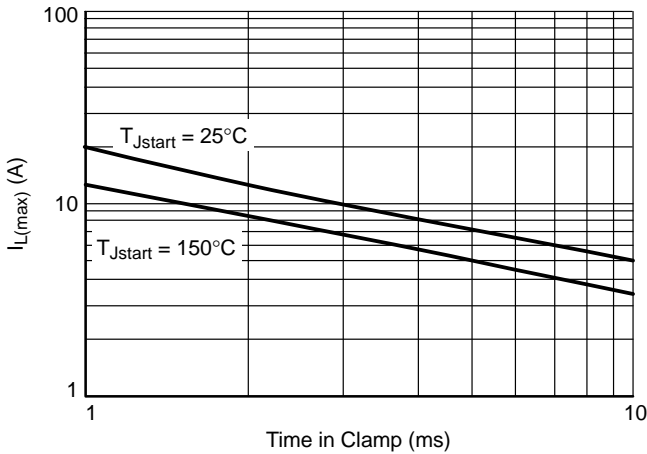
NCV8401A, NCV8401B
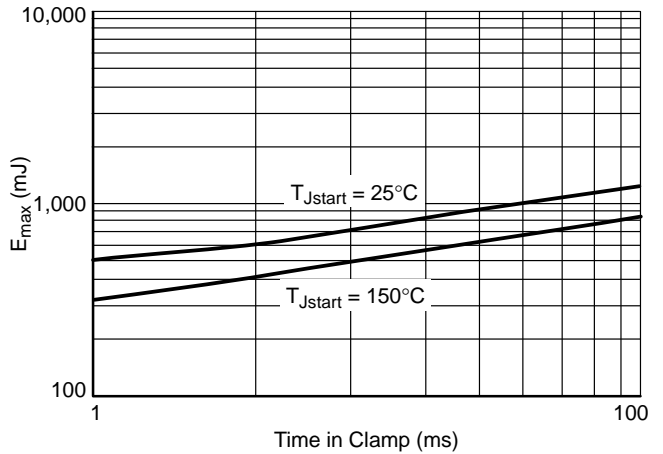
TYPICAL PERFORMANCE CURVES
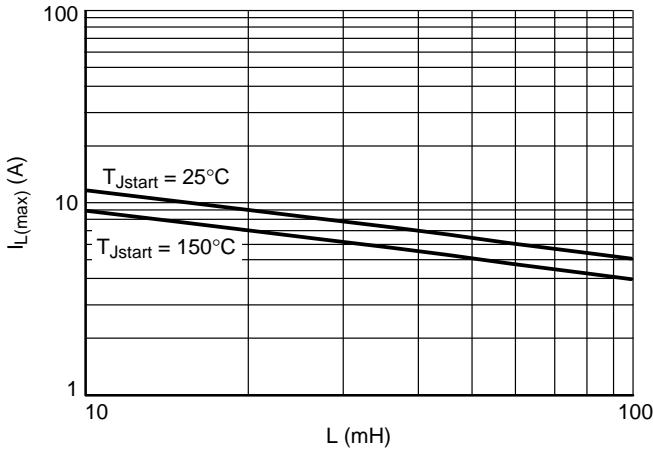
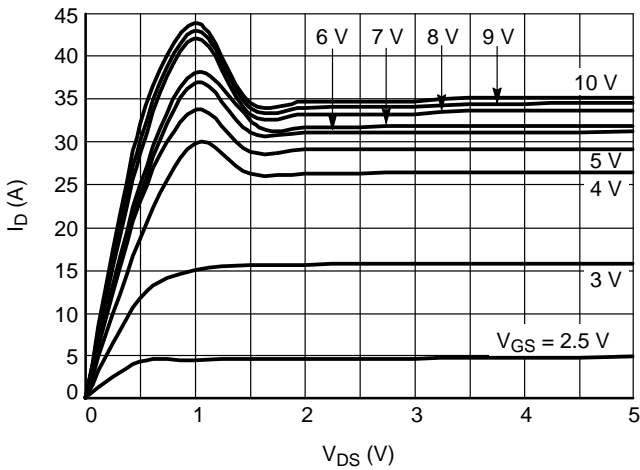Figure 2. Single Pulse Maximum Switch–off Current vs. Load Inductance
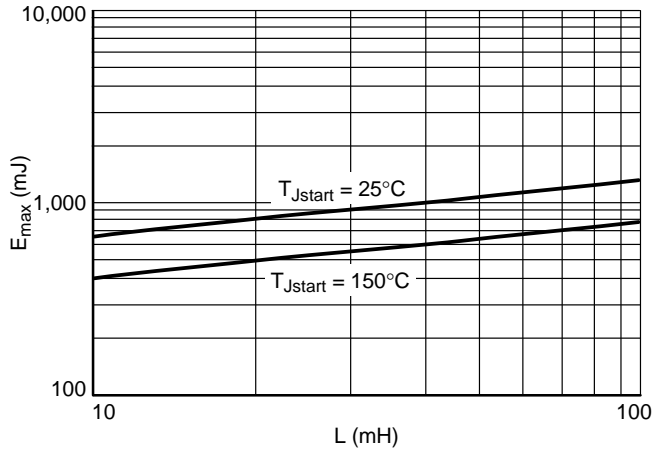
Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance
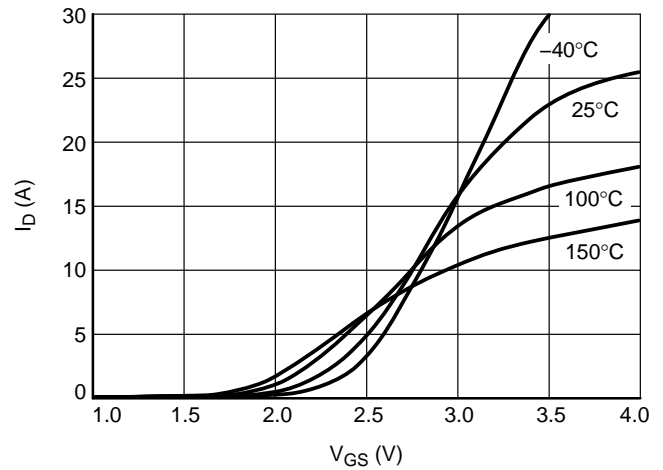

Figure 4. Single Pulse Maximum Inductive Switch–off Current vs. Time in Clamp

Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

Figure 6. On–state Output Characteristics at 25°C

Figure 7. Transfer Characteristics (V_{DS} = 10 V)

TYPICAL PERFORMANCE CURVES
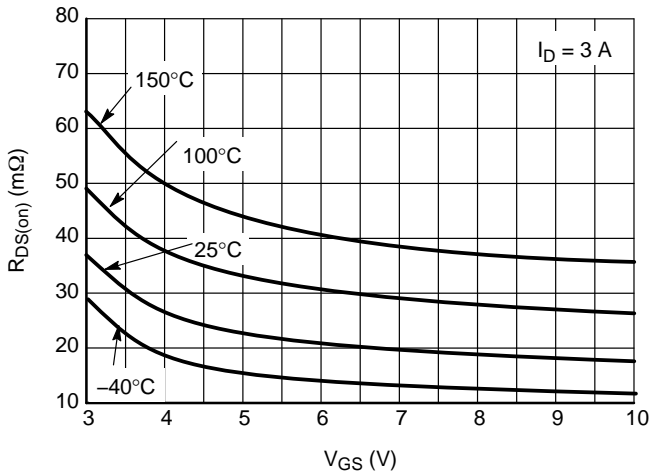
Figure 8. R_DS(on) vs. Gate−Source Voltage
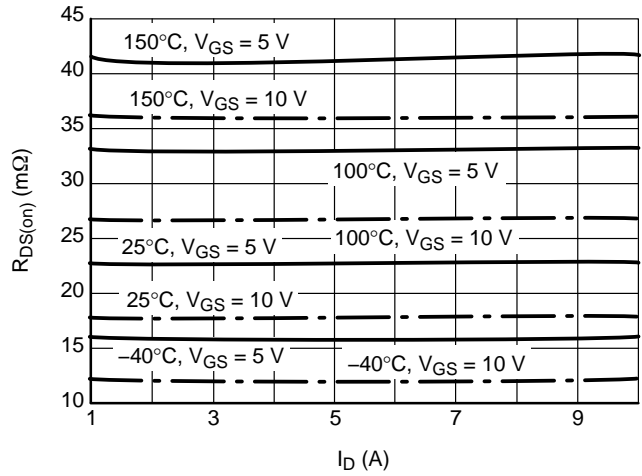
Figure 9. R_DS(on) vs. Drain Current
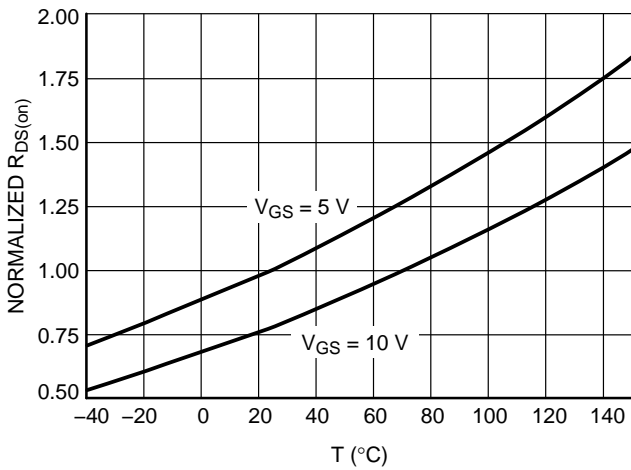
Figure 10. Normalized R_DS(on) vs. Temperature (I_D = 5 A)
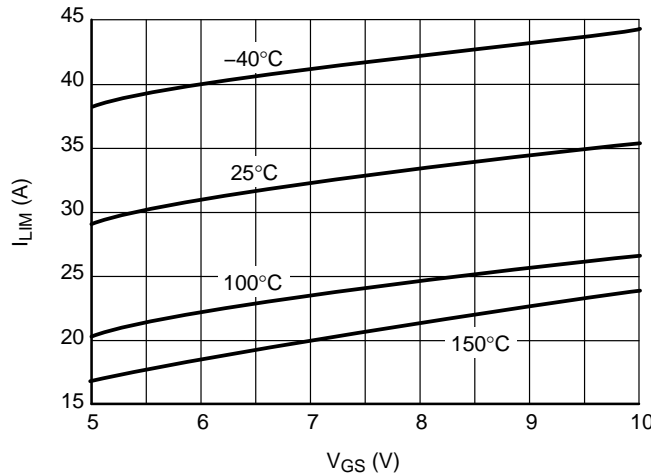
Figure 11. Current Limit vs. Gate−Source Voltage (V_DS = 10 V)
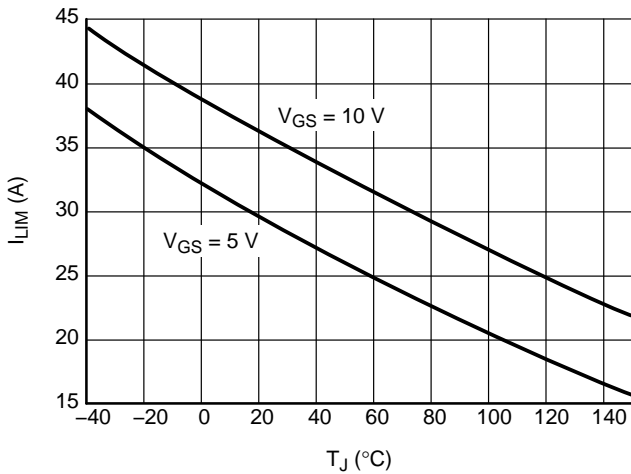
Figure 12. Current Limit vs. Junction Temperature (V_DS = 10 V)
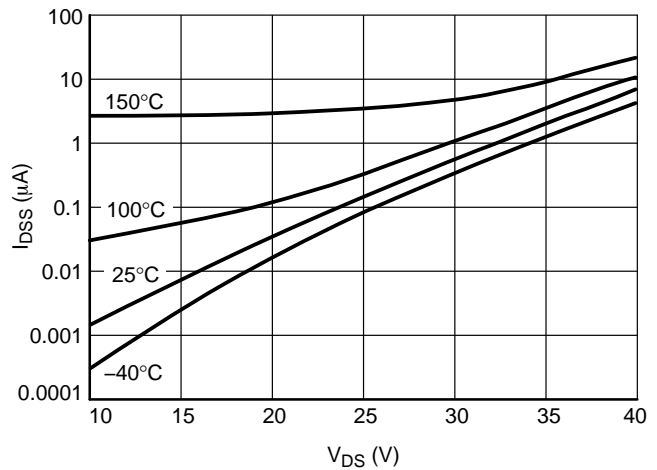
Figure 13. Drain−to−Source Leakage Current (V_GS = 0 V)
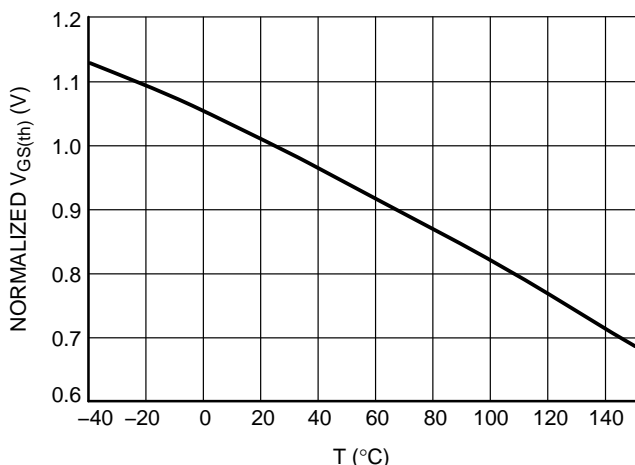
TYPICAL PERFORMANCE CURVES

Figure 14. Normalized Threshold Voltage vs. Temperature (I_D = 1.2 mA, V_{DS} = V_{GS})
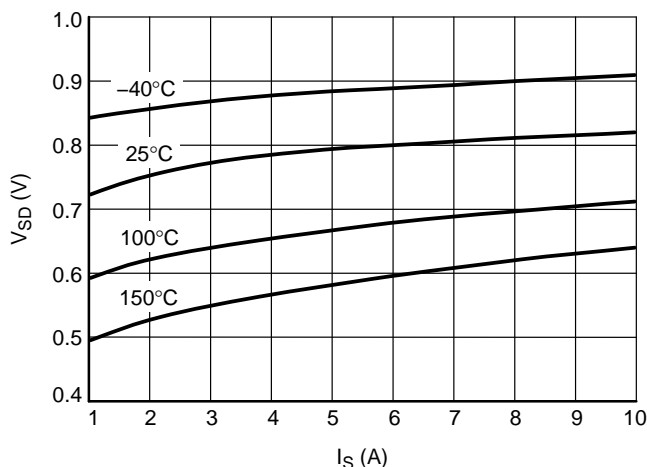
Figure 15. Source−Drain Diode Forward Characteristics (V_{GS} = 0 V)
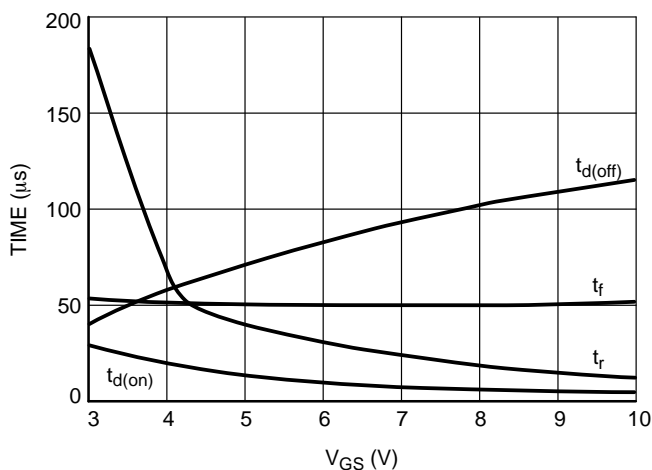
Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage (V_{DD} = 25 V, I_D = 5 A, R_G = 0 Ω)
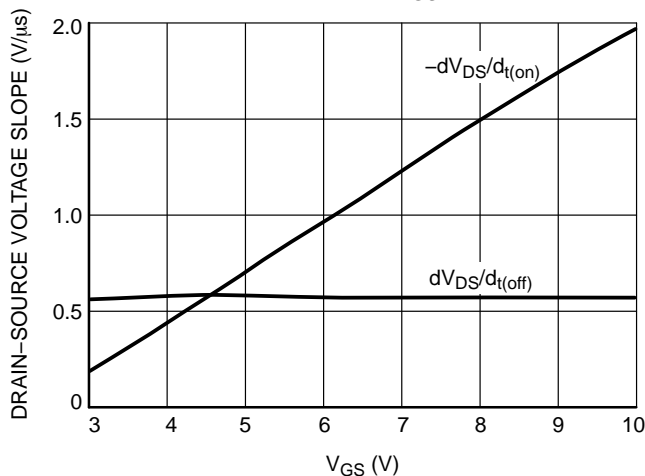
Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage (V_{DD} = 25 V, I_D = 5 A, R_G = 0 Ω)
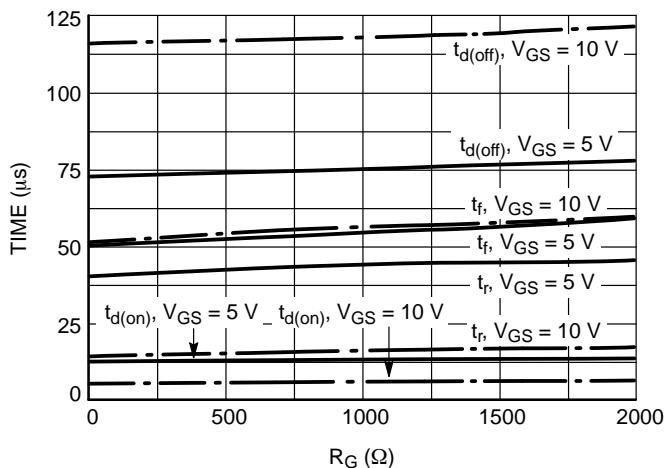

Figure 18. Resistive Load Switching Time vs. Gate Resistance (V_{DD} = 25 V, I_D = 5 A)
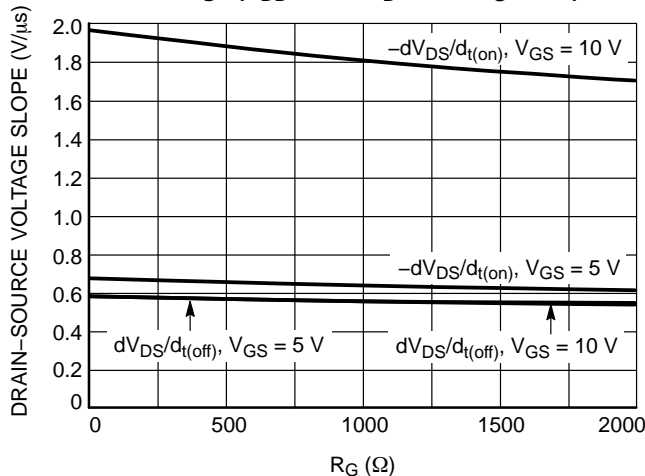
Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance (V_{DD} = 25 V, I_D = 5 A)
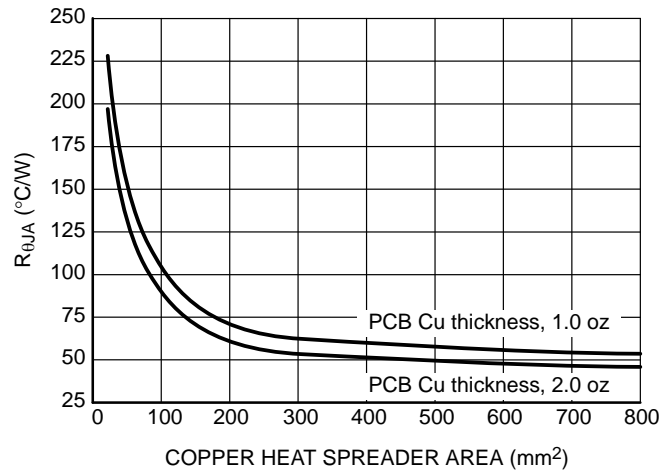
NCV8401A, NCV8401B

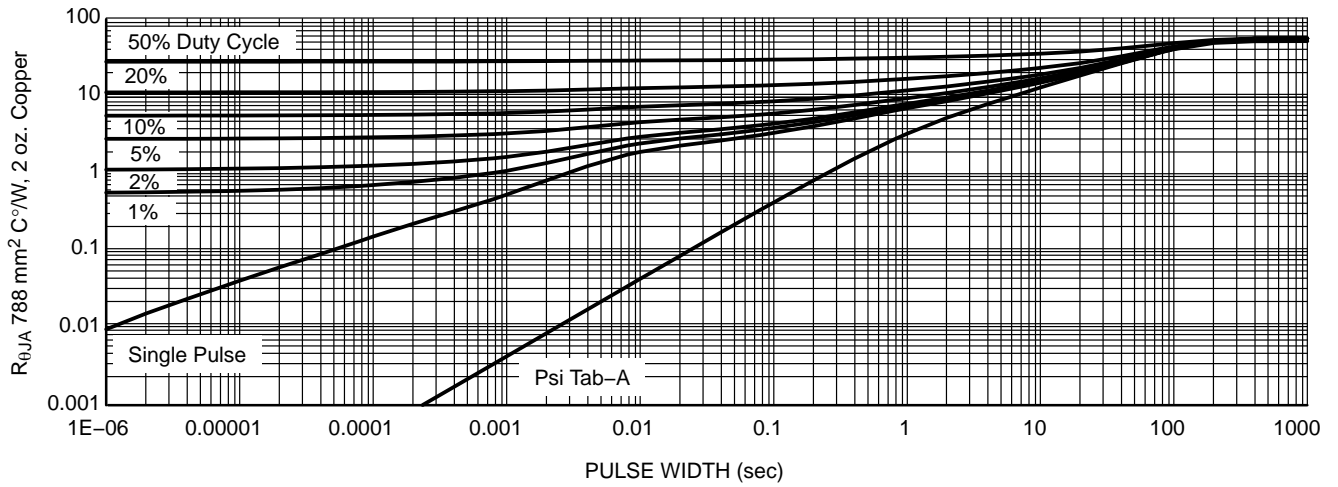**TYPICAL PERFORMANCE CURVES**

Figure 20. R$_{\theta JA}$ vs. Copper Area

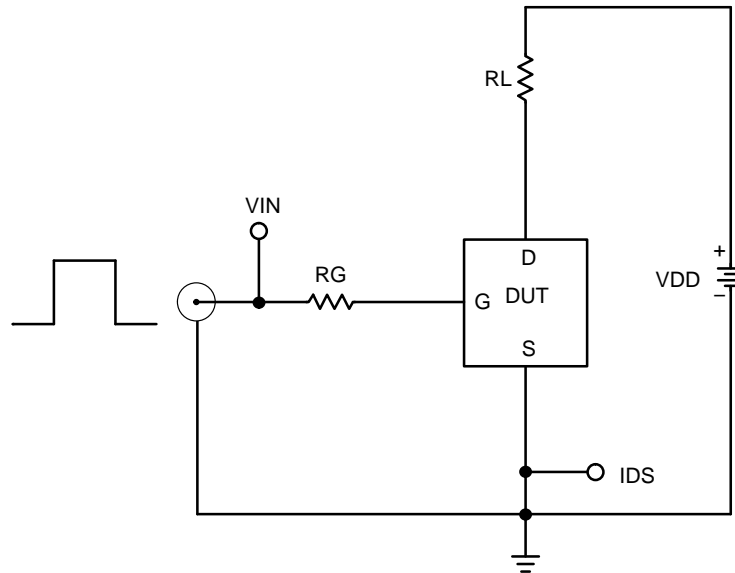**Figure 21. Transient Thermal Resistance**

TEST CIRCUITS AND WAVEFORMS

Figure 22. Resistive Load Switching Test Circuit

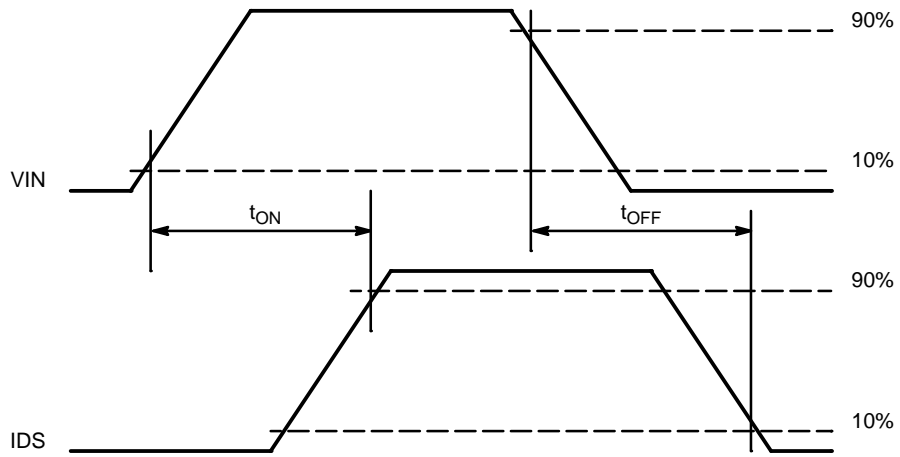**Figure 23. Resistive Load Switching Waveforms**

TEST CIRCUITS AND WAVEFORMS

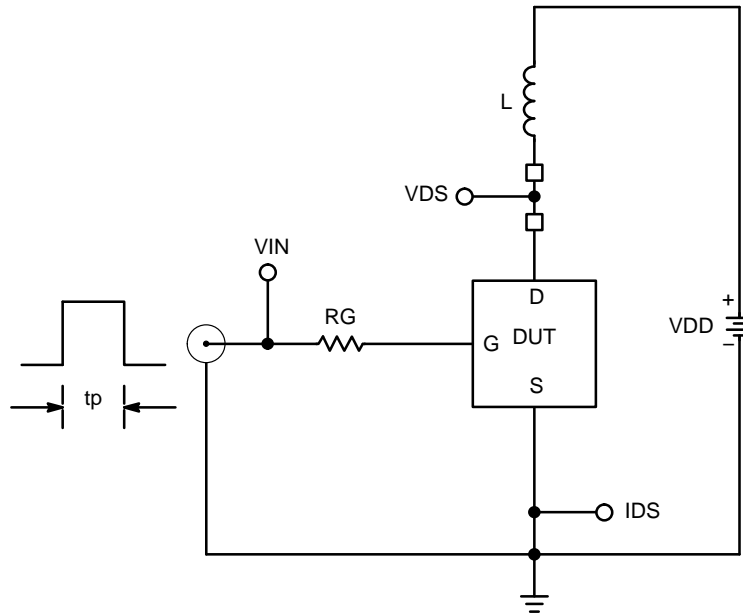**Figure 24. Inductive Load Switching Test Circuit**

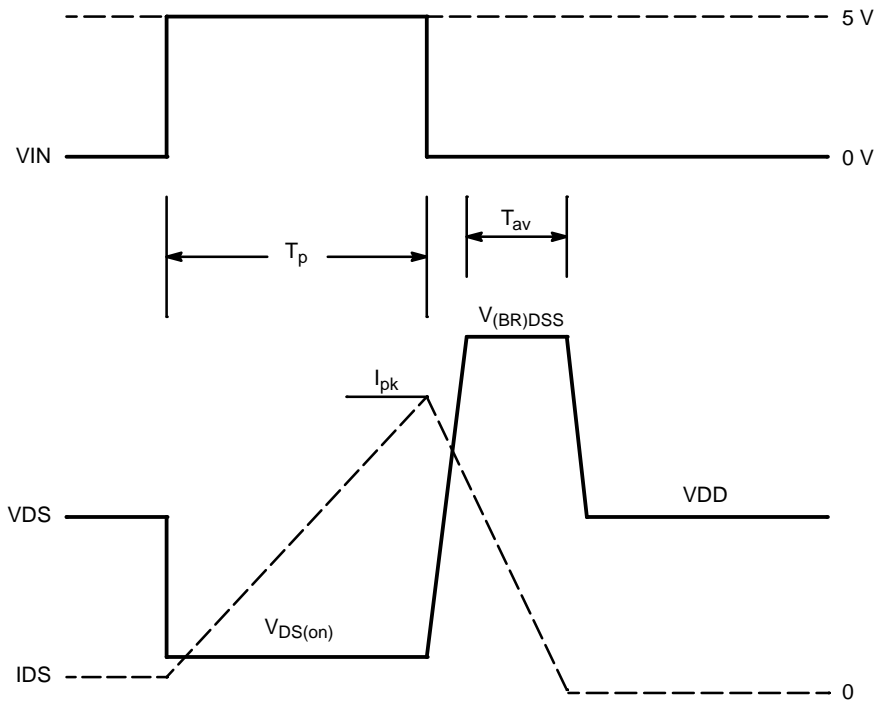**Figure 25. Inductive Load Switching Waveforms**

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DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

SCALE 1:1

TOP VIEW

⊕ | 0.005 (0.13) Ⓜ | C

DETAIL A

SIDE VIEW

BOTTOM VIEW

BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

DETAIL A
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

XXXXXXG
ALYWW

IC

AYWW
XXX
XXXXXG

Discrete

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*

6.20 / 0.244
3.00 / 0.118
2.58 / 0.102
5.80 / 0.228
1.60 / 0.063
6.17 / 0.243

SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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