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LDO Regulator, Ultra Low I_q, with Enable and Reset, 350 mA

NCV8772C

The NCV8772C is 350 mA LDO regulator with integrated reset function dedicated for microprocessor applications. Its robustness allows NCV8772C to be used in severe automotive environments. Ultra low quiescent current as low as 18 μA typical makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. This feature is especially critical when modules remain in active mode when ignition is off. The Enable function can be used for further decrease of quiescent current in shutdown mode to 1 μA. The NCV8772C contains protection functions as current limit, thermal shutdown and reverse output current protection.

Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±2%
- Output Current up to 350 mA
- Ultra Low Quiescent Current: typ 18 μA (max 24 μA)
- Very Wide Range of C_{out} and ESR Values for Stability
- Enable Function
  - 1 μA Max Quiescent Current when disabled
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features
  - Current Limitation
  - Thermal Shutdown
  - Reverse Output Current Protection
- EMC Compliant
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

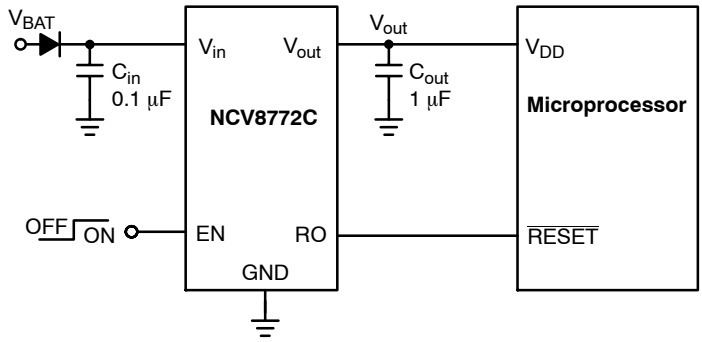

Figure 1. Typical Application Schematic

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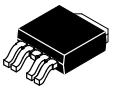
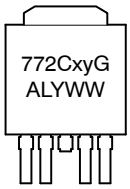
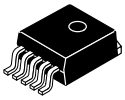
MARKING DIAGRAMS

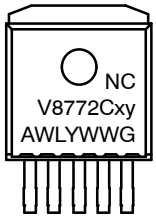


DPAK−5
DT SUFFIX
CASE 175AA





D²PAK−5
DS SUFFIX
CASE 936A



x	= Voltage Option
y	= Timing and Reset Threshold Option
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

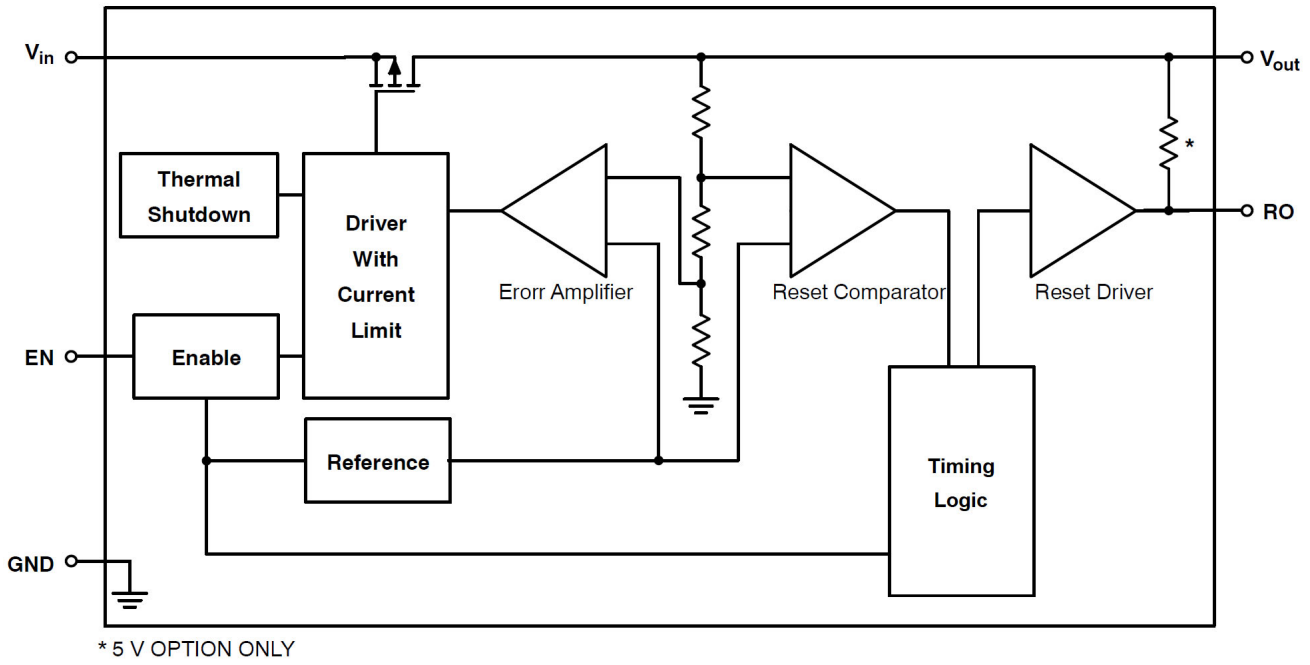


Figure 2. Simplified Block Diagram

PIN CONNECTIONS

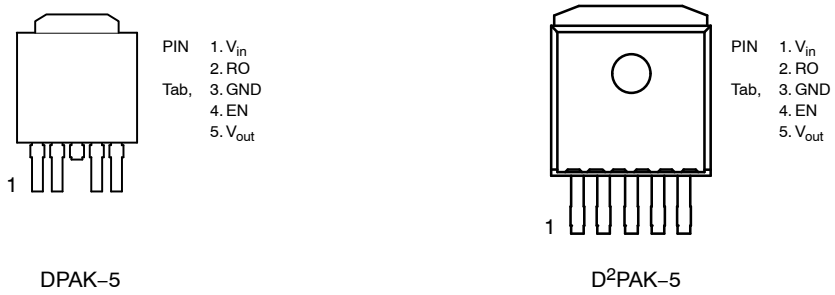


Figure 3. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No. DPAK−5 D2PAK−5	Pin Name	Description
1	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
2	RO	Reset Output. 30 kΩ internal Pull−up resistor (5 V option only) connected to V_{out}. RO goes Low when V_{out} drops by more than 7% from its nominal value (for NCV8772Cy devices with y = 0,1,2,...).
3, TAB	GND	Power Supply Ground.
4	EN	Enable Input. Low level disables the IC.
5	V_{out}	Regulated Output Voltage. Connect 1 μF capacitor with ESR < 5 Ω to ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC Input Voltage (Note 1) Load Dump − Suppressed	V_{in} V_{s*}	−0.3 −	40 45	V
Output Voltage (Note 2)	V_{out}	−0.3	7	V
Enable Input Voltage	V_{EN}	−0.3	40	V
Reset Output Voltage	V_{RO}	−0.3	7.0	V
Junction Temperature Range	T_J	−40	150	°C
Storage Temperature Range	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750 − 2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750 − 1.
2. 5.5 V or (V_{in} + 0.3 V) (whichever is lower).

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−4	4	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level DPAK−5 D2PAK−5	MSL	1 1		−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS (Note 5)

Rating	Symbol	Value	Unit
Thermal Characteristics, DPAK−5 Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Case (Note 6)	 $R_{\theta JA}$ $R_{\Psi JC}$	 47.1 12.6	°C/W
Thermal Characteristics, D2PAK−5 Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Case (Note 6)	 $R_{\theta JA}$ $R_{\Psi JC}$	 42.3 12.6	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.
   Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGE (Note 7)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 8)	V_{in}	4.5	40	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
8. Minimum V_{in} = 4.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3 V, C_{in} = 0.1 μF, C_{out} = 1 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statical correlation. Typical values are referenced to T_J = 25°C. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %)		V_{out}	(−2 %)		(+2%)	V
3.3 V	V_{in} = 4.5 V to 40 V, I_{out} = 0.1 mA to 200 mA		3.234	3.3	3.366	
	V_{in} = 4.5 V to 16 V, I_{out} = 0.1 mA to 350 mA		3.234	3.3	3.366	
5.0 V	V_{in} = 5.6 V to 40 V, I_{out} = 0.1 mA to 200 mA		4.9	5.0	5.1	
	V_{in} = 5.975 V to 16 V, I_{out} = 0.1 mA to 350 mA		4.9	5.0	5.1	
Line Regulation		Reg_{line}				mV
3.3 V	V_{in} = 4.5 V to 28 V, I_{out} = 5 mA		−20	0	20	
5.0 V	V_{in} = 6 V to 28 V, I_{out} = 5 mA		−20	0	20	
Load Regulation	I_{out} = 0.1 mA to 350 mA	Reg_{load}	−35	10	35	mV
Dropout Voltage (Note 11)		V_{DO}				mV
5.0 V	I_{out} = 200 mA		–	250	450	
	I_{out} = 350 mA		–	440	800	
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V, T_J < 125°C	I_{DIS}	–	–	1	μA
Quiescent Current (I_q = I_{in} − I_{out})		I_q				μA
	I_{out} = 0 mA, T_J = 25°C		–	18	22	
	I_{out} = 0 mA, T_J ≤ 125°C		–	–	24	
	I_{out} = 0.1 mA, T_J = 25°C		–	20	24	
	I_{out} = 0.1 mA, T_J ≤ 125°C		–	–	26	
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	400	–	1100	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	400	–	1100	mA
REVERSE OUTPUT CURRENT PROTECTION						
Reverse Output Current Protection	V_{EN} = 0 V, I_{out} = −1 mA	V_{out_rev}	–	2	5.5	V
PSRR						
Power Supply Ripple Rejection (Note 12)	f = 100 Hz, 0.5 V_{pp}	PSRR	–	75	–	dB
ENABLE THRESHOLDS						
Enable Input Threshold Voltage		$V_{th(EN)}$				V
Logic Low			0.8	1.65	–	
Logic High			–	1.75	2.5	
Enable Input Current						μA
Logic High	V_{EN} = 5 V	I_{EN_ON}	–	3	5	
Logic Low	V_{EN} = 0 V	I_{EN_OFF}	–	0.5	1	
RESET OUTPUT RO						
Input Voltage Reset Threshold	V_{in} decreasing, V_{out} > V_{RT}	V_{in_RT}				V
3.3 V			–	3.8	4.2	
Output Voltage Reset Threshold (Note 13)	V_{out} decreasing	V_{RT}	90	93	96	%V_{out}
Reset Hysteresis		V_{RH}	–	2.0	–	%V_{out}
Maximum Reset Sink Current 3.3 V	V_{out} = 3 V, V_{RO} = 0.25 V	I_{ROmax}	1.3	–	–	mA
5.0 V	V_{out} = 4.5 V, V_{RO} = 0.25 V		1.75	–	–	
Reset Output Low Voltage	V_{out} > 1 V, I_{RO} < 200 μA	V_{ROL}	–	0.15	0.25	V
Reset Output High Voltage 5.0 V		V_{ROH}	4.5	–	–	V

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3 V, C_{in} = 0.1 μF, C_{out} = 1 μF. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statical correlation. Typical values are referenced to T_J = 25°C. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT RO						
Reset High Level Leakage Current 3.3 V		I_{ROLK}	–	–	1.0	μA
Integrated Reset Pull−up Resistor 5.0 V		R_{RO}	15	30	50	kΩ
Reset Delay Time (Note 13)	Min Available Time Max Available Time	t_{RD}	– 102.4	0 128	– 153.6	ms
Reset Reaction Time (see Figure 31)		t_{RR}	16	25	38	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 12)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 12)		T_{SH}	–	10	–	°C

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

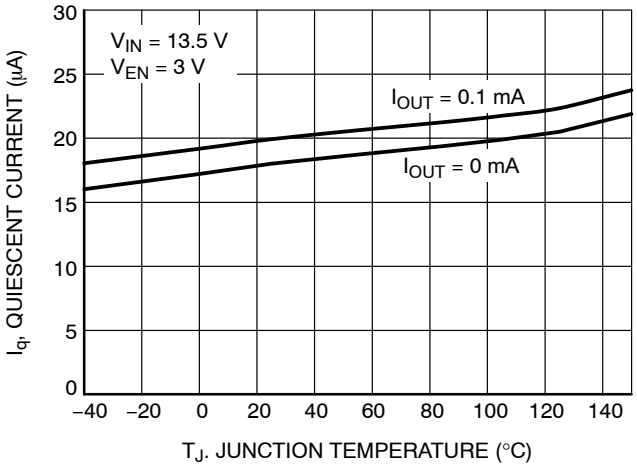


Figure 4. Quiescent Current vs. Temperature

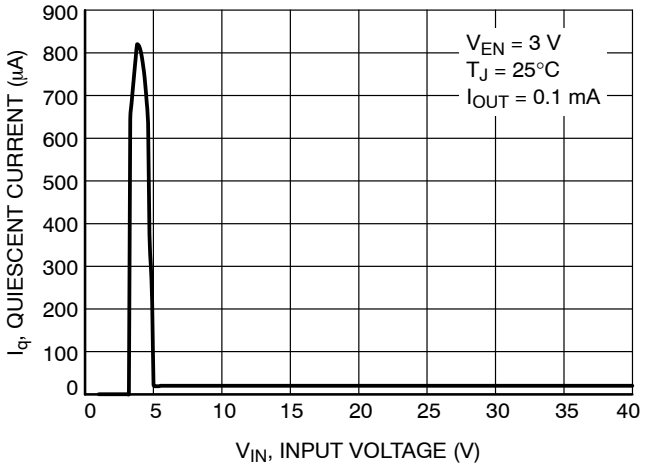


Figure 5. Quiescent Current vs. Input Voltage

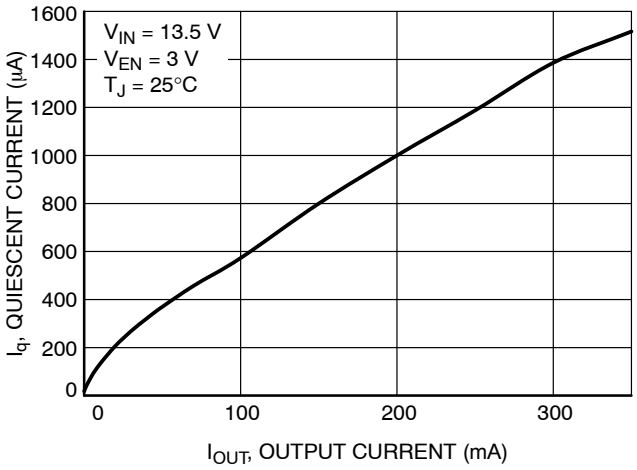


Figure 6. Quiescent Current vs. Output Current

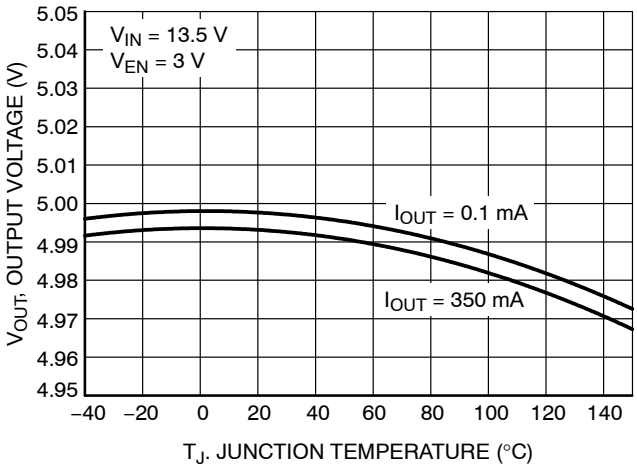


Figure 7. Output Voltage vs. Temperature (5 V Option)

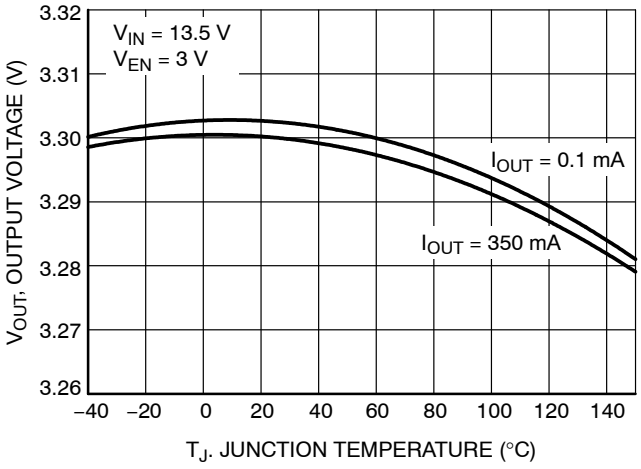


Figure 8. Output Voltage vs. Temperature (3.3 V Option)

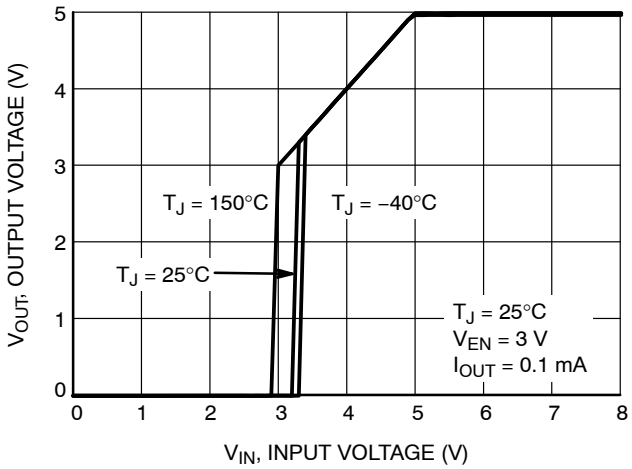


Figure 9. Output Voltage vs. Input Voltage (5 V Option)

TYPICAL CHARACTERISTICS

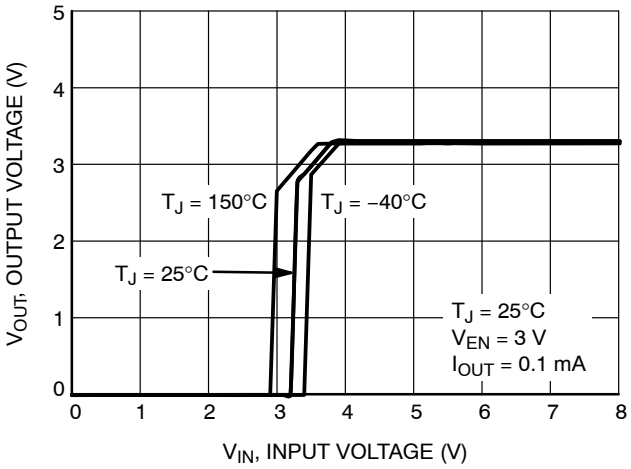


Figure 10. Output Voltage vs. Input Voltage (3.3 V Option)

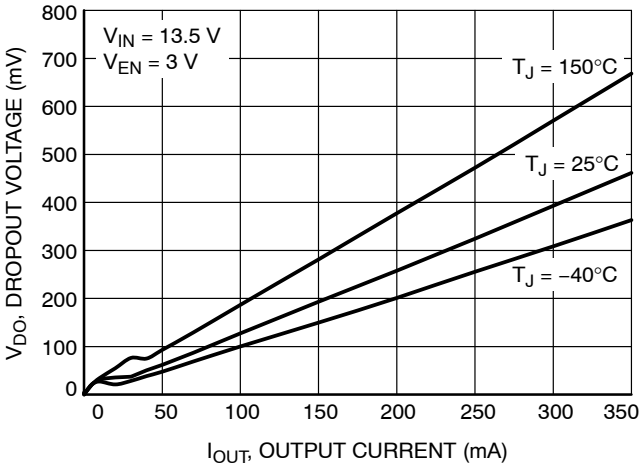


Figure 11. Dropout vs. Output Current (5 V Option)

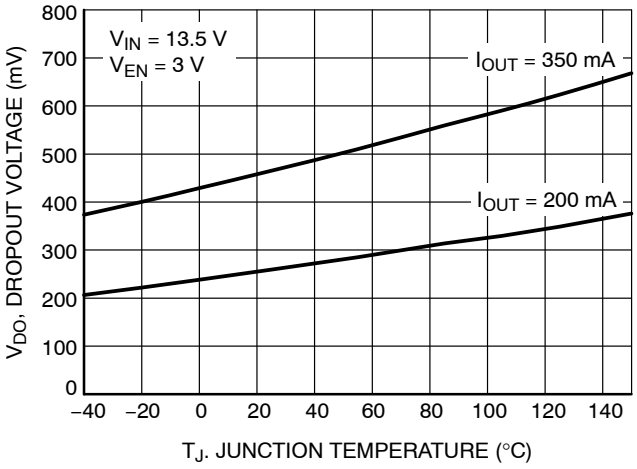


Figure 12. Dropout vs. Temperature (5 V Option)

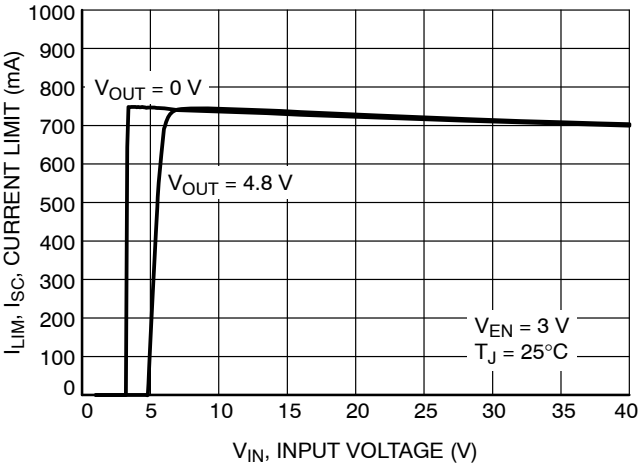


Figure 13. Output Current Limit vs. Input Voltage (5 V Option)

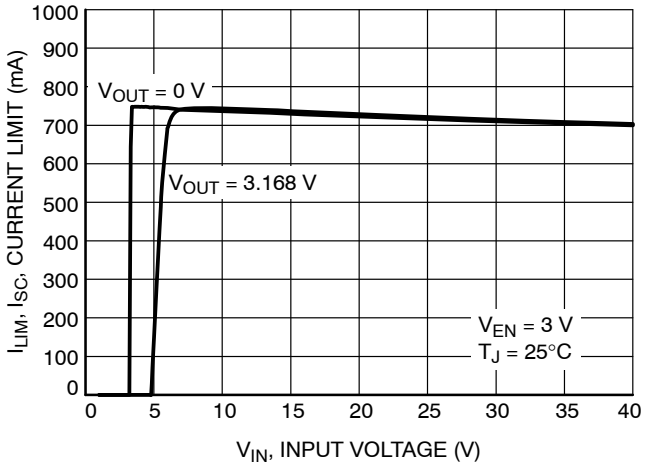


Figure 14. Output Current Limit vs. Input Voltage (3.3 V Option)

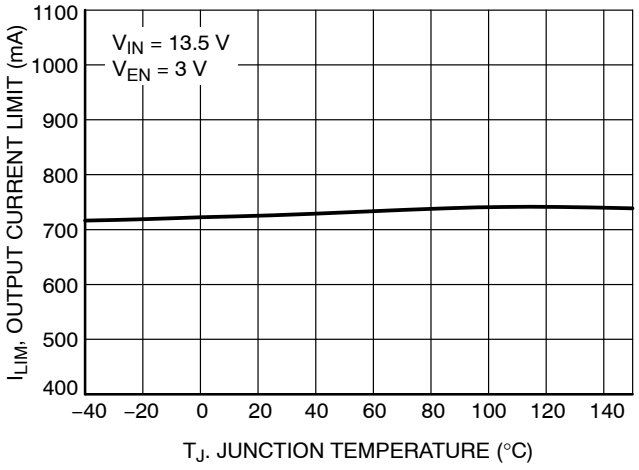


Figure 15. Output Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

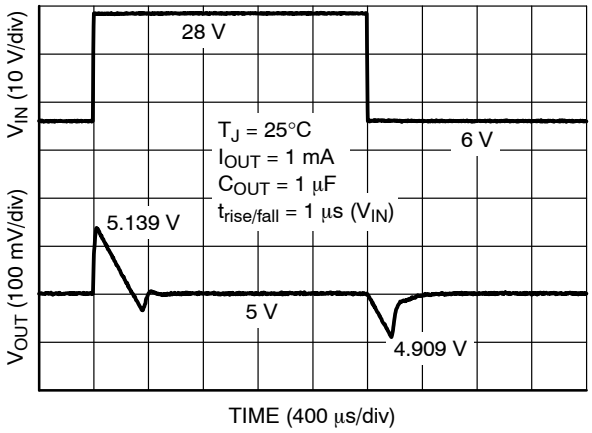


Figure 16. Line Transients (5 V Option)

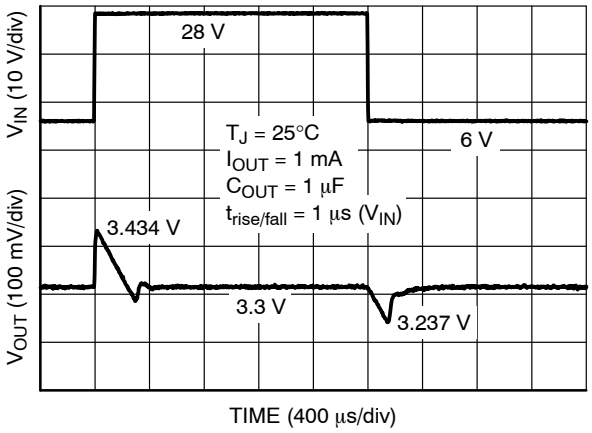


Figure 17. Line Transients (3.3 V Option)

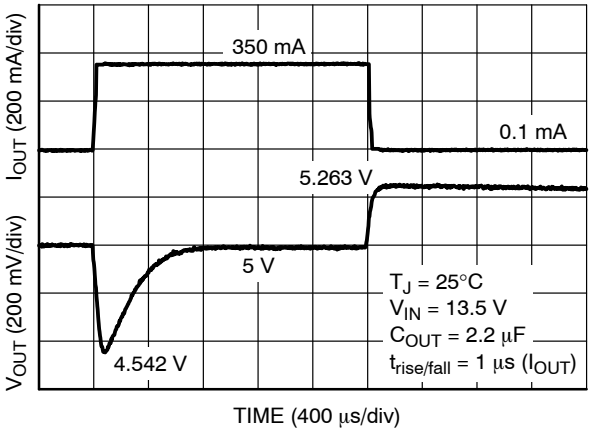


Figure 18. Load Transients (5 V Option)

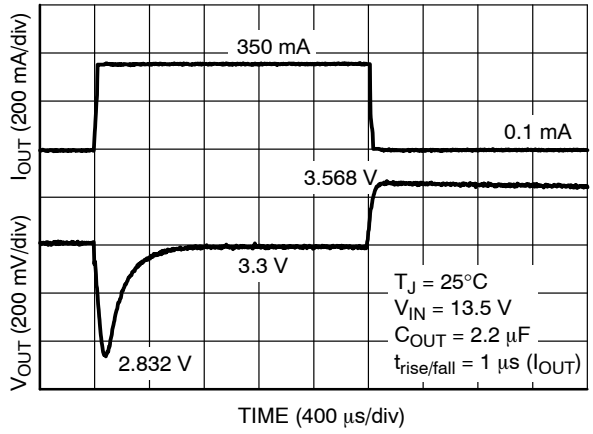


Figure 19. Load Transients (3.3 V Option)

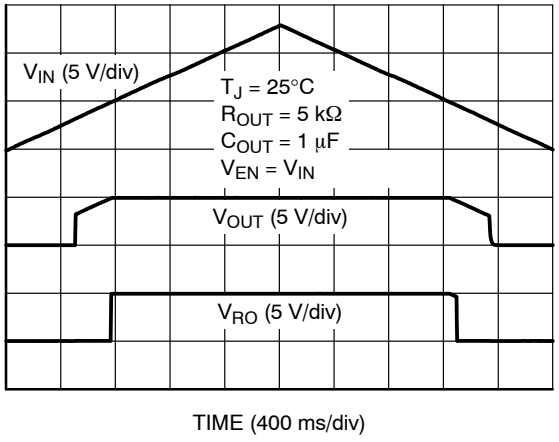


Figure 20. Power Up/Down Response (5 V Option)

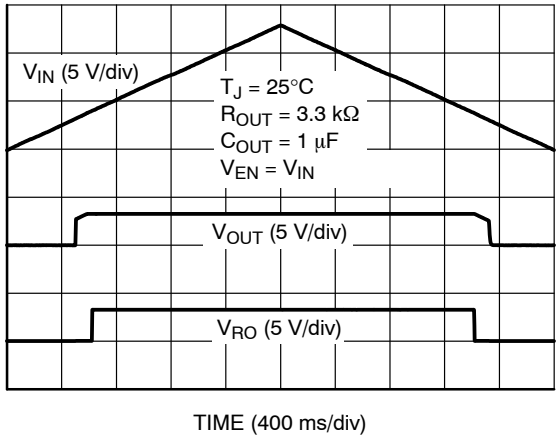


Figure 21. Power Up/Down Response (3.3 V Option)

TYPICAL CHARACTERISTICS

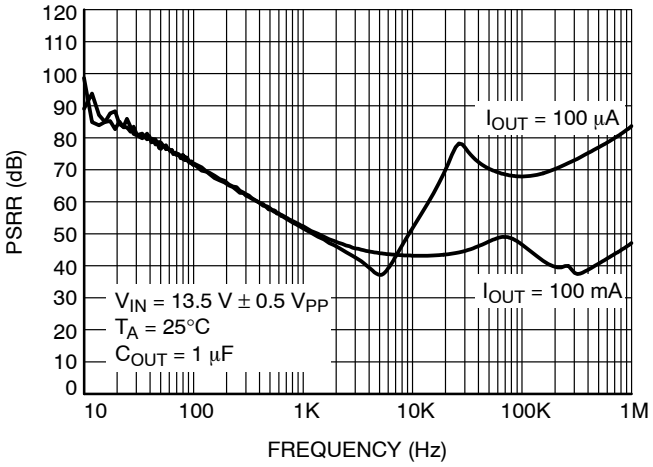


Figure 22. PSRR vs. Frequency (5 V Option)

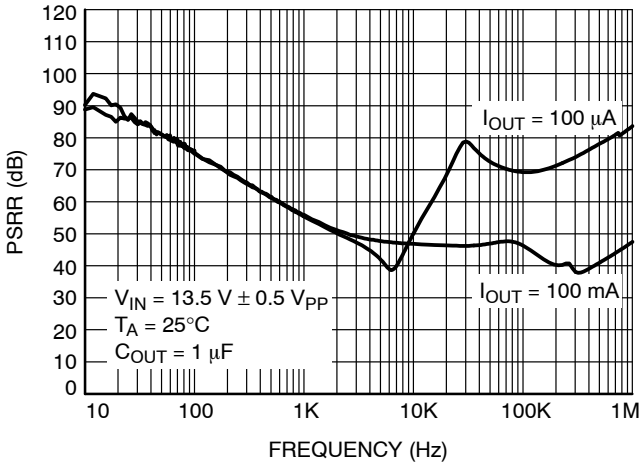


Figure 23. PSRR vs. Frequency (3.3 V Option)

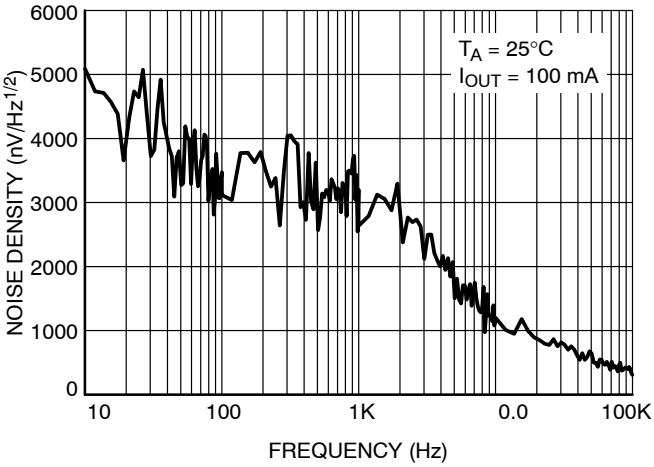


Figure 24. Noise vs. Frequency

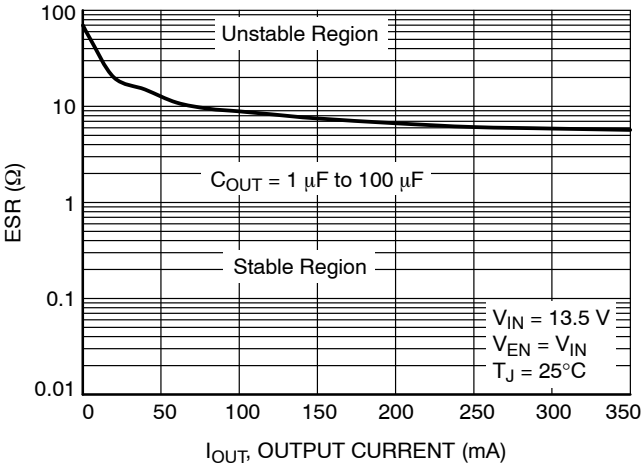


Figure 25. C_{out} ESR Stability Region vs. Output Current

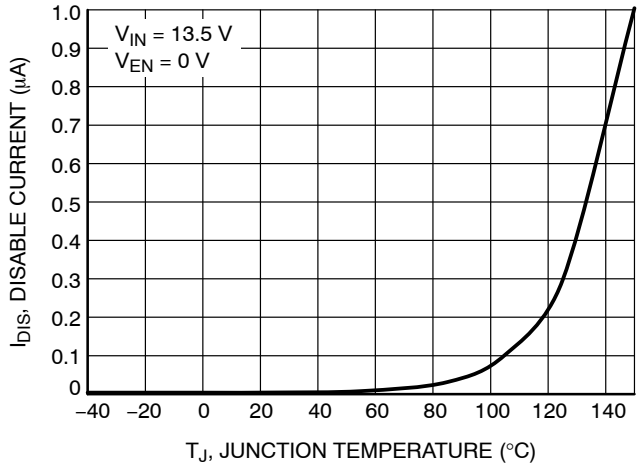


Figure 26. Disable Current vs. Temperature

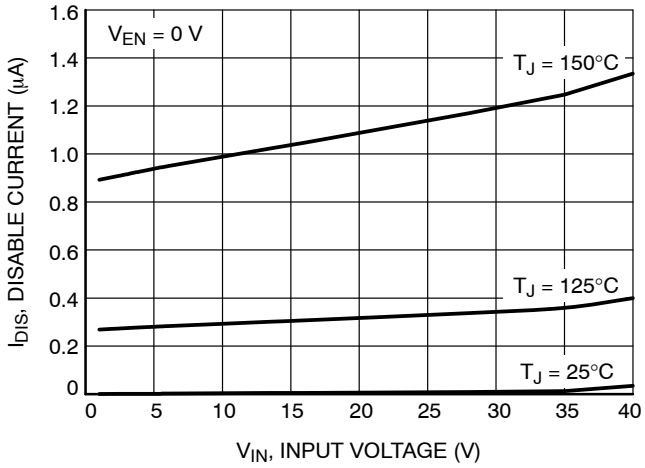


Figure 27. Disable Current vs. Input Voltage

TYPICAL CHARACTERISTICS

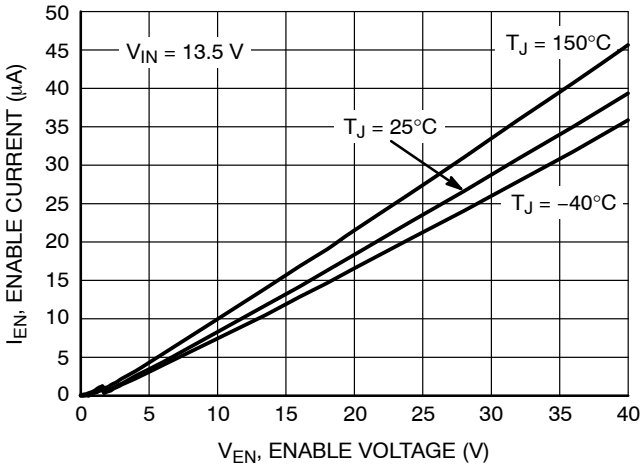


Figure 28. Enable Current vs. Enable Voltage

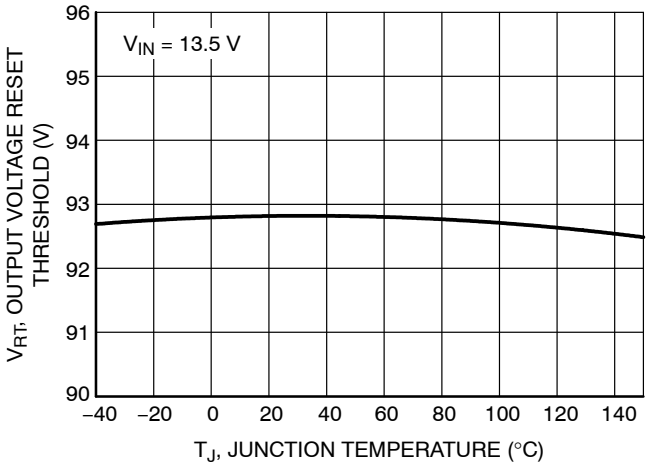


Figure 29. Output Voltage Reset Threshold vs. Temperature

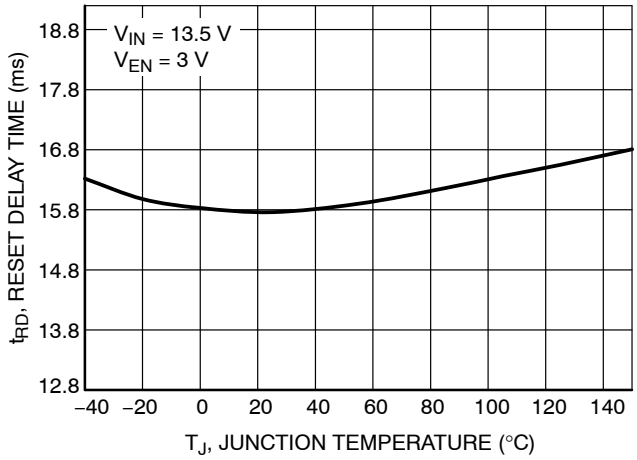


Figure 30. Reset Delay Time vs. Temperature

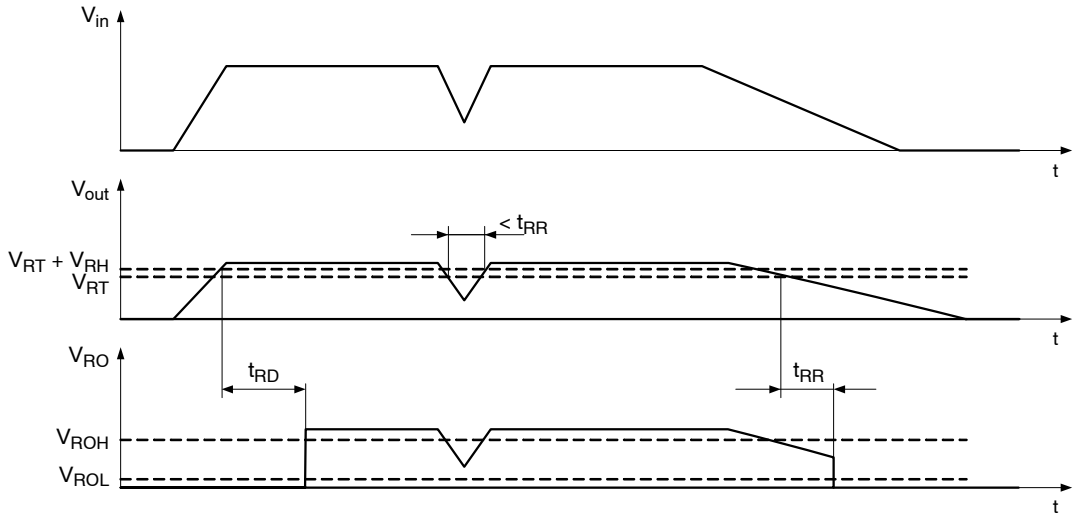


Figure 31. Reset Function and Timing Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8772C regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 4 to Figure 30.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8772C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8772C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs Output Current is shown in Figure 25. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this datasheet.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 31. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{out} = 1.0 V. For 5 V voltage option, the Reset Output (RO) circuitry includes internal pull−up (30 kΩ) connected to the output (V_{out}) No external pull−up is necessary. For voltage options and 3.3 V RO is open drain output and external pull−up resistor is required. Select pull−up resistor in range between 5 kΩ to 100 kΩ with respect to I_{ROmax} and I_{ROLK} limits to keep V_{RO} logic levels at appropriate range.

Reset signal is also generated in case when input voltage decreases below its minimum operating limit (4.5 V). The Input Voltage Reset Threshold is typically 3.8 V.

RESET DELAY AND RESET THRESHOLD OPTIONS (DPAK−5 AND D2PAK−5)

	Reset Delay Time	Reset Threshold
NCV8772CDTxx0 NCV8772CDSxx0	0 ms	93%
NCV8772CDTxx1 NCV8772CDSxx1	2 ms	93%
NCV8772CDTxx2 NCV8772CDSxx2	4 ms	93%
NCV8772CDTxx3 NCV8772CDSxx3	8 ms	93%
NCV8772CDTxx4 NCV8772CDSxx4	16 ms	93%
NCV8772CDTxx5 NCV8772CDSxx5	32 ms	93%
NCV8772CDTxx6 NCV8772CDSxx6	64 ms	93%
NCV8772CDTxx7 NCV8772CDSxx7	128 ms	93%

NOTE: The timing values can be selected from the following list: 0, 2, 4, 8, 16, 32, 64, 128 ms. Contact factory for options not included in ORDERING INFORMATION table on page 13.

Thermal Considerations

As power in the NCV8772C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8772C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8772C can handle is given by:

$$P_{D(max)} = \frac{\left[T_{J(max)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8772C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2.95 W (for D2PAK−5) when the ambient temperature (T_A) is 25°C. See Figure 32 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8772C can be calculated from the following equations:

$$P_D = V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(max)} = \frac{P_{D(max)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

NOTE: Items containing I_q can be neglected if $I_{out} >> I_q$.

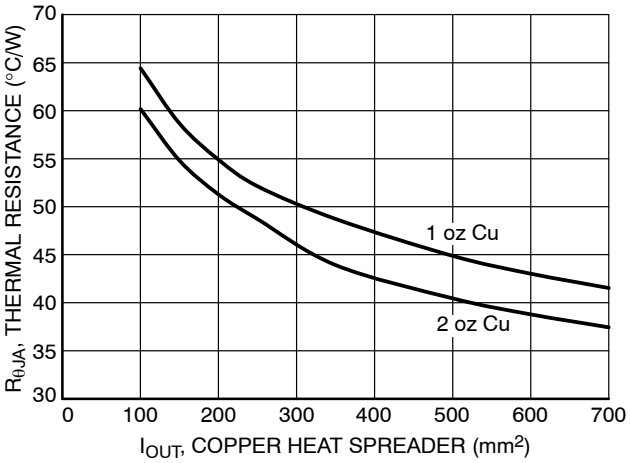


Figure 32. Thermal Resistance vs. PCB Copper Area (D2PAK−5)

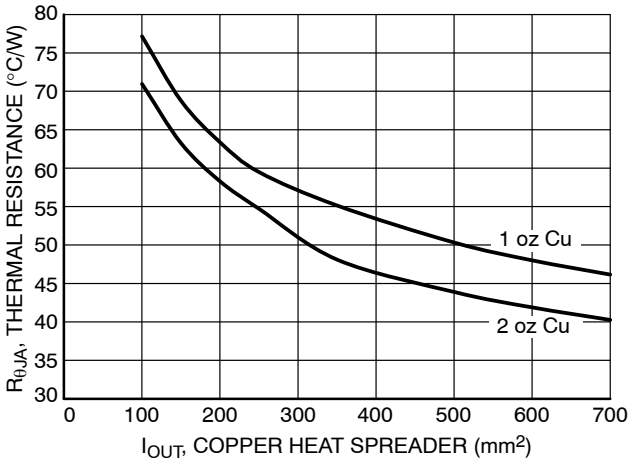


Figure 33. Thermal Resistance vs. PCB Copper Area (DPAK−5)

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8772C and make traces as short as possible.

The NCV8772C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application diagram shown in Figure 34 can be used.

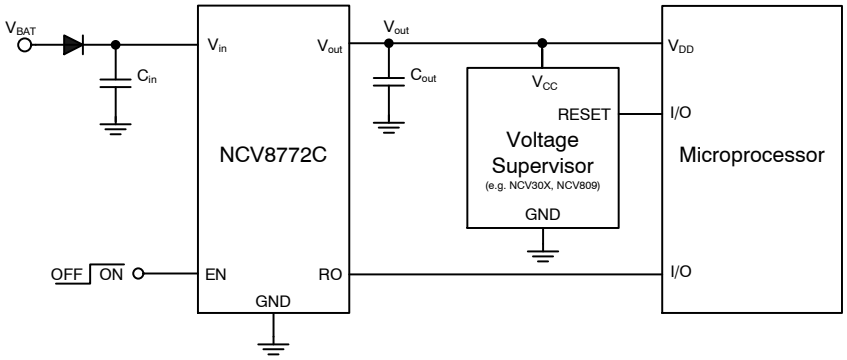


Figure 34. Application Diagram

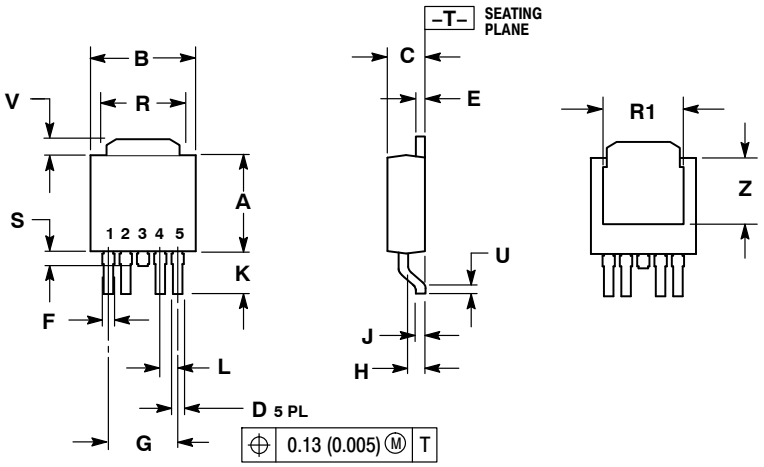
ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time	Reset Threshold	Marking	Package	Shipping†
NCV8772CDS334R4G	3.3 V	16 ms	93%	NC V8772C34	D²PAK−5 (Pb−Free)	800 / Tape & Reel
NCV8772CDT334RKG	3.3 V	16 ms	93%	772C34G	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCV8772CDT504RKG	5.0 V	16 ms	93%	772C54G	DPAK−5 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

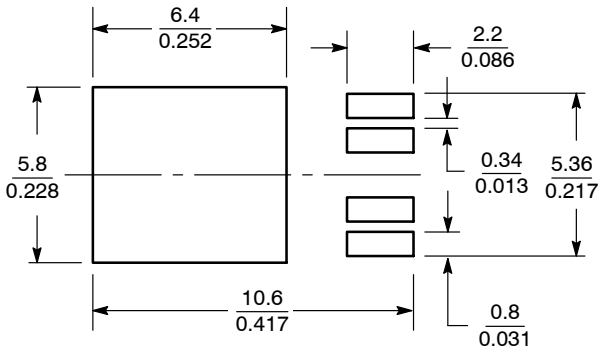
DPAK 5, CENTER LEAD CROP
CASE 175AA
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

SOLDERING FOOTPRINT*

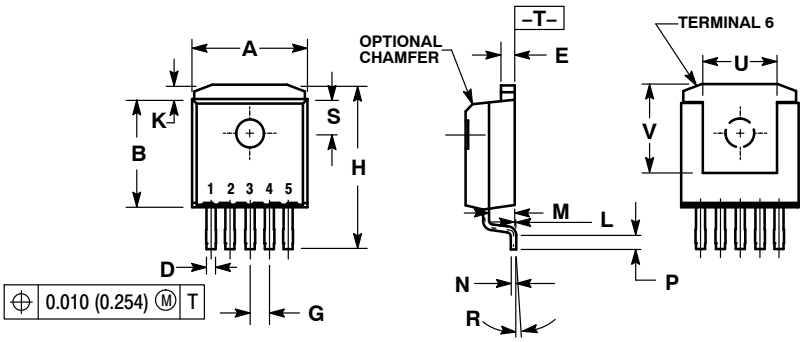


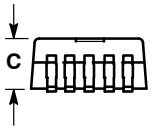
SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

D²PAK 5
CASE 936A−02
ISSUE D

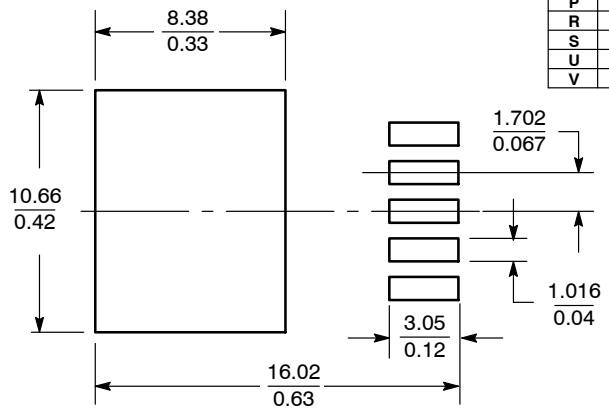




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
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