

NCV885300EVB

NCV885300 Evaluation Board User's Manual



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EVAL BOARD USER'S MANUAL

Description

The NCV885300 evaluation board provides a convenient way to evaluate and integrate a complete high-efficiency non-synchronous buck converter design. No additional components are required, other than dc supplies for the input voltage and enable pin. The board can also be connected to an external clock source to synchronize the switching frequency. The power good signal can be pulled up externally with the PG+ pin. The board is configured for a 5.0 V output with a 340 kHz switching frequency and a 3 A current limit, intended for applications requiring 2 A of current.

Modifying the NCV885300 evaluation board for different output voltage, switching frequency, or current limit is straightforward, requiring minimal component changes.

Key Features

- 5.0 V Output Voltage
- 340 kHz Switching Frequency
- 2.0 A Current Limit
- Power Good Signal
- Wide Input Voltage of 6.0 V to 36 V
- Regulated through Load Dump Conditions
- External Clock Synchronization up to 500 kHz
- Automotive Grade



Figure 1. NCV885300EVB Board Picture

NCV885300EVB

Table 1. EVALUATION BOARD TERMINALS

| Pin Name | Function |
|----------|---|
| VIN | Positive dc input voltage |
| VOUT | Regulated dc output voltage |
| GND | Common dc return |
| EN/SYNC | Enable input and external clock synchronization input |
| PG | Digital power good output |
| PG+ | Power good pull-up. Use this pin only when pulling-up PG to an external voltage source. |

Table 2. ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

| Rating | Value | Units |
|--------------------------------------|-------------|-------|
| Dc supply voltage (VIN) | -0.3 to 36 | V |
| Dc supply voltage (EN/SYNC, PG, PG+) | -0.3 to 6.0 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $6.0\text{ V} \leq V_{IN} \leq 36\text{ V}$, $V_{EN/SYNC} = 5.0\text{ V}$, $0 \leq I_{OUT} \leq 2.0\text{ A}$, unless otherwise specified)

| Characteristics | Conditions | Typical Value | Units |
|-----------------------------------|--------------------------|---------------|------------------|
| Regulation | | | |
| Output Voltage | | 5.0 | V |
| Voltage Accuracy | | 2 | % |
| Line Regulation | $I_{OUT} = 1.0\text{ A}$ | 0.04 | % |
| Load Regulation | $V_{IN} = 13.2\text{ V}$ | 0.12 | % |
| Switching | | | |
| Switching Frequency | | 340 | kHz |
| Soft-start Time | | 2.0 | ms |
| SYNC Frequency Range | | 270 to 500 | kHz |
| Current Limit | | | |
| Cycle-by-Cycle Current Limit | | 3.33 | A |
| Over Current Protection Threshold | | 5.0 | A |
| Protections | | | |
| Input Undervoltage Lockout (UVLO) | V_{IN} decreasing | 3.1 | V |
| Thermal Shutdown | T_J rising | 170 | $^\circ\text{C}$ |

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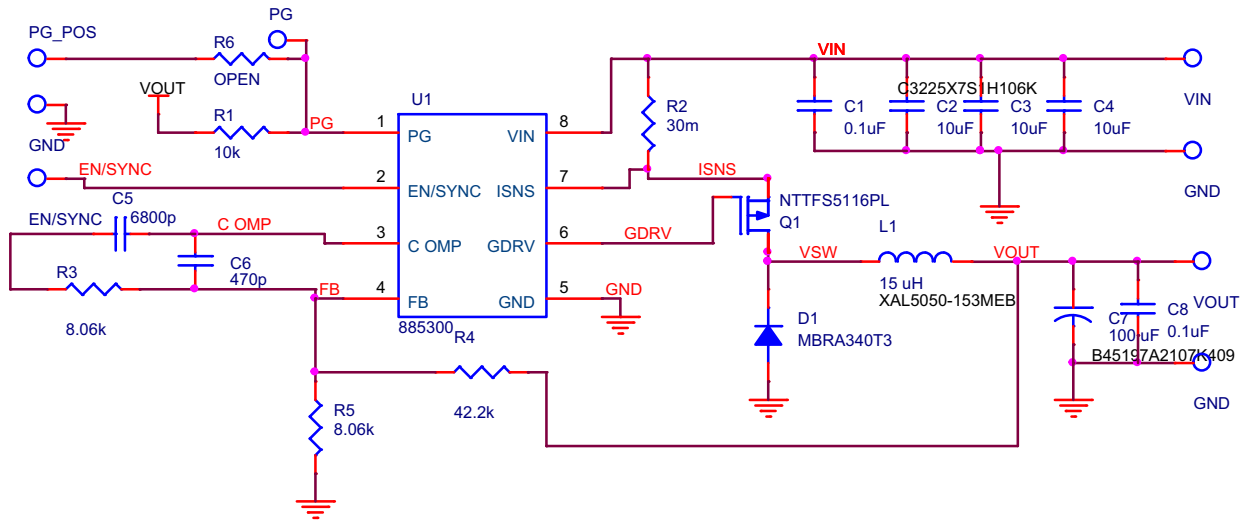


Figure 2. NCV885300EVB Board Schematic

Operational Guidelines

1. Connect a dc input voltage, within the 6.0 V to 36 V range, between VIN and GND
2. Connect a load between VOUT and GND
3. Connect a dc enable voltage, within the 2.0 V to 5.5 V range, between EN/SYNC and GND
4. Optionally, for external clock synchronization, connect a pulse source between EN/SYNC and GND. The high state level should be within the 2.0 V to 5.5 V range, and the low state level within the 0.0 V to 0.8 V range, with a frequency within the 270 kHz to 500 kHz range.

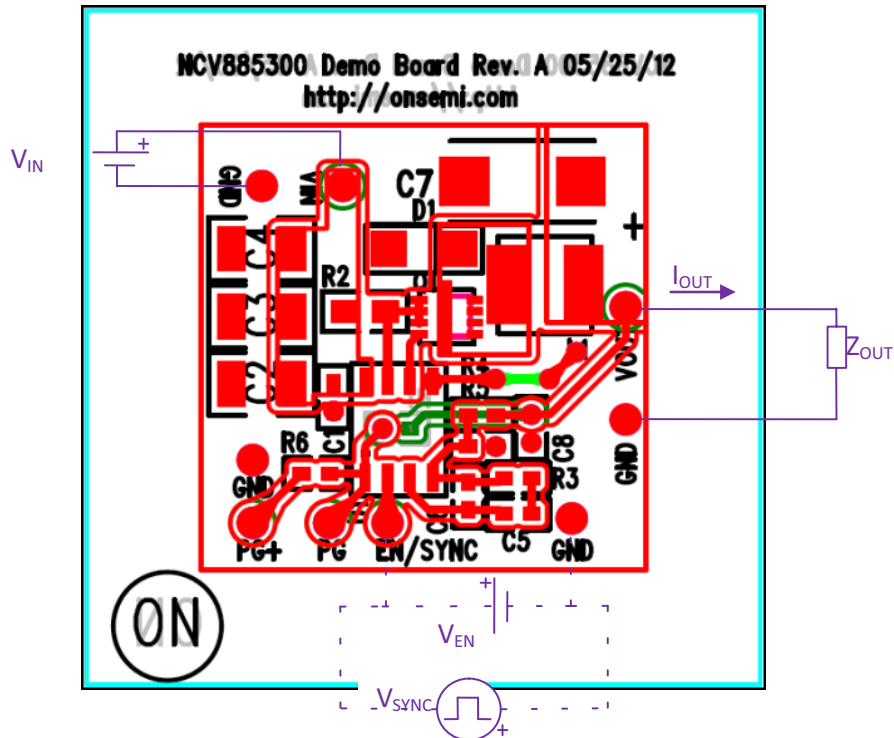


Figure 3. NCV885300EVB Board Connections

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Power Good Operation

- The Power Good pin (PG) allows you to digitally monitor the output voltage. When VOUT is above 90% of the expected value, the PG signal is in a high state. By default, PG is pulled high to VOUT through a 10 kΩ resistor.
- Optional: To pull the PG pin high using a signal other than VOUT, please make the following board modifications:
 1. Remove R1 from the board.
 2. Populate R6 with a 10 kΩ resistor.
 3. Connect the a voltage source between PG+ and GND (please see the Absolute Maximum Ratings table for more information).
 4. PG is now ready to digitally monitor VOUT using an external pull-up.

TYPICAL PERFORMANCE

Regulation

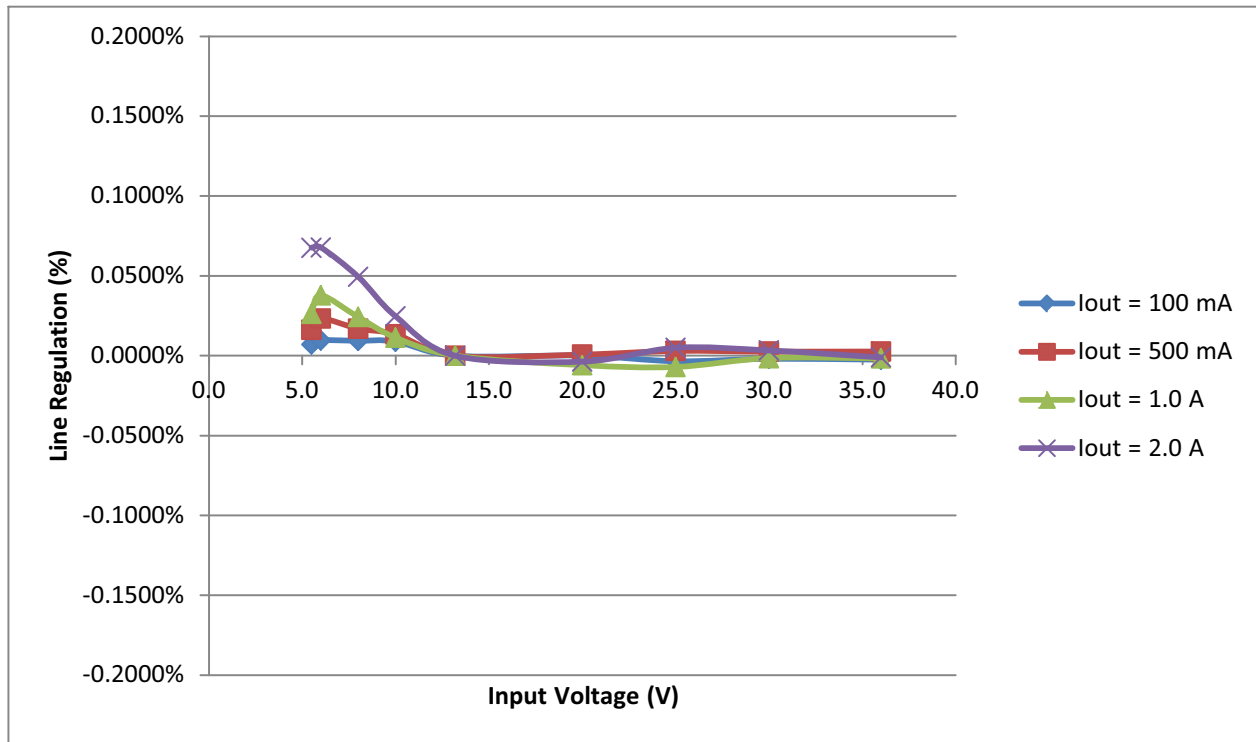


Figure 4. Line Regulation for 340 kHz and a 5.0 V Output

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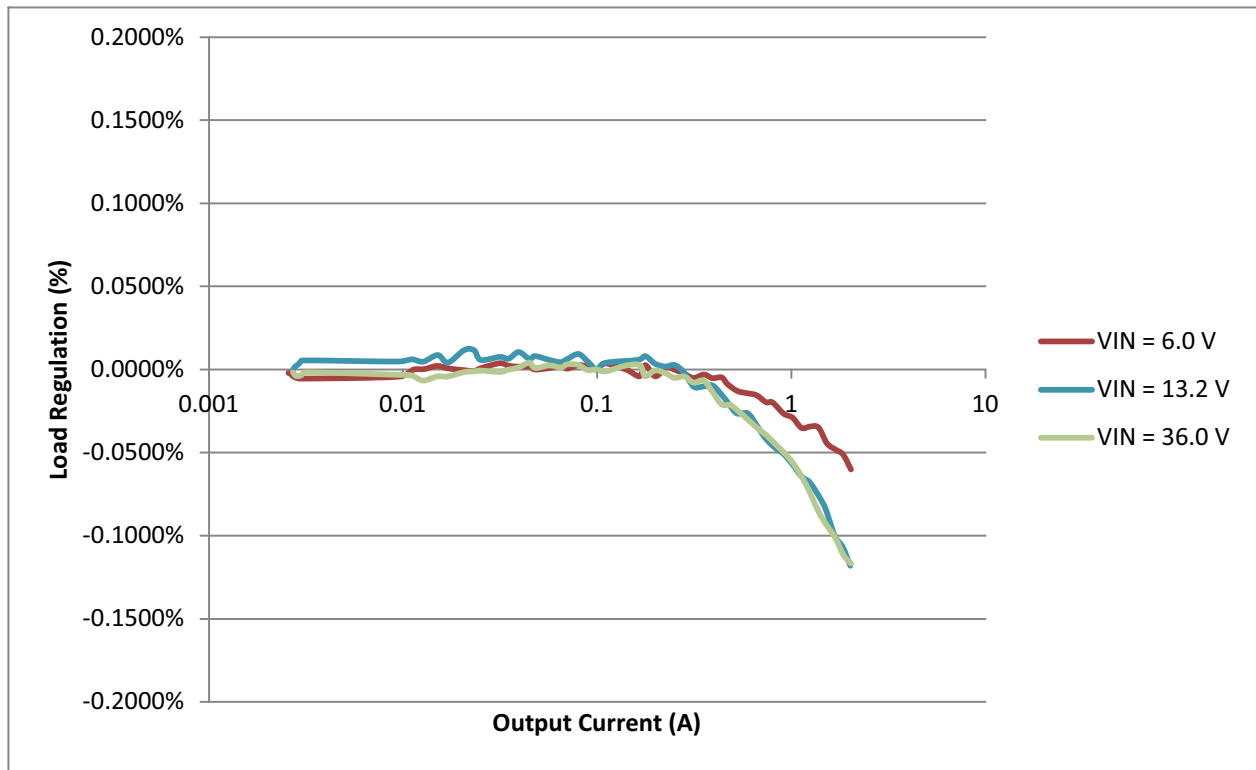


Figure 5. Load Regulation for 340 kHz and a 5.0 V Output

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SCHEMATIC

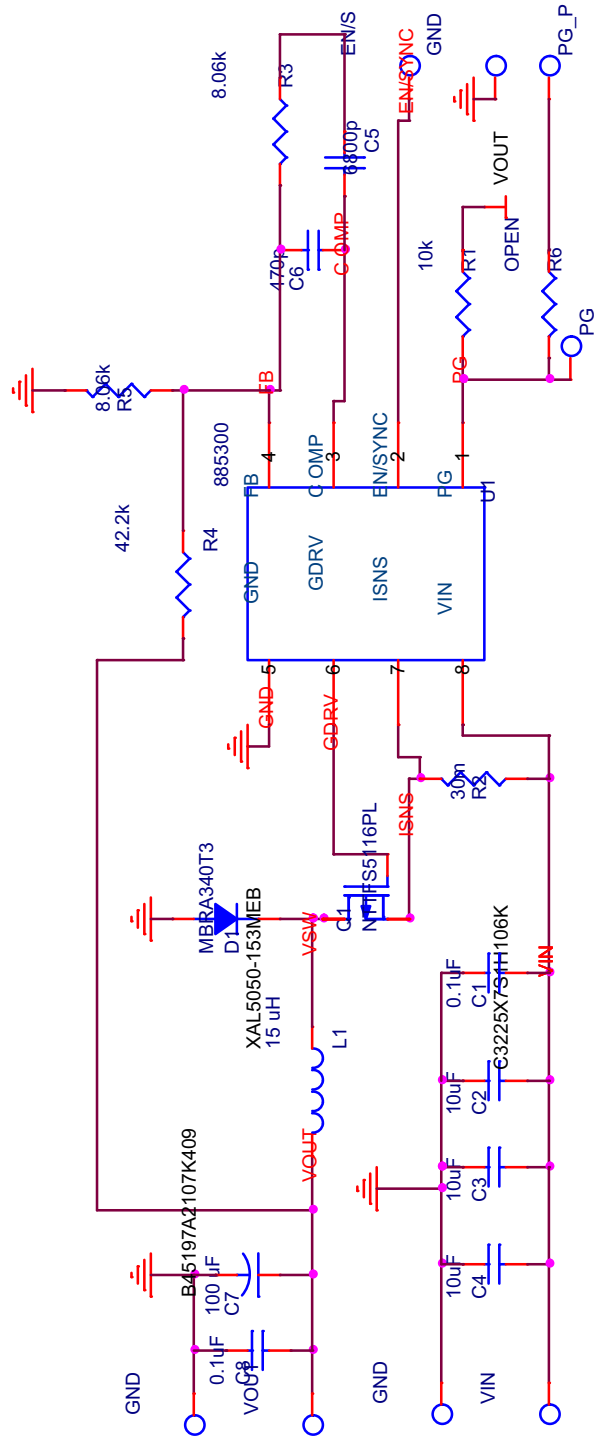


Figure 6. Evaluation Board Schematic

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PCB LAYOUT

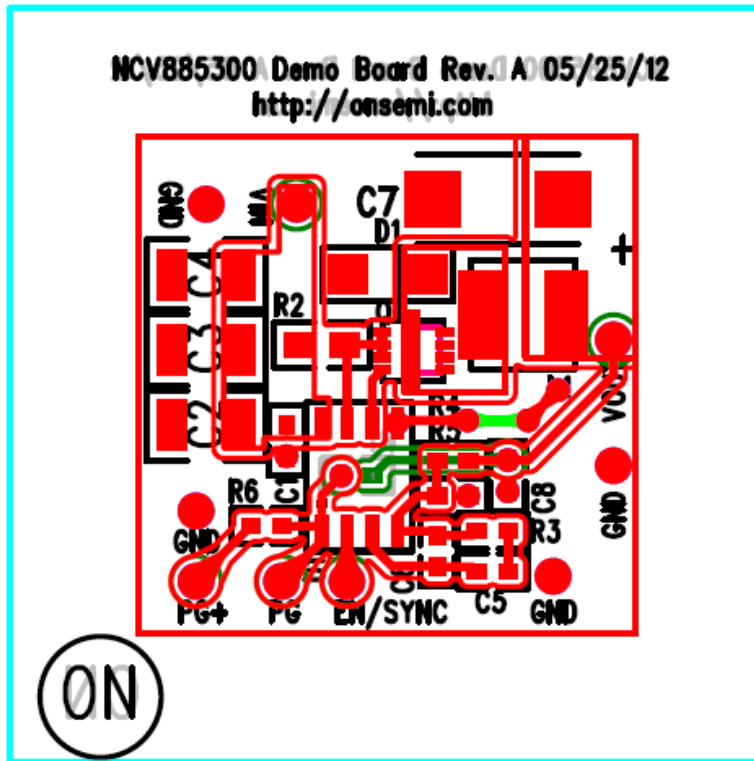


Figure 7. Top View

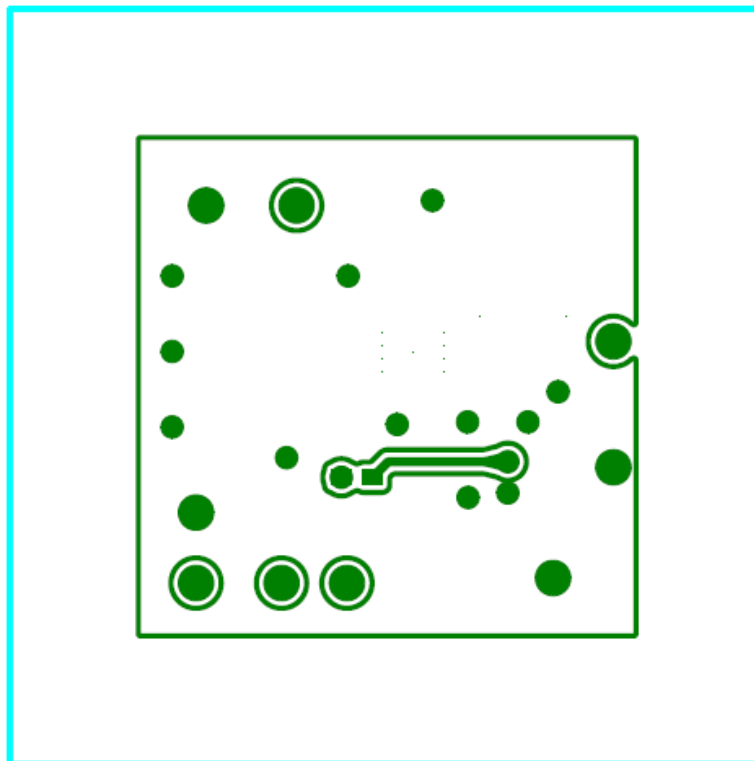


Figure 8. Bottom View

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Table 4. BILL OF MATERIALS

| Reference | Value | Part # | Manufacturer | Description | Package |
|------------|-----------------|--------------------|------------------|-------------------------------|-------------|
| U1 | | NCV885300 | ON Semiconductor | Integrated circuit | SOIC-8 |
| Q1 | | NTTFS5116PL | ON Semiconductor | Power MOSFET, P-Channel | WDFN8 |
| D1 | | MBRA340T3G | ON Semiconductor | Diode, Schottky, 40 V, 3 A | SMA |
| L1 | 15 μ H | XAL5050-153MEB | Coilcraft | Shielded Power Inductor | 5 mm x 5 mm |
| R1 | 10.0 k Ω | CRCW060310K0FKEA | Vishay/Dale | Resistor, 1% | 0603 |
| R2 | 0.03 Ω | WSL0805R0300FEA18 | Vishay/Dale | Resistor, 1% | 0805 |
| R3, R5 | 8.06 k Ω | CRCW06038K06FKEA | Vishay/Dale | Resistor, 1% | 0603 |
| R4 | 42.2 k Ω | CRCW060342K2FKEA | Vishay/Dale | Resistor, 1% | 0603 |
| C1 | 0.1 μ F | GCM188R71H104KA57D | Murata | Capacitor, 50 V, X7R | 0603 |
| C2, C3, C4 | 10 μ F | GRM32DF51H106ZA01L | Murata | Capacitor, 50 V, Y5V | 1210 |
| C5 | 6800 pF | EMK107SD682JA-T | Taiyo Yuden | Capacitor, 16 V | 0603 |
| C6 | 470 pF | 06033A471JAT2A | AVX | Capacitor, 25 V, NP0 | 0603 |
| C7 | 100 μ F | B45197A2107K409 | Kemet | Capacitor, 10 V | 2917 |
| C8 | 0.1 | C0603C104K8RACTU | Kemet | Capacitor, 10 V, X7R | 0603 |

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