NDD60N745U1

N-Channel Power MOSFET
600 V, 745 mΩ

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX
600 V	745 mΩ @ 10 V

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	600	V
Gate-to-Source Voltage			V_{GS}	±25	V
Continuous Drain Current $R_{\theta JC}$	Steady State	T_C = 25°C	I_D	6.6	A
		T_C = 100°C		4.2	
Power Dissipation − $R_{\theta JC}$	Steady State	T_C = 25°C	P_D	84	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	27	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	6.6	A
Single Pulse Drain-to-Source Avalanche Energy (I_D = 2.5 A)			EAS	38	mJ
Peak Diode Recovery (Note 1)			dv/dt	15	V/ns
Lead Temperature for Soldering Leads			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{SD} < 6.6 A, di/dt ≤ 400 A/μs, $V_{DS\ peak}$ ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

THERMAL RESISTANCE

Parameter		Symbol	Value	Unit
Junction-to-Case (Drain) NDD60N745U1		$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient Steady State (Note 3) NDD60N745U1 (Note 2) NDD60N745U1−1 (Note 2) NDD60N745U1−35		$R_{\theta JA}$	47 98 95	°C/W

2. Insertion mounted
3. Surface mounted on FR4 board using 1″ sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

N-Channel MOSFET

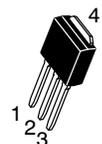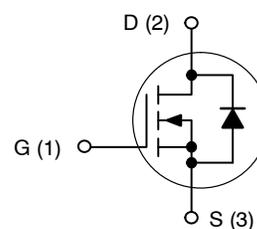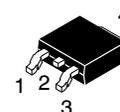

**IPAK
CASE 369D
STYLE 2**

**DPAK
CASE 369C
STYLE 2**

**IPAK
CASE 369AD
STYLE 2**

ORDERING INFORMATION

NDD60N745U1

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 1$ mA		600			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				540		mV/°C
Drain–to–Source Leakage Current	I_{DSS}	$V_{DS} = 600$ V, $V_{GS} = 0$ V	$T_J = 25°C$			1	µA
			$T_J = 125°C$			100	
Gate–to–Source Leakage Current	I_{GSS}	$V_{GS} = \pm20$ V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250$ µA		2	3.2	4	V
Negative Threshold Temperature Co-efficient	$V_{GS(TH)}/T_J$	Reference to 25°C, $I_D = 250$ µA			7.6		mV/°C
Static Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 3.25$ A			610	745	mΩ
Forward Transconductance	g_{FS}	$V_{DS} = 15$ V, $I_D = 3.25$ A			5.6		S
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{iss}	$V_{DS} = 50$ V, $V_{GS} = 0$ V, f = 1 MHz			440		pF
Output Capacitance	C_{oss}				27		
Reverse Transfer Capacitance	C_{rss}				1.5		
Effective output capacitance, energy related (Note 6)	$C_{o(er)}$	$V_{GS} = 0$ V, $V_{DS} = 0$ to 480 V			21		
Effective output capacitance, time related (Note 7)	$C_{o(tr)}$	I_D = constant, $V_{GS} = 0$ V, $V_{DS} = 0$ to 480 V			71		
Total Gate Charge	Q_g	$V_{DS} = 300$ V, $I_D = 6.8$ A, $V_{GS} = 10$ V			15		nC
Gate-to-Source Charge	Q_{gs}				2.9		
Gate-to-Drain Charge	Q_{gd}				7.3		
Plateau Voltage	V_{GP}				5.3		V
Gate Resistance	R_g				4.4		Ω
RESISTIVE SWITCHING CHARACTERISTICS (Note 5)							
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 300$ V, $I_D = 6.8$ A, $V_{GS} = 10$ V, $R_G = 0$ Ω			8		ns
Rise Time	t_r				10		
Turn-off Delay Time	$t_{d(off)}$				19		
Fall Time	t_f				7		
SOURCE–DRAIN DIODE CHARACTERISTICS							
Diode Forward Voltage	V_{SD}	$I_S = 6.6$ A, $V_{GS} = 0$ V	$T_J = 25°C$		0.90	1.6	V
			$T_J = 100°C$		0.82		
Reverse Recovery Time	t_{rr}	$V_{GS} = 0$ V, $V_{DD} = 30$ V $I_S = 6.8$ A, $di/dt = 100$ A/µs			260		ns
Charge Time	t_a				130		
Discharge Time	t_b				130		
Reverse Recovery Charge	Q_{rr}				2.1		µC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
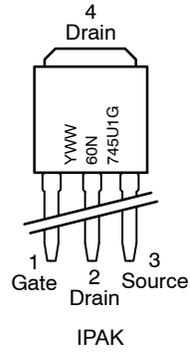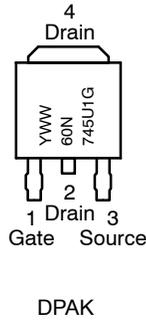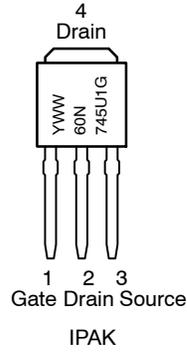4. Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
6. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
7. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

NDD60N745U1

MARKING DIAGRAMS


```
    4
  Drain

  Y W W
  6 0 N
  745U1G

  1   2   3
Gate Drain Source

    IPAK
```

```
    4
  Drain

  Y W W
  6 0 N
  745U1G

      2
  1  Drain  3
Gate     Source

    DPAK
```

```
    4
  Drain

  Y W W
  6 0 N
  745U1G

  1    2    3
Gate  Drain  Source

    IPAK
```

Y   = Year
WW   = Work Week
G   = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping[†]
NDD60N745U1−1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N745U1−35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rali
NDD60N745U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS
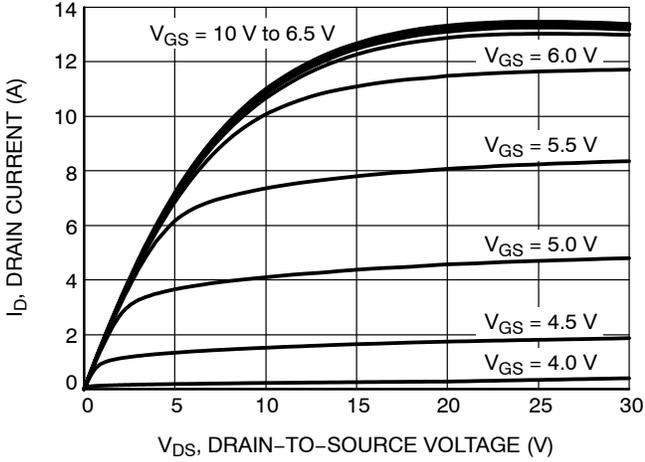
Figure 1. On−Region Characteristics
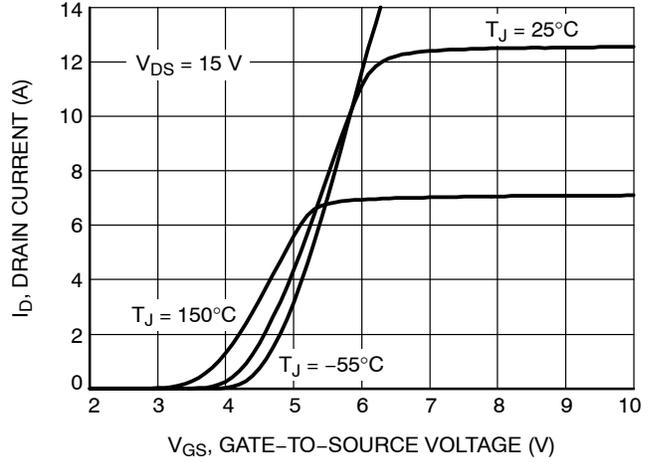
Figure 2. Transfer Characteristics
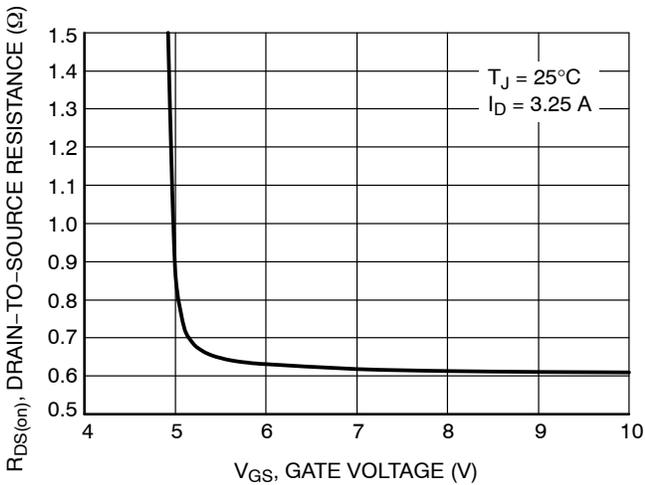
Figure 3. On−Resistance vs. Gate−to−Source Voltage
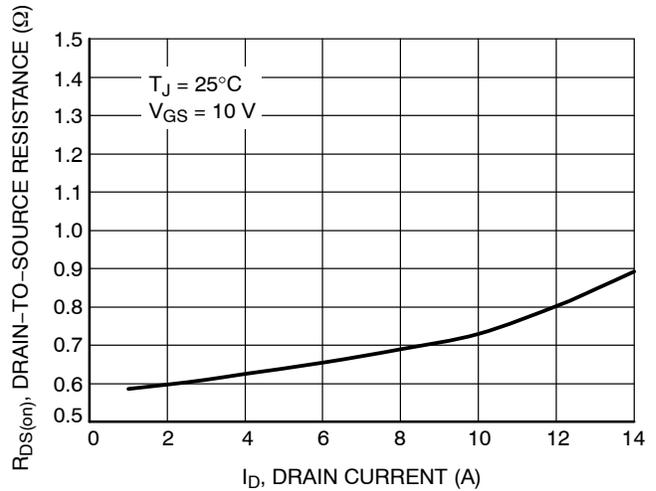
Figure 4. On−Resistance vs. Drain Current and Gate Voltage
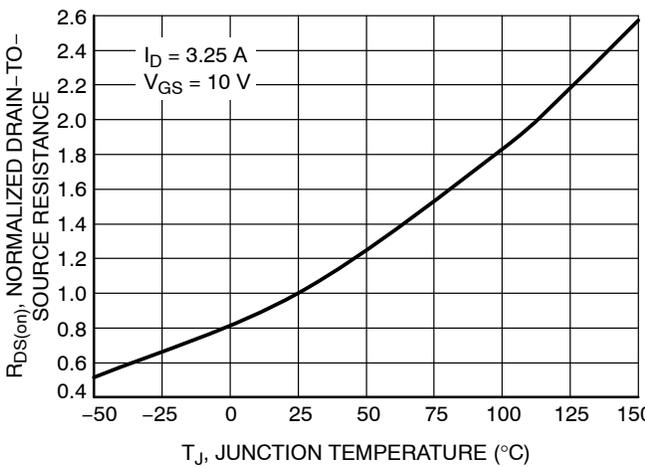
Figure 5. On−Resistance Variation with Temperature
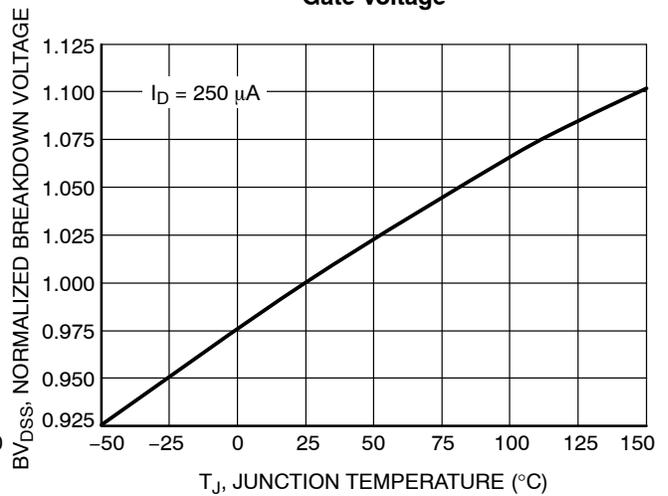
Figure 6. Breakdown Voltage Variation with Temperature

TYPICAL CHARACTERISTICS
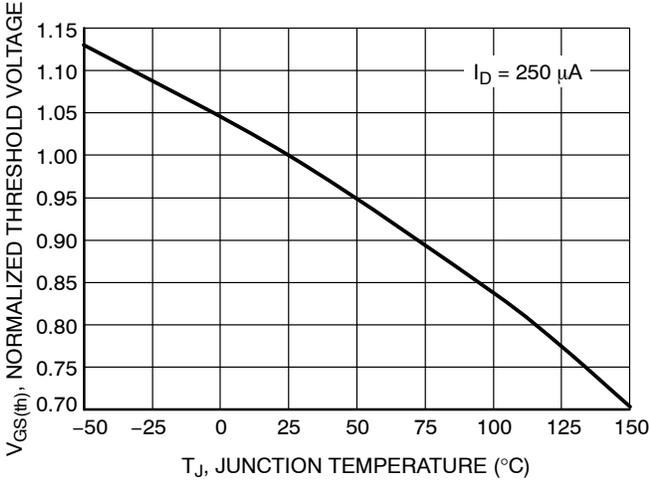
Figure 7. Threshold Voltage Variation with Temperature
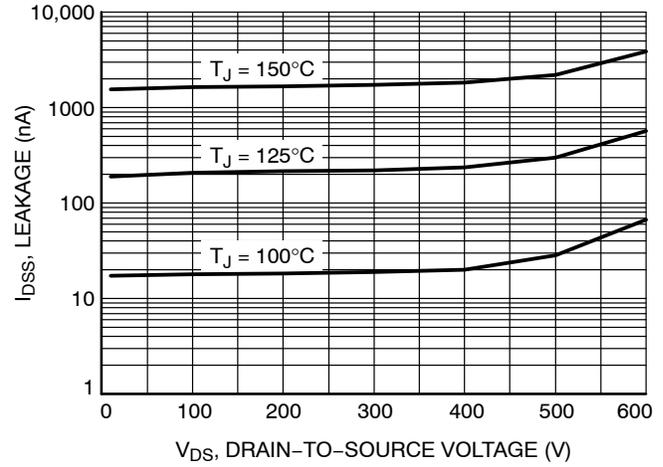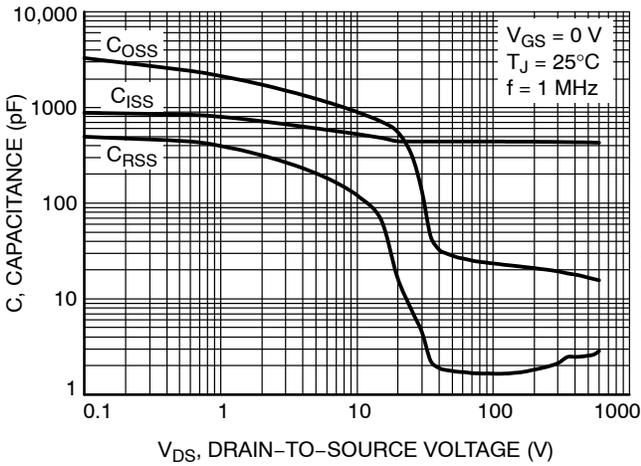

Figure 8. Drain−to−Source Leakage Current vs. Voltage

Figure 9. Capacitance Variation
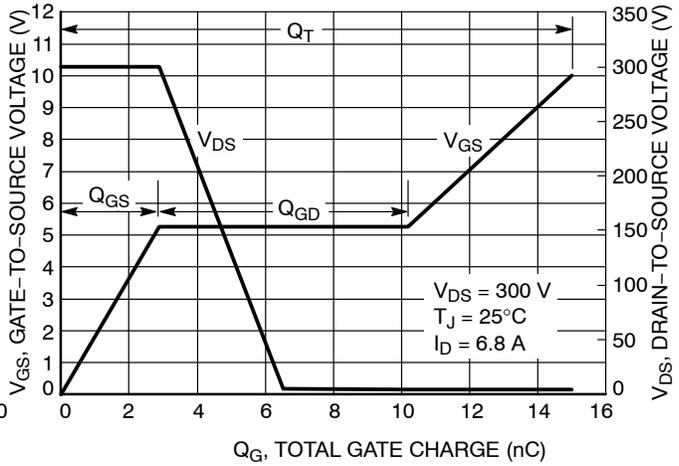
Figure 10. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge
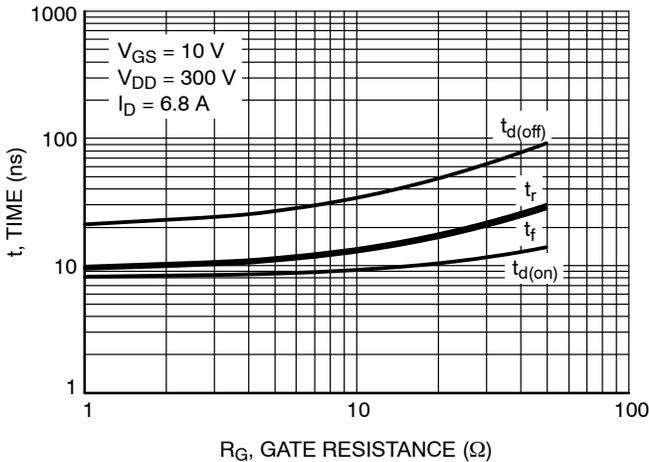
Figure 11. Resistive Switching Time Variation vs. Gate Resistance
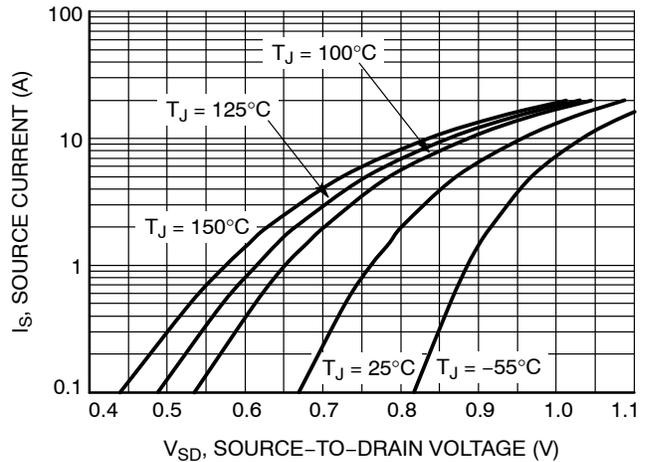
Figure 12. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS
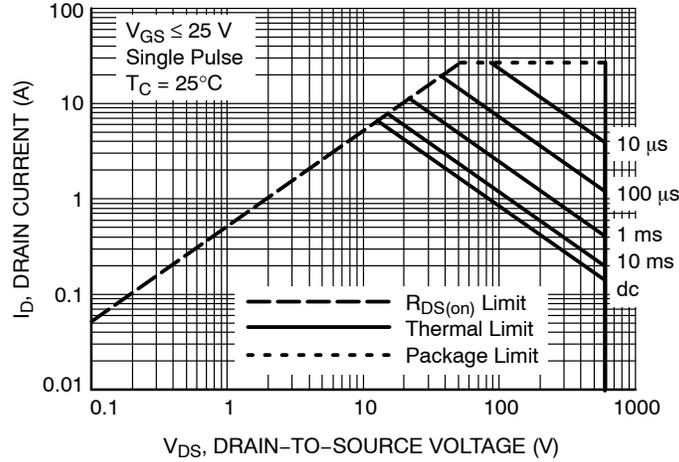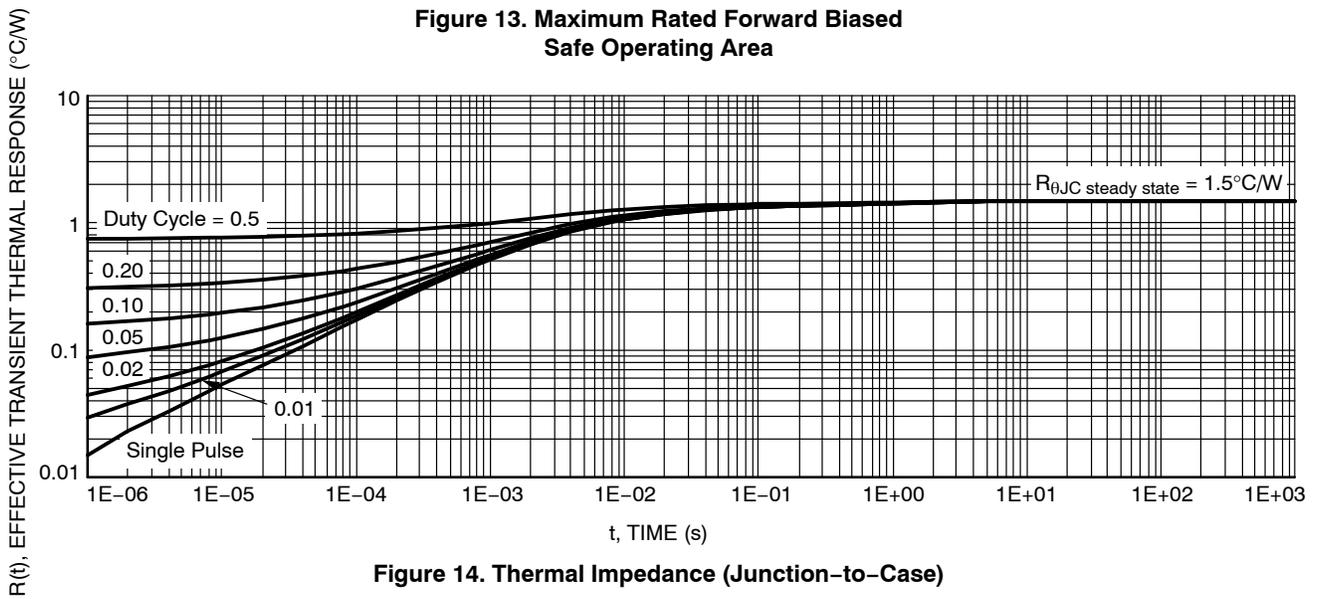

**Figure 13. Maximum Rated Forward Biased
Safe Operating Area**

Figure 14. Thermal Impedance (Junction−to−Case)

IPAK
CASE 369D−01
ISSUE C

DATE 15 DEC 2010

SCALE 1:1
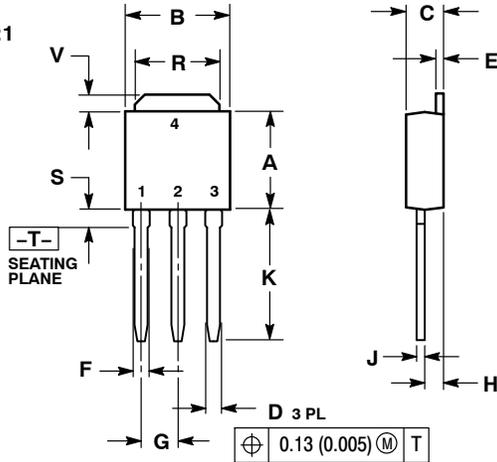
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	–––	3.93	–––

⊕ | 0.13 (0.005) Ⓜ | T

STYLE 1:
PIN 1. BASE
     2. COLLECTOR
     3. EMITTER
     4. COLLECTOR

STYLE 2:
PIN 1. GATE
     2. DRAIN
     3. SOURCE
     4. DRAIN

STYLE 3:
PIN 1. ANODE
     2. CATHODE
     3. ANODE
     4. CATHODE

STYLE 4:
PIN 1. CATHODE
     2. ANODE
     3. GATE
     4. ANODE

STYLE 5:
PIN 1. GATE
     2. ANODE
     3. CATHODE
     4. ANODE

STYLE 6:
PIN 1. MT1
     2. MT2
     3. GATE
     4. MT2

STYLE 7:
PIN 1. GATE
     2. COLLECTOR
     3. EMITTER
     4. COLLECTOR

MARKING DIAGRAMS

Discrete

Integrated Circuits

YWW
XXXXXXXX
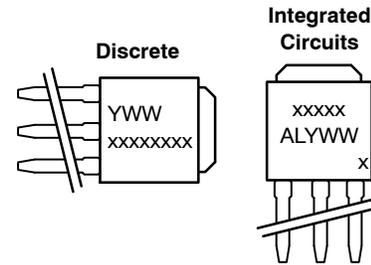
XXXXX
ALYWW
x

xxxxxxxxx = Device Code
A   = Assembly Location
IL   = Wafer Lot
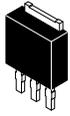Y   = Year
WW   = Work Week

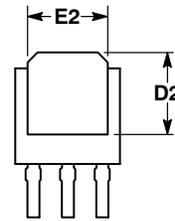| DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)		PAGE 1 OF 1

3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD
ISSUE B

DATE 18 APR 2013

SCALE 1:1
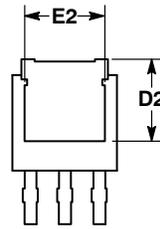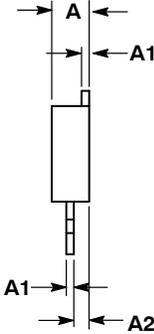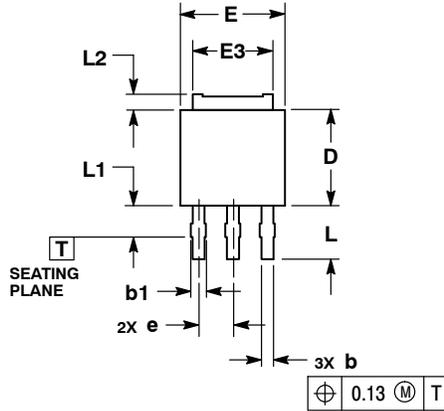
NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

SEATING PLANE

$\oplus$ | 0.13 $\textcircled{M}$ | T

OPTIONAL CONSTRUCTION

GENERIC MARKING DIAGRAMS*

Discrete

AYWW
XXX
XXXXXG

Integrated Circuits

XXXXXXG
ALYWW

STYLE 1:
PIN 1. BASE
     2. COLLECTOR
     3. EMITTER
     4. COLLECTOR

STYLE 2:
PIN 1. GATE
     2. DRAIN
     3. SOURCE
     4. DRAIN
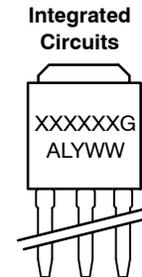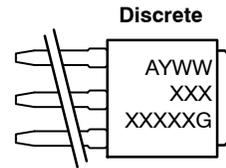
STYLE 3:
PIN 1. ANODE
     2. CATHODE
     3. ANODE
     4. CATHODE

STYLE 4:
PIN 1. CATHODE
     2. ANODE
     3. GATE
     4. ANODE

STYLE 5:
PIN 1. GATE
     2. ANODE
     3. CATHODE
     4. ANODE

STYLE 6:
PIN 1. MT1
     2. MT2
     3. GATE
     4. MT2

STYLE 7:
PIN 1. GATE
     2. COLLECTOR
     3. EMITTER
     4. COLLECTOR

XXXXXX = Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
WW   = Work Week
G   = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.
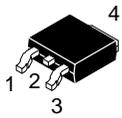
DOCUMENT NUMBER:	98AON23319D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**3.5 MM IPAK, STRAIGHT LEAD**	PAGE 1 OF 1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

SCALE 1:1

TOP VIEW $\quad \oplus \;\; 0.005\;(0.13)\; \text{M} \;\; C$

DETAIL A

SIDE VIEW

BOTTOM VIEW

BOTTOM VIEW
ALTERNATE
CONSTRUCTIONS

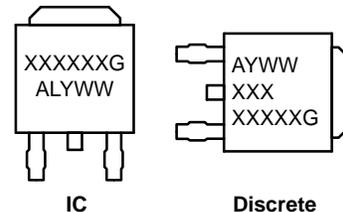GAUGE PLANE

SEATING PLANE

DETAIL A
ROTATED 90° CW
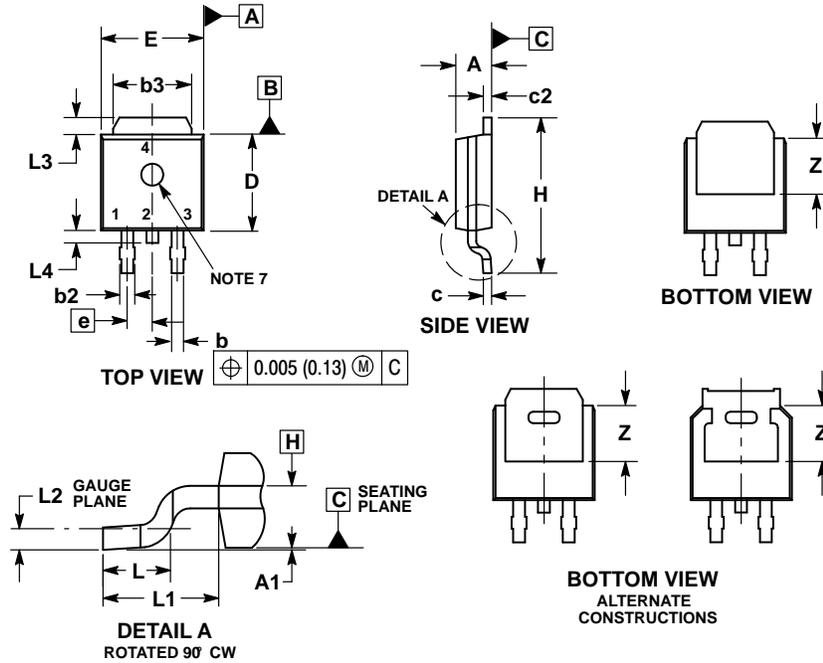
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

IC

Discrete
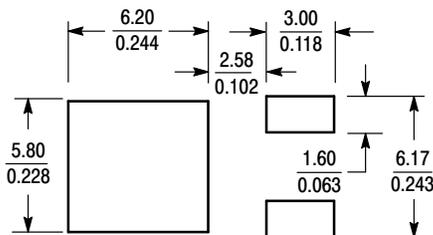
XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*

$\dfrac{6.20}{0.244}$ $\quad$ $\dfrac{3.00}{0.118}$

$\dfrac{2.58}{0.102}$

$\dfrac{5.80}{0.228}$

$\dfrac{1.60}{0.063}$ $\quad$ $\dfrac{6.17}{0.243}$

SCALE 3:1 $\left(\dfrac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC TO−252	
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

PUBLICATION ORDERING INFORMATION

◊

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for MOSFET *category:*

Click to view products by ON Semiconductor *manufacturer:*

Other Similar products are found below :

614233C 648584F MCH3443-TL-E MCH6422-TL-E FW231A-TL-E APT5010JVR NTNS3A92PZT5G IRF100S201 JANTX2N5237
2SK2464-TL-E 2SK3818-DL-E FCA20N60_F109 FDZ595PZ STD6600NT4G FSS804-TL-E 2SJ277-DL-E 2SK1691-DL-E 2SK2545(Q,T)
405094E 423220D MCH6646-TL-E TPCC8103,L1Q(CM 367-8430-0972-503 VN1206L 424134F 026935X 051075F SBVS138LT1G
614234A 715780A NTNS3166NZT5G 751625C 873612G IRF7380TRHR IPS70R2K0CEAKMA1 RJK60S3DPP-E0#T2 RJK60S5DPK-
M0#T0 APT5010JVFR APT12031JFLL APT12040JVR DMN3404LQ-7 NTE6400 JANTX2N6796U JANTX2N6784U
JANTXV2N5416U4 SQM110N05-06L-GE3 SIHF35N60E-GE3 2SK2614(TE16L1,Q) 2N7002KW-FAI APT1201R6BVFRG