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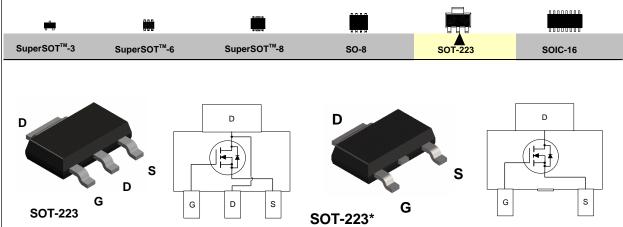
NDT3055 N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 4 A, 60 V. $R_{DS(ON)} = 0.100 \Omega @ V_{GS} = 10 V.$
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.



(J23Z)

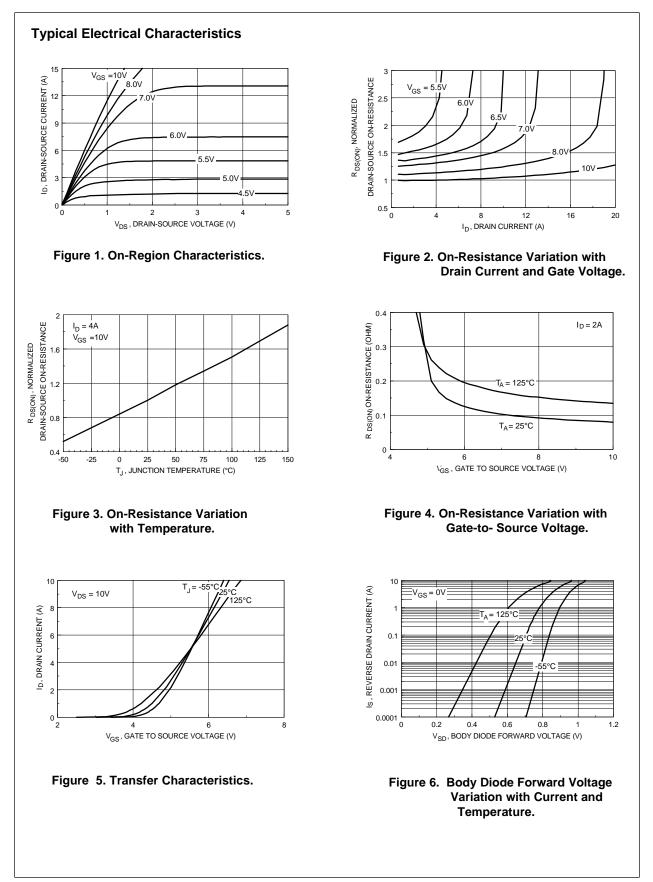
Absolute Maximum Ratings $T_{A} = 25^{\circ}C$ unless otherwise noted

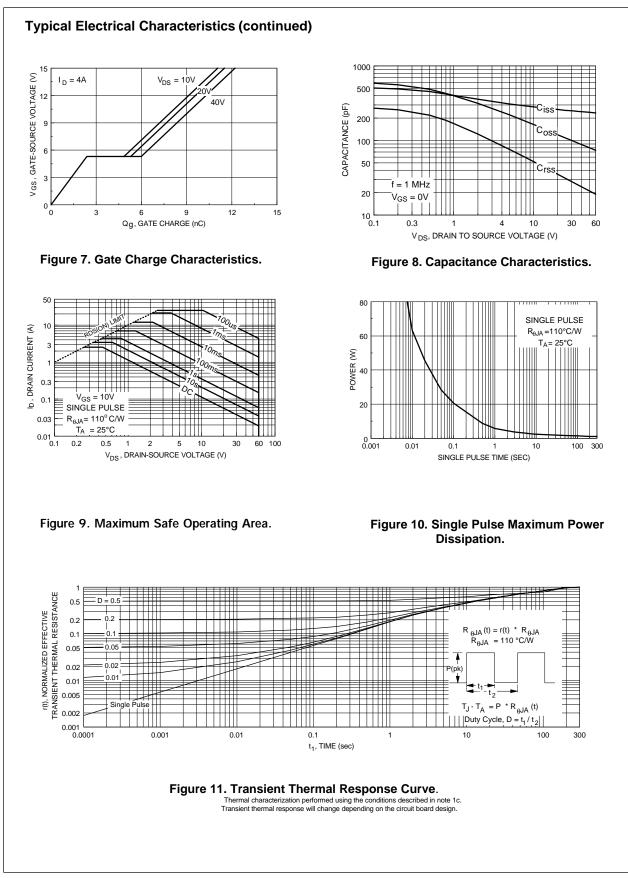
Symbol	Parameter		NDT3055	Units
V _{DSS}	Drain-Source Voltage Gate-Source Voltage - Continuous		60	V
V _{GSS}			±20	V
I _D	Maximum Drain Current - Continuo	JS (Note 1a)	4	A
	- Pulse	1	25	
P _D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
Tj,T _{stg}	Operating and Storage Temperature Range		-65 to 150	C°
THERMA	L CHARACTERISTICS			
R _{eja}	Thermal Resistance, Junction-to-Ar	nbient (Note 1a)	42	°C/W
R ^{өлс}	Thermal Resistance, Junction-to-Ca	ISE (Note 1)	12	°C/W

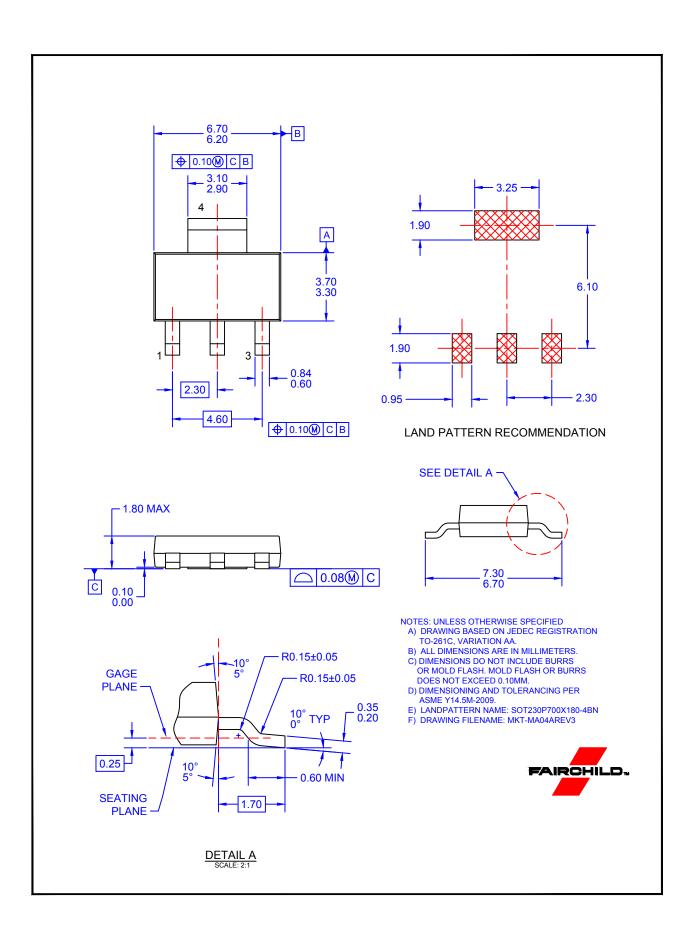
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May 1998

Electrical	Characteristics ($T_A = 25$ °C unless of	herwise noted)					
Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHARA	ACTERISTICS				•		
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		60			V
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_D = 250 \ \mu\text{A}$, Referenced to $25 \ ^\circ\text{C}$			63		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$				10	μA
			T _J =125°C			100	μA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 V, V_{DS} = 0 V$				-100	nA
ON CHARAC	CTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		2	3	4	V
			T _J =125°C	1.5	2.4	3	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 4 \text{ A}$			0.084	0.1	Ω
()			T_=125°C		0.14	0.18	
I _{D(ON)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, \text{ V}_{DS} = 10 \text{ V}$	5	15			А
g _{FS}	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 4 \text{ A}$			6		S
-	HARACTERISTICS			1			
C _{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			250		pF
C _{oss}	Output Capacitance				100		pF
C _{rss}	Reverse Transfer Capacitance				30		pF
	CHARACTERISTICS (Note 2)			1			1
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 25 \text{ V}, \ \text{I}_{D} = 1.2 \text{ A},$ $V_{GS} = 10 \text{ V}, \ \text{R}_{GEN} = 50 \Omega$			10	25	ns
ţ,	Turn - On Rise Time				18	50	ns
t _{D(off)}	Turn - Off Delay Time				37	65	ns
<u>- ()</u> t _i	Turn - Off Fall Time				30	60	ns
Q _g	Total Gate Charge	$V_{DS} = 40 V, I_D = 4 A,$ $V_{GS} = 10 V$			9	15	nC
Q _{gs}	Gate-Source Charge				2.3		nC
Q _{gd}	Gate-Drain Charge				2.6		nC
* *	RCE DIODE CHARACTERISTICS AND MAXI	MUM RATINGS		1			
l _s	Maximum Continuous Drain-Source Diode Fo	rward Current				2.5	А
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = 2.5 A$ (Note 2)			0.85	1.2	V
Notes:	1			1			
-	of the junction-to-case and case-to-ambient thermal resistance will design while R_{gch} is determined by the user's board design.	here the case thermal reference is define	ed as the solder mo	unting surfa	ace of	the drain p	bins. R _{eJC} is
	ing the board layouts shown below on FR-4 PCB in a still air enviro	onment:					
	>						
		Ψ		ψ			
	a. 42°C/W when mounted on a 1 in ² pad of	b. 95°C/W when mounted	1 on a 0.066 in ²		c. 110°C/W w		d on a 0.0012
P	2oz Cu.	pad of 2oz Cu.		ዋዋዋ	in ² pad of 2oz	cu.	
		999		999			
6	ь р <u> </u>						
	letter size paper						
2. Pulse Test: Puls	e Width \leq 300µs, Duty Cycle \leq 2.0%						
							NDT3055 R







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