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### NDT451AN

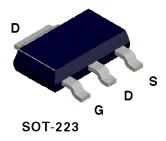
## N-Channel Enhancement Mode Field Effect Transistor

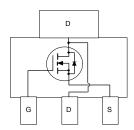
### **General Description**

Power SOT N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

### **Features**

- 7.2A, 30V.  $R_{DS(ON)} = 0.035\Omega$  @  $V_{GS} = 10V$   $R_{DS(ON)} = 0.05\Omega$  @  $V_{GS} = 4.5V$ .
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability in a widely used surface mount package.





**Absolute Maximum Ratings** T<sub>A</sub>= 25°C unless otherwise noted

Symbol	Parameter		NDT451AN	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	± 7.2	Α
	- Pulsed		± 25	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range		-65 to 150	°C
THERMA	L CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$				1	μΑ
			$T_J = 55^{\circ}C$			10	μΑ
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAR	ACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.6	3	V
			T <sub>J</sub> = 125°C	0.7	1.2	2.2	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 7.2 \text{ A}$	<u>.</u>		0.03	0.035	Ω
			T <sub>J</sub> = 125°C		0.042	0.063	
		$V_{GS} = 4.5 \text{ V}, I_{D} = 6.0 \text{ A}$			0.042	0.05	
			T <sub>J</sub> = 125°C		0.058	0.09	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$		25			Α
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		15			
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 7.2 \text{ A}$			11		S
DYNAMIC	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$			720		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			370		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				250		pF
SWITCHII	NG CHARACTERISTICS (Note 2)						
$\mathbf{t}_{D(on)}$	Turn - On Delay Time	$V_{DD} = 10 \text{ V}, I_{D} = 1 \text{ A},$			12	20	ns
ţ,	Turn - On Rise Time	$V_{GEN}$ = 10 V, $R_{GEN}$ = 6 $\Omega$			13	30	ns
$\mathbf{t}_{D(off)}$	Turn - Off Delay Time				29	50	ns
t <sub>r</sub>	Turn - Off Fall Time				10	20	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10 \text{ V},$ $I_{D} = 7.2 \text{ A}, V_{GS} = 10 \text{ V}$			19	30	nC
$Q_{gs}$	Gate-Source Charge				2.3		nC
$Q_{gd}$	Gate-Drain Charge				5.5		nC

Electrical Characteristics (T <sub>A</sub> = 25°C unless otherwise noted)								
Symbol	Parameter	Conditions	Min	Тур	Max	Units		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS								
I <sub>s</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.3	Α		
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.2A (Note 2)		0.9	1.3	V		
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 1.25 A, dI <sub>F</sub> /dt = 100 A/µs			100	ns		

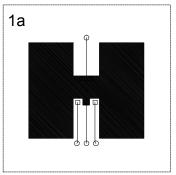
#### Notes:

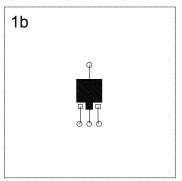
1. R<sub>Bux</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>Bux</sub> is guaranteed by design while R<sub>Bux</sub> is determined by the user's board design.

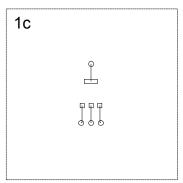
$$P_D(t) = \frac{\tau_{J^-} \tau_A}{R_{\theta J} \, \hat{\chi}^t)} = \frac{\tau_{J^-} \tau_A}{R_{\theta J} \, \hat{\sigma}^R \theta_0 C \hat{\chi}^t)} = I_D^2(t) \times R_{DS(CN)} \hat{q}_{TJ}$$

Typical  $R_{\rm BJA}$  using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 42°C/W when mounted on a 1 in² pad of 2oz copper.
- b. 95°C/W when mounted on a 0.066 in<sup>2</sup> pad of 2oz copper.
- c. 110°C/W when mounted on a 0.0123 in² pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq$  300µs, Duty Cycle  $\leq$  2.0%.

# **Typical Electrical Characteristics**

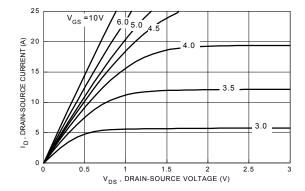


Figure 1. On-Region Characteristics.

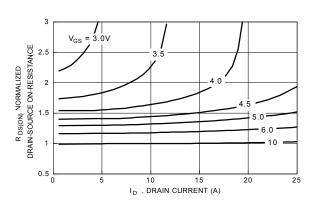


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

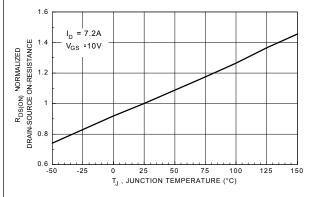


Figure 3. On-Resistance Variation with Temperature.

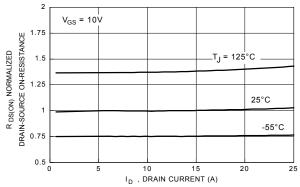


Figure 4. On-Resistance Variation with Drain Current and Temperature.

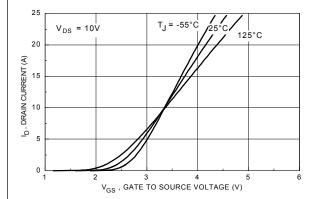


Figure 5. Transfer Characteristics.

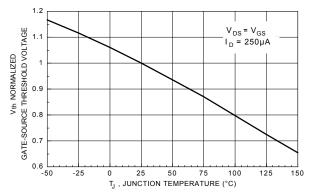


Figure 6. Gate Threshold Variation with Temperature.

# **Typical Electrical Characteristics**

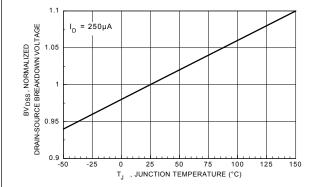


Figure 7. Breakdown Voltage Variation with Temperature.

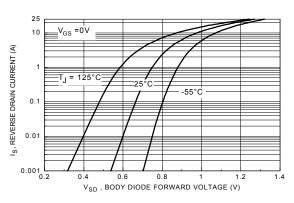


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

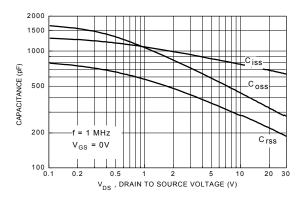


Figure 9. Capacitance Characteristics.

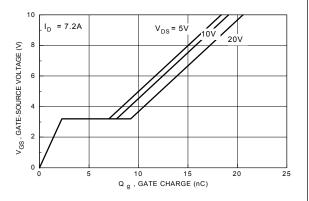


Figure 10. Gate Charge Characteristics.

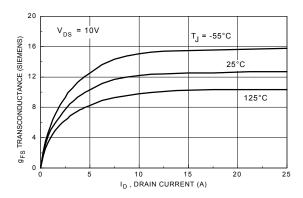


Figure 11. Transconductance Variation with Drain Current and Temperature.

## **Typical Thermal Characteristics**

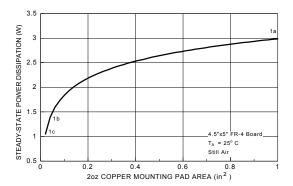


Figure 12. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

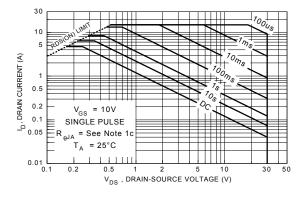


Figure 14. Maximum Safe Operating Area.

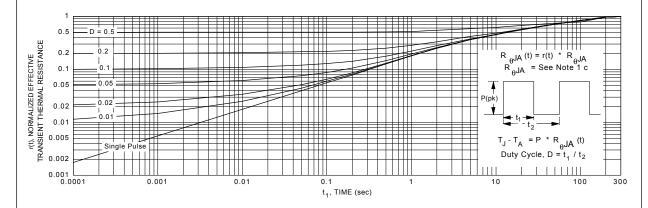


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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