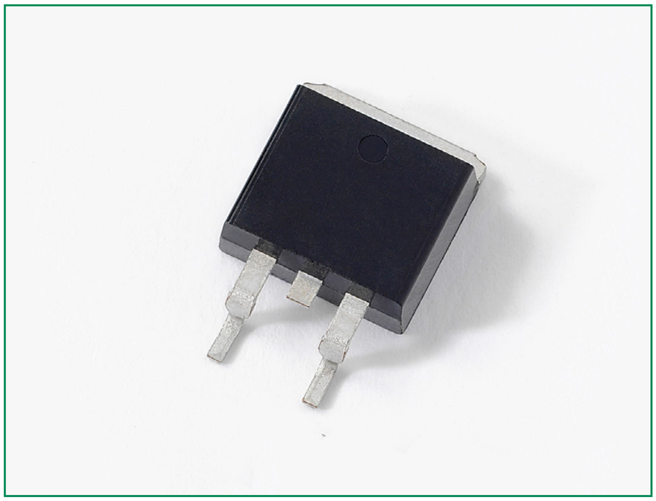
NGB18N40ACLB - 18 A, 400 V, N-Channel Ignition IGBT, D^2PAK



18 Amps, 400 Volts

V_{CE}(on) ≤ 2.0 V @

I_C = 10 A, V_{GE} ≥ 4.5 V

Maximum Ratings (TJ = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	430	V_{DC}
Collector–Gate Voltage	V_{CER}	430	V_{DC}
Gate–Emitter Voltage	V_{GE}	18	V_{DC}
Collector Current–Continuous @TC = 25°C – Pulsed	I_C	18 50	A_{DC} A_{AC}
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @TC = 25°C Derate above 25°C	PD	115 0.77	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

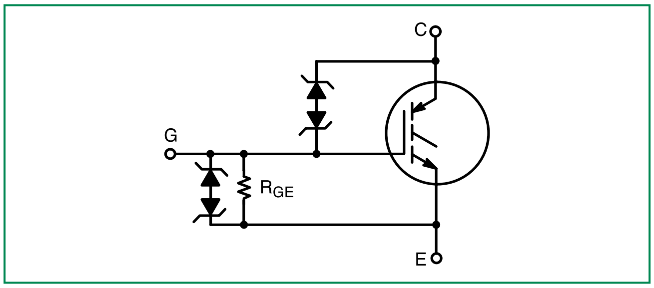
Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil–on–Plug Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor (R_G) and Gate–Emitter Resistor (R_{GE})
- Emitter Ballasting for Short–Circuit Capability
- These are Pb–Free Devices

Functional Diagram



Additional Information

Datasheet | Resources | Samples

Unclamped Collector–To–Emitter Avalanche Characteristics (–55°≤ T_J ≤ 150°C)

Rating	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy			
V_{CC} = 50 V, V_{GE} = 5.0 V, P_k I_L = 21.1 A, L = 1.8 mH, Starting T_J = 25°C	E_{AS}	400	mJ
V_{CC} = 50 V, V_{GE} = 5.0 V, P_k I_L = 18.3 A, L = 1.8 mH, Starting T_J = 125°C		300	
Reverse Avalanche Energy			
V_{CC} = 100 V, V_{GE} = 20 V, P_k I_L = 25.8 A, L = 6.0 mH, Starting T_J = 25°C	$E_{AS\ (R)}$	2000	mJ

Maximum Short-Circuit Times (–55° ≤ T_J ≤ 150°C)

Rating	Symbol	Value	Unit
Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period)	t_{sc1}	750	µs
Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period)	t_{sc2}	5.0	ms

Thermal Characteristics

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W
Thermal Resistance, Junction to Ambient D²PAK (Note 1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	275	°C

Electrical Characteristics - OFF

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Collector–Emitter Clamp Voltage	BV_{CES}	IC = 2.0 mA	TJ = −40°C to 150°C	**380**	**395**	**420**	V_{DC}
		IC = 10 mA	TJ = −40°C to 150°C	**390**	**405**	**430**	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25°C	–	2.0	20	μA
			T_J = 150°C	–	10	40*	
			T_J = −40°C	–	1.0	10	
Reverse Collector–Emitter Leakage Current	I_{ECS}	V_{CE} = −24 V	T_J = 25°C	–	0.7	2.0	mA
			T_J = 150°C	–	12	25*	
			T_J = −40°C	–	0.1	1.0	
Reverse Collector–Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = −75 mA	T_J = 25°C	27	33	37	V_{DC}
			T_J = 150°C	30	36	40	
			T_J = −40°C	25	32	35	
Gate–Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = −40°C to 150°C	11	13	15	V_{DC}
Gate–Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = −40°C to 150°C	384	640	1000	$μA_{DC}$
Gate Emitter Resistor	R_{GE}	–	T_J = −40°C to 150°C	10	16	26	kΩ

Electrical Characteristics - ON (Note 2)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Collector–to–Emitter On–Voltage	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.0	1.4	1.6	V_{DC}
			T_J = 150°C	0.9	1.3	1.6	
			T_J = −40°C	1.1	1.45	1.7*	
		I_C = 8.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.3	1.6	1.9*	
			T_J = 150°C	1.2	1.55	1.8	
			T_J = −40°C	1.4	1.6	1.9*	
		I_C = 10 A, V_{GE} = 4.0 V	T_J = 25°C	1.4	1.8	2.05	
			T_J = 150°C	1.5	1.8	2.0	
			T_J = −40°C	1.4	1.8	2.1*	
		I_C = 15 A, V_{GE} = 4.0 V	T_J = 25°C	1.6	1.9	2.2	
			T_J = 150°C	1.7	2.1	2.3	
			T_J = −40°C	1.6	1.8	2.2	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = 25°C	1.3	1.8	2.0*	
			T_J = 150°C	1.3	1.75	2.0*	
			T_J = −40°C	1.4	1.8	2.0*	
		I_C = 6.5 A, V_{GE} = 3.7 V	T_J = 25°C	–	–	1.65	
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = −40°C to 150°C	8.0	14	25	Mhos

Dynamic Characteristics

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Input Capacitance	C_{ISS}	V_{CC} = 25 V, V_{GE} = 0 V, f = 1.0 MHz	T_J = −40°C to 150°C	400	800	1000	pF
Output Capacitance	C_{OSS}			50	75	100	
Transfer Capacitance	C_{RSS}			4.0	7.0	10	

Switching Characteristics

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Turn–Off Delay Time (Resistive)	$t_{d(off)}$	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	4.0	10	μS
Fall Time (Resistive)	tf	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	9.0	15	
Turn–On Delay Time	$t_{d(on)}$	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω,	T_J = 25°C	–	0.7	4.0	μS
Rise Time	t_r	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω,	T_J = 25°C	–	4.5	7.0	

*Maximum Value of Characteristic across Temperature Range.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

Ratings and Characteristic Curves

Figure 1. Output Characteristics

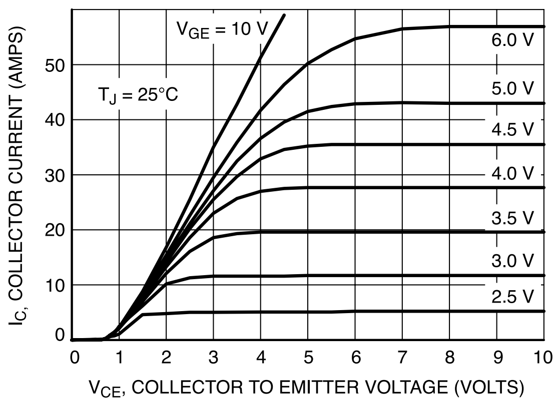


Figure 2. Output Characteristics

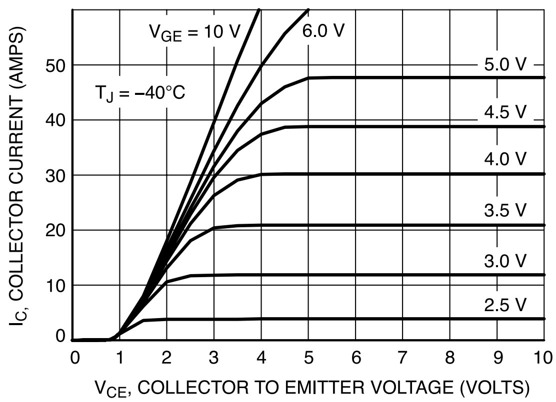


Figure 3. Output Characteristics

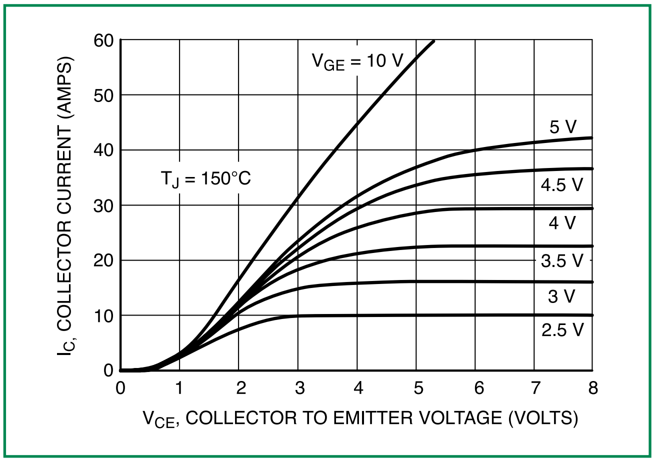


Figure 4. Transfer Characteristics

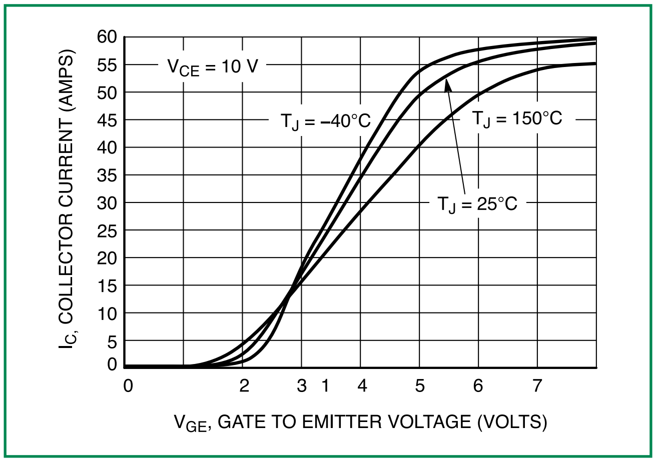


Figure 5. Collector–to–Emitter Saturation Voltage versus Junction Temperature

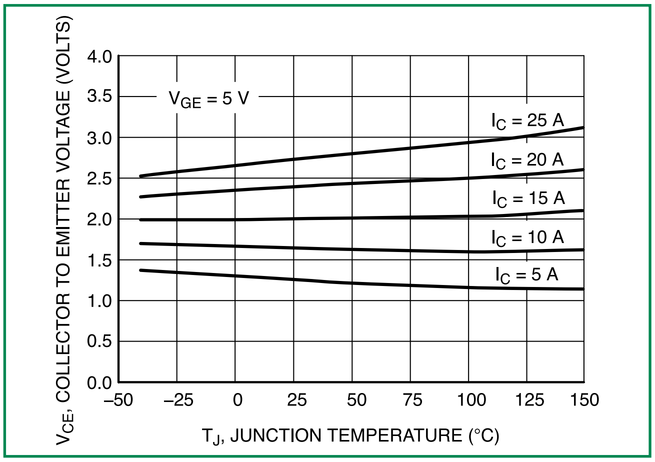


Figure 6. Collector–to–Emitter Voltage versus Gate–to–Emitter Voltage

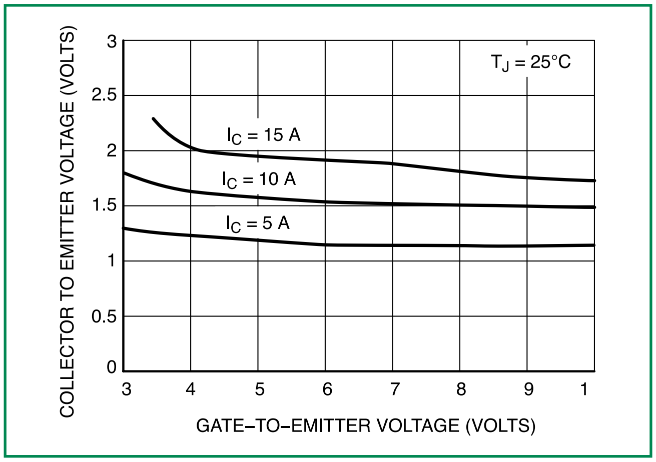


Figure 7. Collector–to–Emitter Voltage versus Gate–to–Emitter Voltage

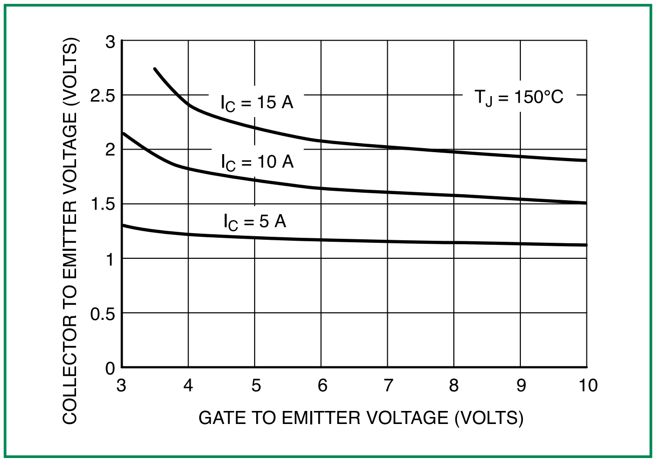


Figure 8. Capacitance Variation

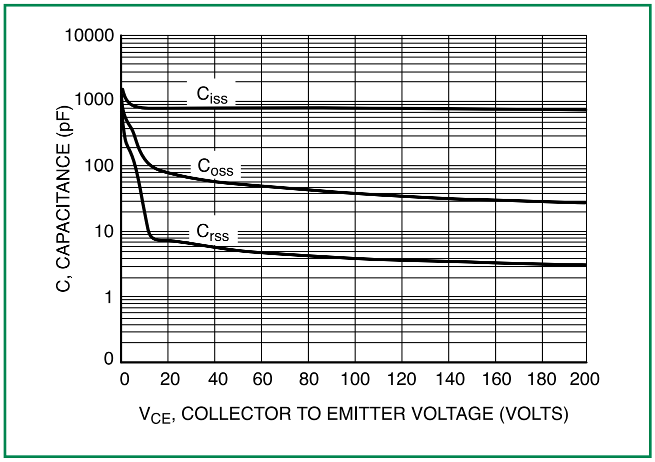


Figure 9. Gate Threshold Voltage versus Temperature

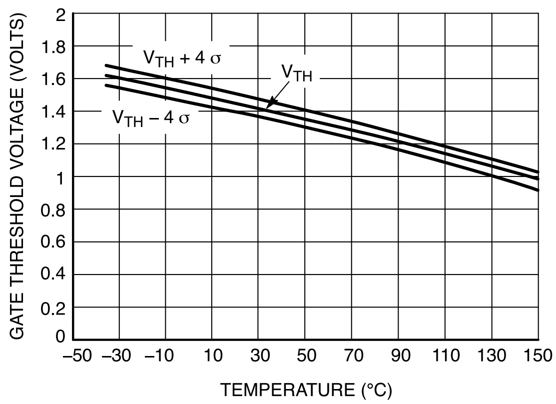


Figure 10. Minimum Open Secondary Latch Current versus Temperature

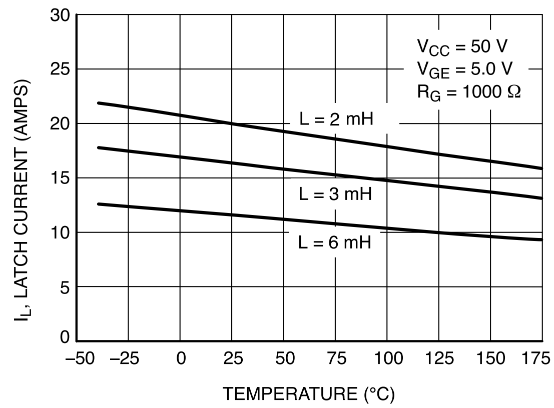


Figure 11. Typical Open Secondary Latch Current versus Temperature

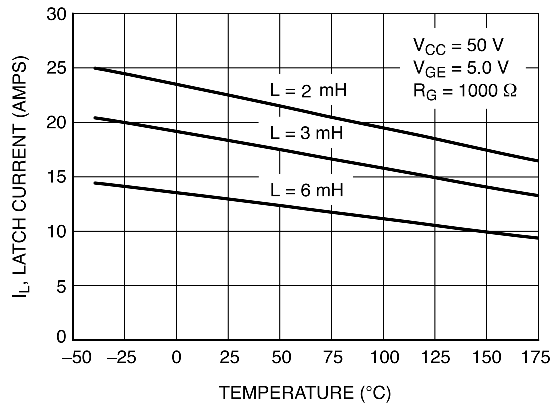


Figure 12. Inductive Switching Fall Time versus Temperature

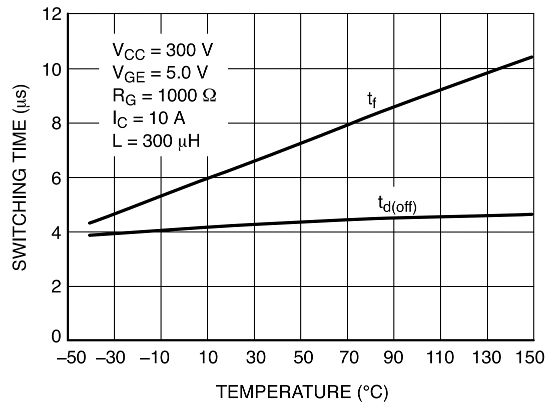


Figure 13. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at T_A = 25°C)

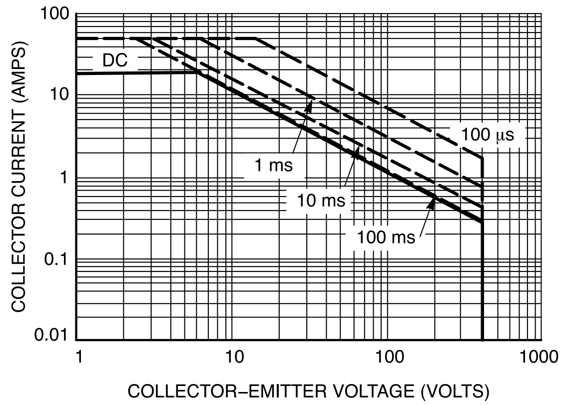


Figure 14. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at T_A = 125°C)

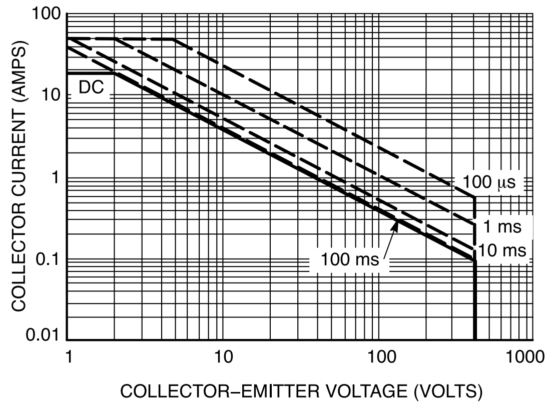


Figure 15. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at T_c = 25°C)

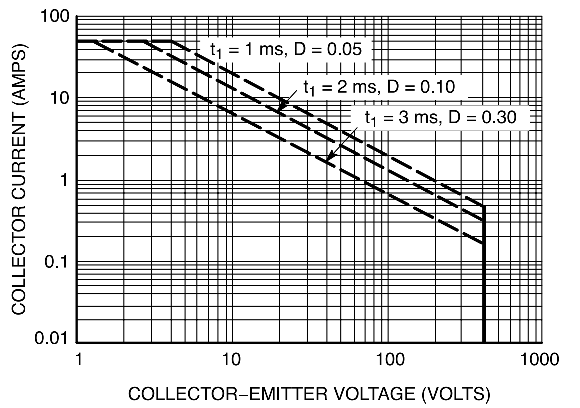


Figure 15. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at T_c = 125°C)

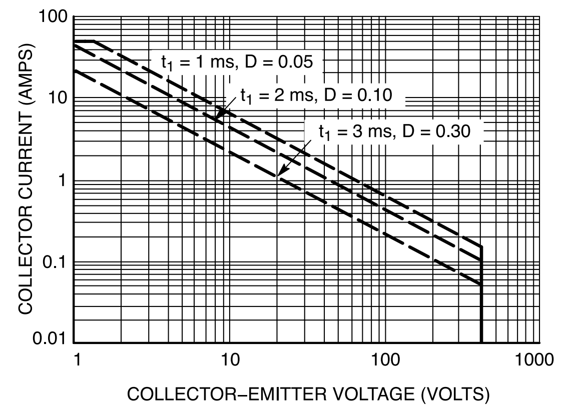


Figure 17. Circuit Configuration for Short Circuit Test #1

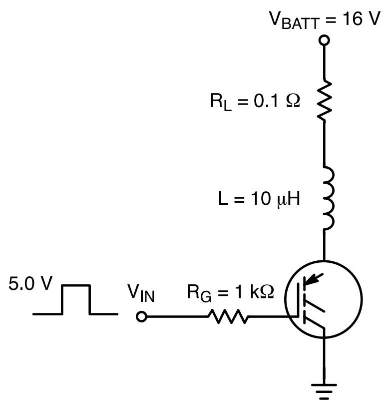


Figure 18. Circuit Configuration for Short Circuit Test #2

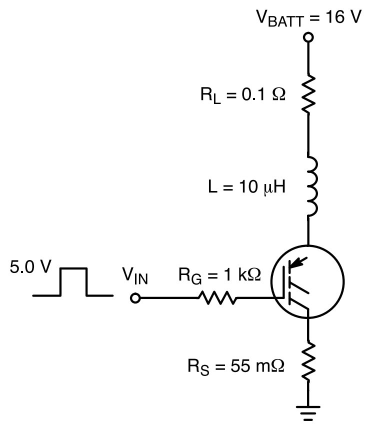
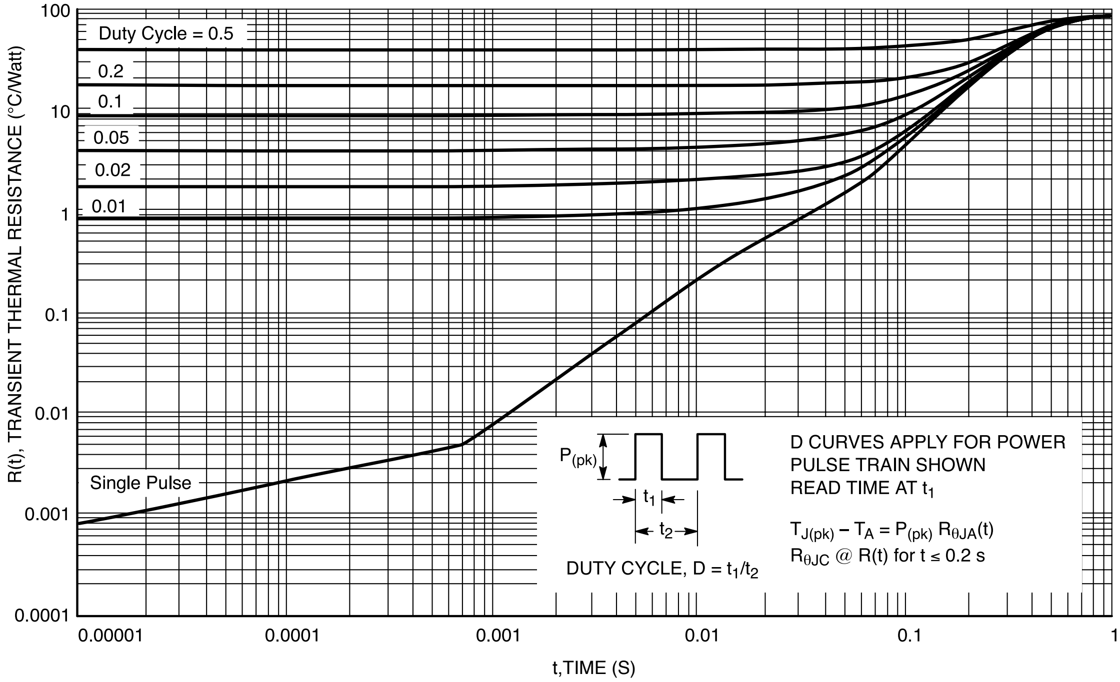
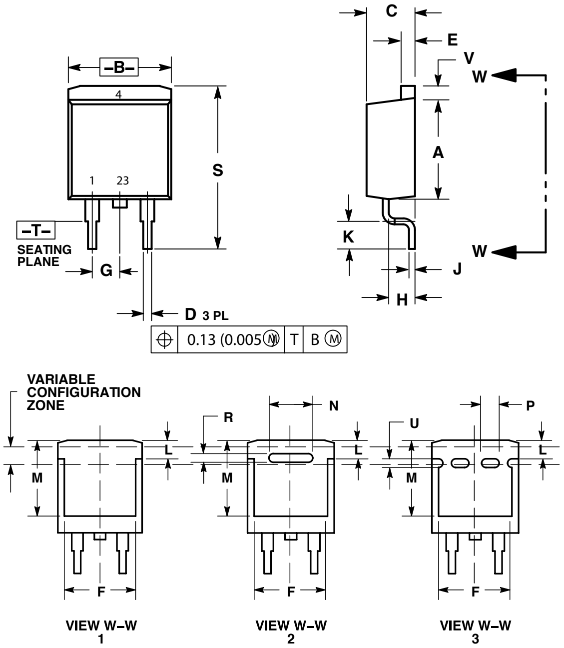


Figure 19. Transient Thermal Resistance (Non–normalized Junction–to–Ambient mounted on minimum pad area)



Dimensions

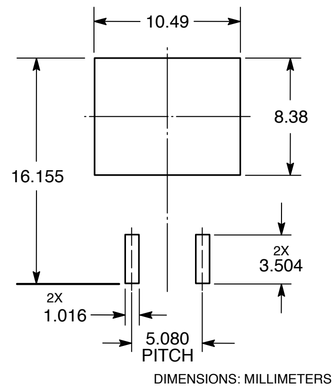


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

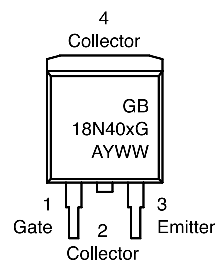
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

Soldering Footrpint



Part Marking System



GB18N40x	= Device Code
x	= B or A
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NGB18N40ACLBT4G	DPAK (Pb–Free)	2500 / Tape & Reel

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