

15 Amps, 410 Volts  
 $V_{CE(on)} \leq 2.1 \text{ V @}$   
 $I_C = 10 \text{ A, } V_{GE} \geq 4.5 \text{ V}$

#### Maximum Ratings ( $T_j = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CES}$	440	$V_{DC}$
Collector–Gate Voltage	$V_{CER}$	440	$V_{DC}$
Gate–Emitter Voltage	$V_{GE}$	15	$V_{DC}$
Collector Current–Continuous @ $T_c = 25^\circ\text{C}$ – Pulsed	$I_C$	15 50	$A_{DC}$ $A_{AC}$
ESD (Human Body Model) $R = 1500 \Omega, C = 100 \text{ pF}$	ESD	8.0	kV
ESD (Machine Model) $R = 0 \Omega, C = 200 \text{ pF}$	ESD	800	V
Total Power Dissipation @ $T_c = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	107 0.71	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_j, T_{stg}$	-55 to +175	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

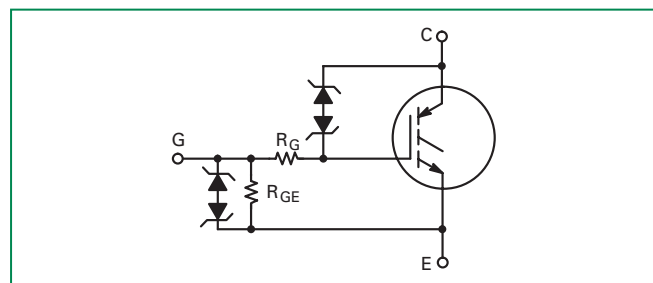
#### Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

#### Features

- Ideal for Coil–on–Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor ( $R_{G1}$ ) and Gate–Emitter Resistor ( $R_{GE}$ )
- These are Pb–Free Devices

#### Functional Diagram



#### Additional Information



Datasheet



Resources



Samples

**Unclamped Collector–To–Emitter Avalanche Characteristics ( $-55^{\circ} \leq T_J \leq 175^{\circ}C$ )**

Rating	Symbol	Value	Unit
<b>Single Pulse Collector–to–Emitter Avalanche Energy</b> $V_{CC} = 50V, V_{GE} = 5.0V, P_k, I_L = 16.6A, L = 1.8mH, \text{Starting } T_C = 25^{\circ}C$ $V_{CC} = 50V, V_{GE} = 5.0V, P_k, I_L = 15A, L = 1.8mH, \text{Starting } T_C = 125^{\circ}C$	$E_{AS}$	250 200	mJ

**Thermal Characteristics**

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^{\circ}C/W$
Thermal Resistance, Junction to Ambient (Note 1)	DPAK (Note 1)	100	
	D <sup>2</sup> PAK (Note 1)	50	
	TO–220	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	275	$^{\circ}C$

**Electrical Characteristics - OFF**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Collector–Emitter Clamp Voltage	$B_{V_{CES}}$	$I_C = 2.0mA$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	380	410	440	$V_{DC}$
		$I_C = 10mA$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	380	410	440	
Zero Gate Voltage Collector Current	$I_{CES}$	$V_{CE} = 350V$ $V_{GE} = 0V$	$T_J = 25^{\circ}C$	–	2.0	20	$\mu A_{DC}$
			$T_J = 150^{\circ}C$	–	10	40*	
			$T_J = -40^{\circ}C$	–	1.0	10	
Reverse Collector–Emitter Leakage Current	$I_{CES}$	$V_{CE} = -24V$	$T_J = 25^{\circ}C$	–	0.7	2.0	mA
			$T_J = 150^{\circ}C$	–	12	25*	
			$T_J = -40^{\circ}C$	–	0.1	1.0	
Reverse Collector–Emitter Leakage Current	$B_{V_{CES(R)}}$	$I_C = -75mA$	$T_J = 25^{\circ}C$	27	33	37	$V_{DC}$
			$T_J = 150^{\circ}C$	30	36	40	
			$T_J = -40^{\circ}C$	25	31	35	
Gate–Emitter Clamp Voltage	$BV_{GES}$	$I_G = 5.0mA$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	11	13	15	$V_{DC}$
Gate–Emitter Leakage Current	$I_{GES}$	$V_{GE} = \pm 10V$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	384	640	1000	$\mu A_{DC}$
Gate Resistor	$R_G$	–	$T_J = -40^{\circ}C$ to $150^{\circ}C$	–	70	–	$\Omega$
Gate–Emitter Resistor	$R_{GE}$	–	$T_J = -40^{\circ}C$ to $150^{\circ}C$	10	16	26	k $\Omega$
Gate Emitter Resistor	$R_{GE}$	–	$T_J = -40^{\circ}C$ to $150^{\circ}C$	14.25	16	25	k $\Omega$

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**Electrical Characteristics - ON (Note 3)**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GE(th)}$	$I_C = 1.0\text{ mA}$ , $V_{GE} = V_{CE}$	$T_J = 25^\circ\text{C}$	1.1	1.4	1.9	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.75	1.0	1.4	
			$T_J = -40^\circ\text{C}$	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/°C
Collector-to-Emitter On-Voltage	$V_{CE(on)}$	$V_{GE} = 4.0\text{ V}$ , $I_C = 6.0\text{ A}$	$T_J = 25^\circ\text{C}$	1.0	1.6	1.8	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.9	1.5	1.8	
			$T_J = -40^\circ\text{C}$	1.1	1.65	1.9*	
		$V_{GE} = 4.0\text{ V}$ , $I_C = 8.0\text{ A}$	$T_J = 25^\circ\text{C}$	1.3	1.8	2.0*	
			$T_J = 150^\circ\text{C}$	1.2	1.7	1.9	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.0*	
		$V_{GE} = 4.0\text{ V}$ , $I_C = 10\text{ A}$	$T_J = 25^\circ\text{C}$	1.4	2.0	2.2	
			$T_J = 150^\circ\text{C}$	1.5	2.0	2.3*	
			$T_J = -40^\circ\text{C}$	1.4	2.0	2.2	
		$V_{GE} = 4.5\text{ V}$ , $I_C = 10\text{ A}$	$T_J = 25^\circ\text{C}$	1.3	1.9	2.1	
			$T_J = 150^\circ\text{C}$	1.3	1.9	2.1	
			$T_J = -40^\circ\text{C}$	1.4	1.95	2.1*	
Forward Transconductance	gfs	$V_{CE} = 5.0\text{ V}$ , $I_C = 6.0\text{ A}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	8	15	25	Mhos

**Dynamic Characteristics**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Input Capacitance	$C_{ISS}$	$V_{CE} = 25\text{ V}$ $V_{GE} = 0\text{ V}$ $f = 1.0\text{ MHz}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	400	650	1000	pF
Output Capacitance	$C_{OSS}$			30	55	100	
Transfer Capacitance	$C_{RSS}$			3.0	4.5	8.0	

**Switching Characteristics**

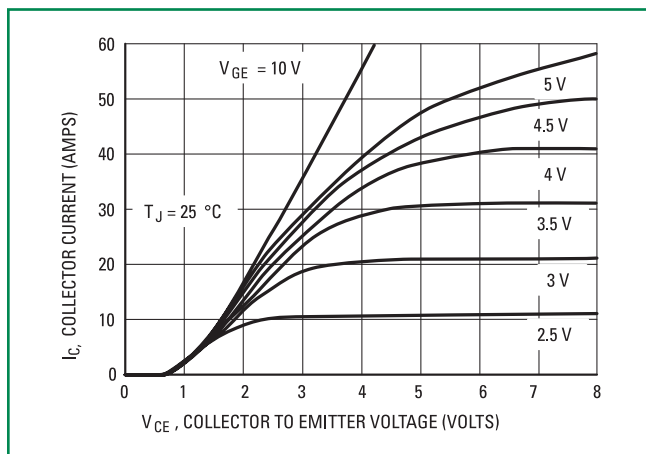
Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
Turn-On Delay Time (Inductive)	$t_{d(off)}$	$V_{CC} = 300\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $L = 300\text{ }\mu\text{H}$	$T_J = 25^\circ\text{C}$	-	4.0	10	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	4.5	10	
Fall Time (Inductive)	$t_f$	$V_{CC} = 300\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $L = 300\text{ }\mu\text{H}$	$T_J = 25^\circ\text{C}$	-	6.0	12	
			$T_J = 150^\circ\text{C}$	-	10	12	
Turn-Off Delay Time (Resistive)	$t_{d(off)}$	$V_{CC} = 300\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $R_L = 46\text{ }\Omega$	$T_J = 25^\circ\text{C}$	-	3.0	10	
			$T_J = 150^\circ\text{C}$	-	3.5	10	
Fall Time (Resistive)	$t_f$	$V_{CC} = 300\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $R_L = 46\text{ }\Omega$	$T_J = 25^\circ\text{C}$	-	8.0	15	
			$T_J = 150^\circ\text{C}$	-	12	15	
Turn-Off Delay Time (Inductive)	$t_{d(on)}$	$V_{CC} = 10\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $R_L = 1.5\text{ }\Omega$	$T_J = 25^\circ\text{C}$	-	0.7	4.0	
			$T_J = 150^\circ\text{C}$	-	0.7	4.0	
Rise Time	$t_r$	$V_{CC} = 10\text{ V}$ $I_C = 6.5\text{ A}$ $R_G = 1.0\text{ k}\Omega$ $R_L = 1.5\text{ }\Omega$	$T_J = 25^\circ\text{C}$	-	4.0	7.0	
			$T_J = 150^\circ\text{C}$	-	5.0	7.0	

\*Maximum Value of Characteristic across Temperature Range.

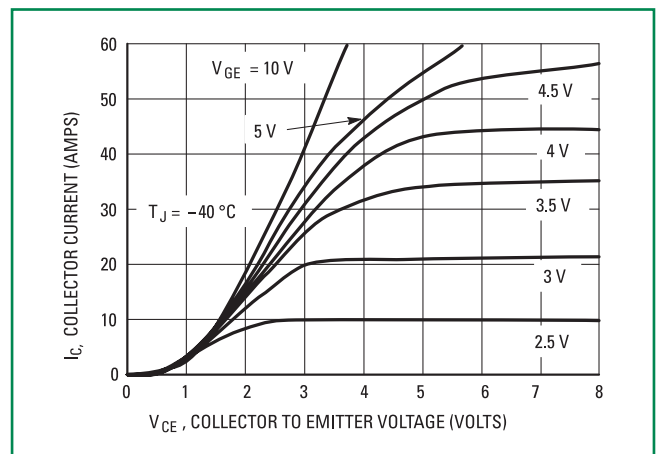
3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

**Ratings and Characteristic Curves**

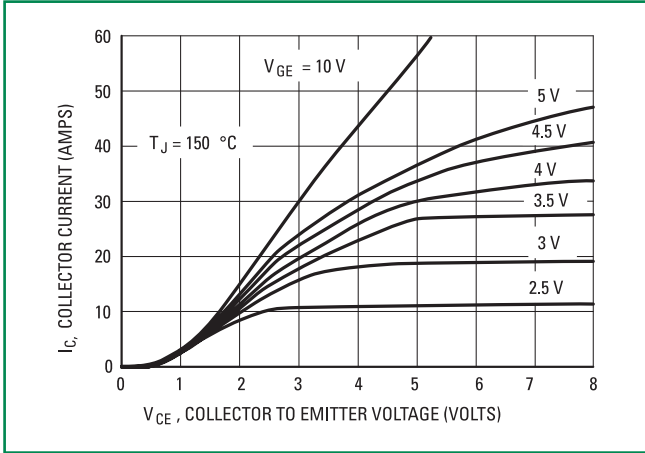
**Figure 1. Output Characteristics**



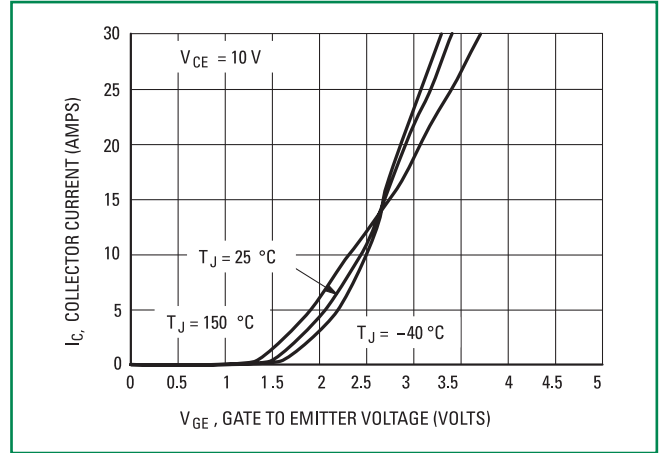
**Figure 2. Output Characteristics**



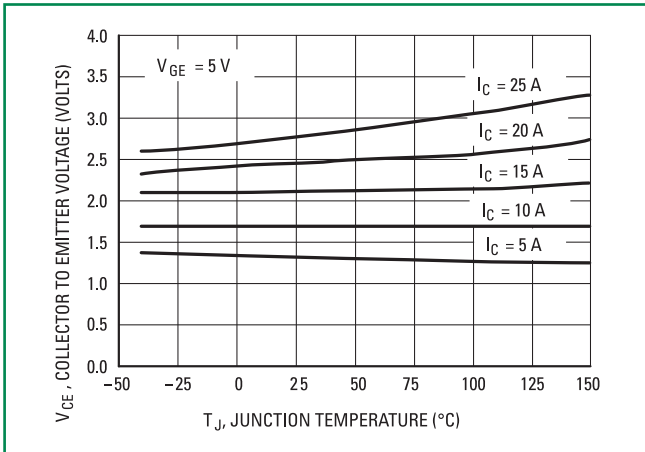
**Figure 3. Output Characteristics**



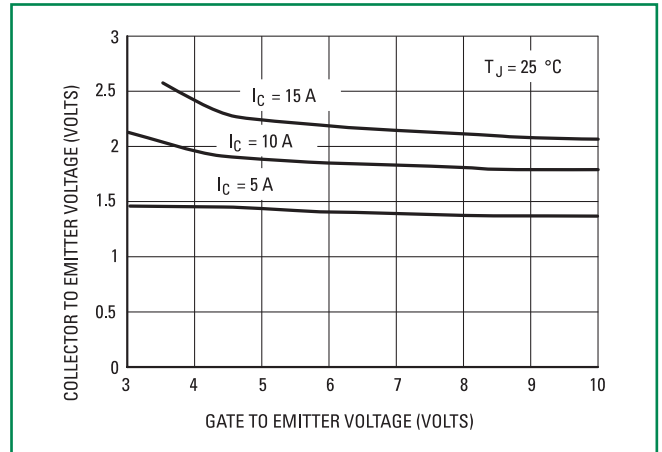
**Figure 4. Transfer Characteristics**



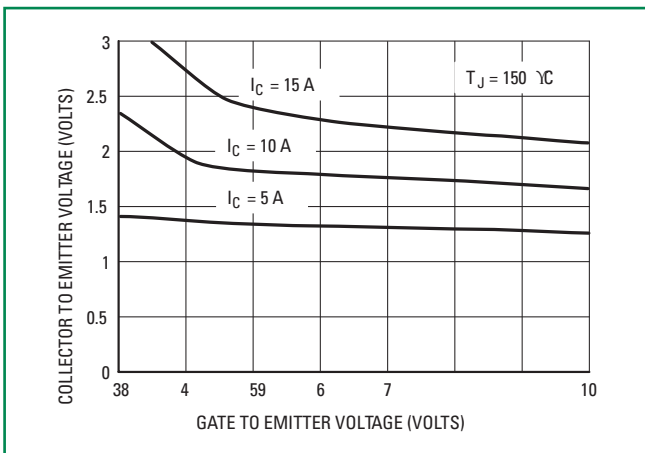
**Figure 5. Collector-to-Emitter Saturation Voltage vs. Junction Temp**



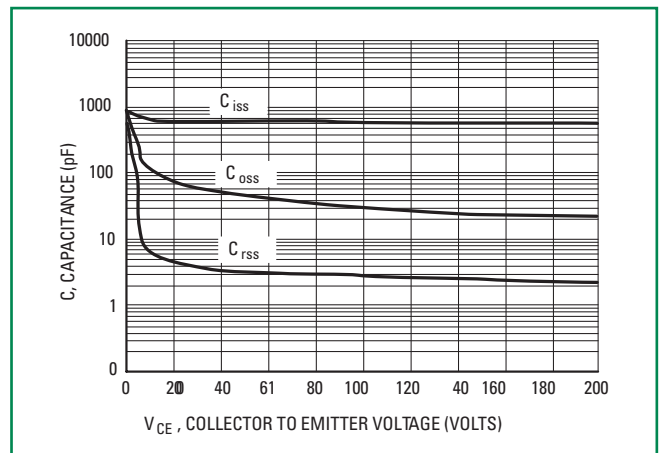
**Figure 6. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage**



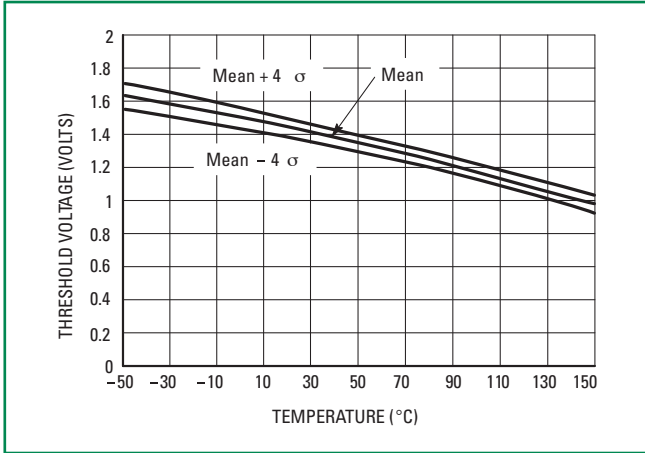
**Figure 7. Collector-to-Emitter Voltage vs Gate-to-Emitter Voltage**



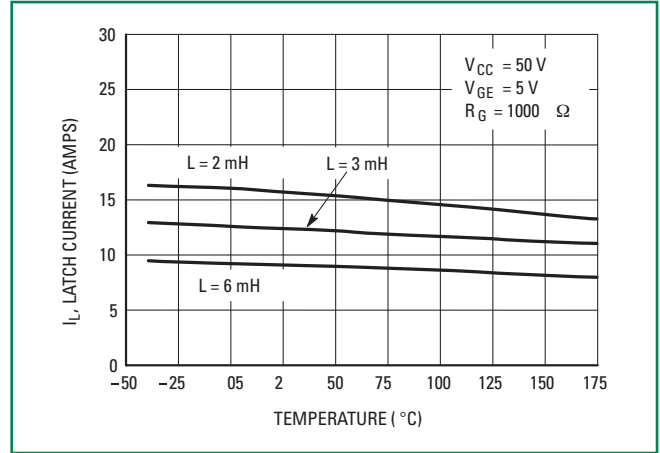
**Figure 8. Capacitance Variation**



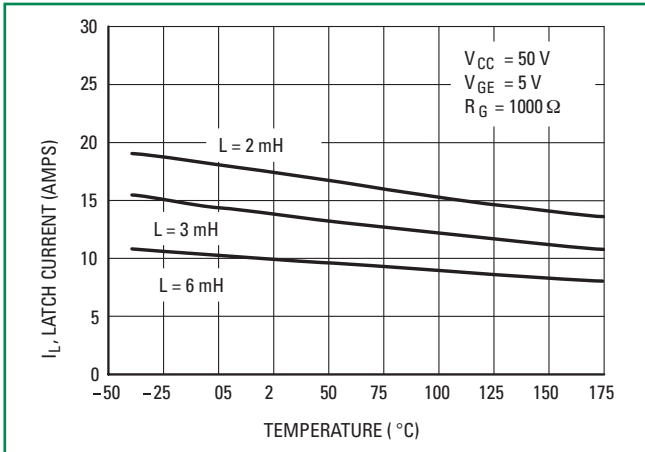
**Figure 9. Gate Threshold Voltage vs. Temperature**



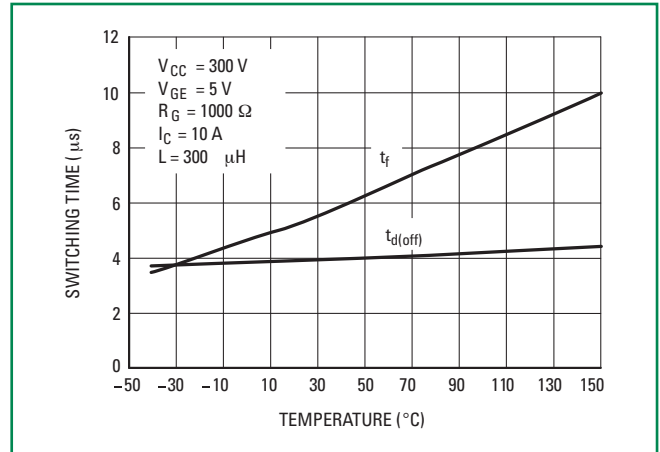
**Figure 10. Minimal Open Secondary Latch Current vs Temperature**



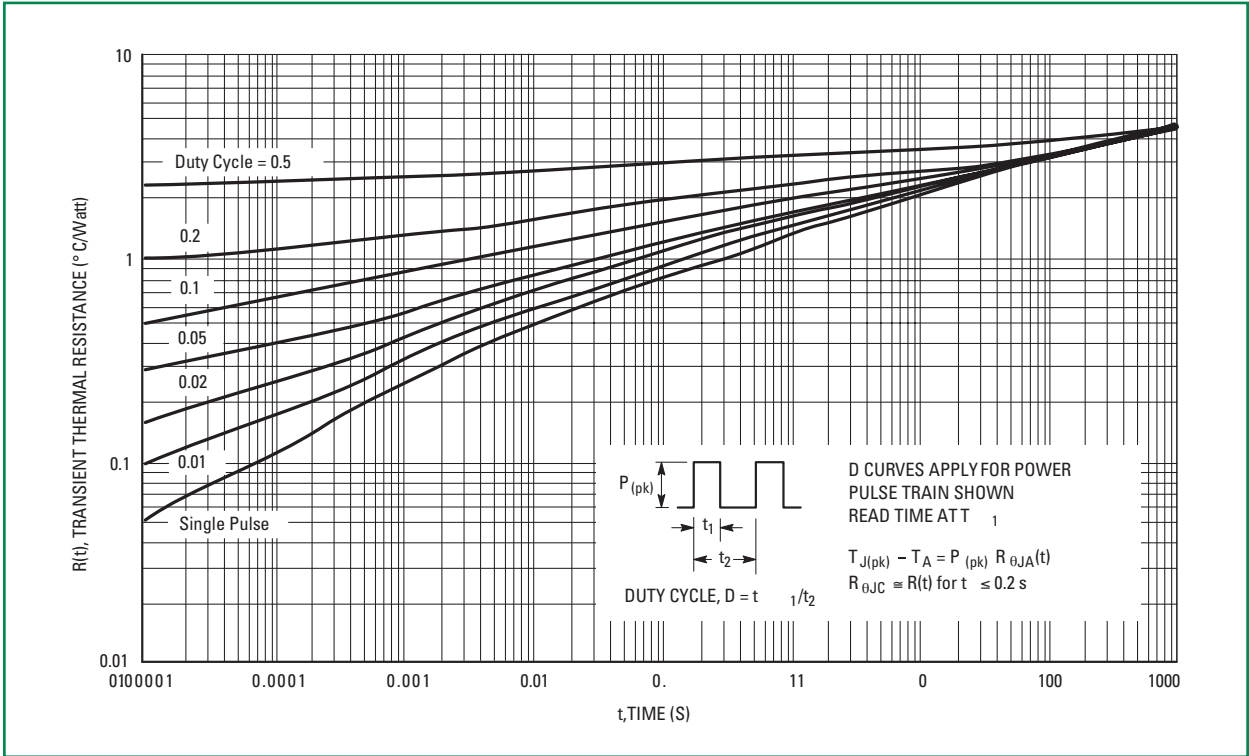
**Figure 11. Typical Open Secondary Latch Current vs Temperature**



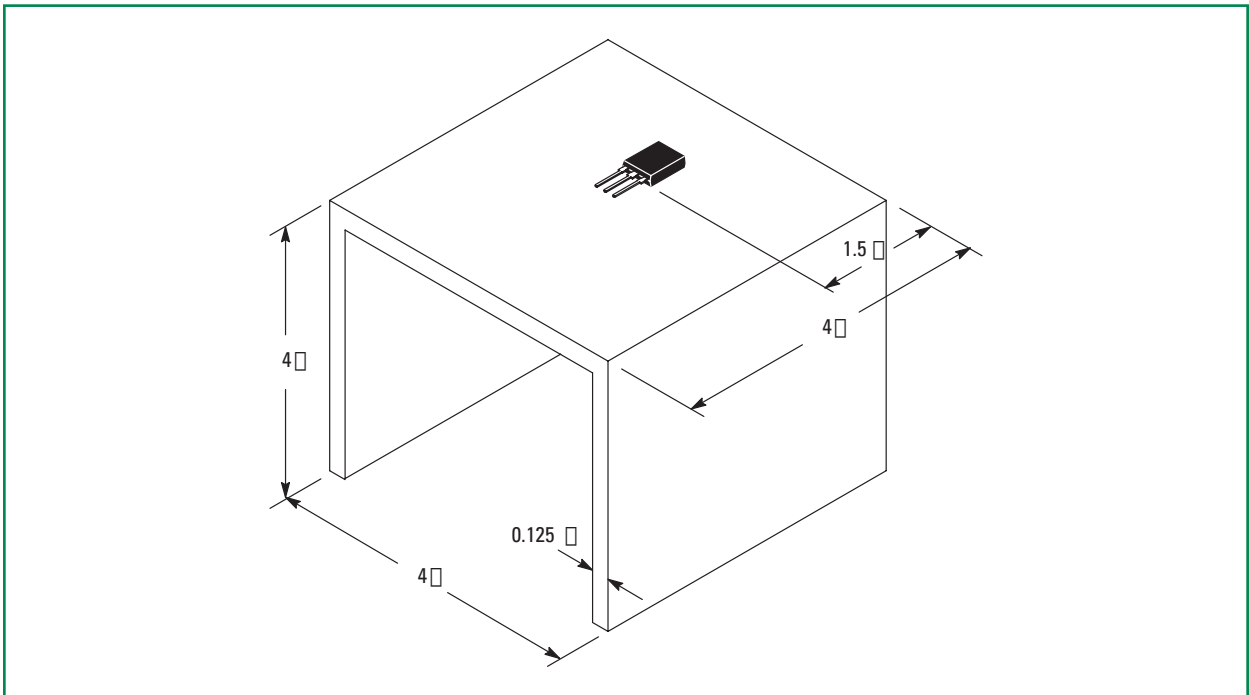
**Figure 12. Inductive Switching Fall Time vs. Temperature**



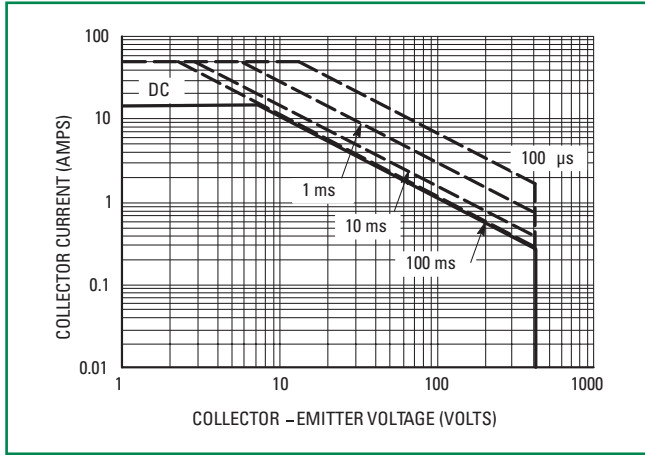
**Figure 13. Transient Thermal Resistance (Non-normalized Junction-to-Ambient mounted on fixture in Figure 14)**



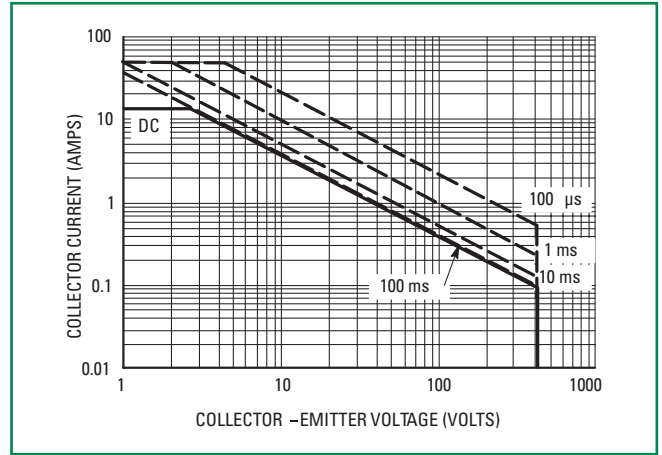
**Figure 14. Test Fixture for Transient Thermal Curve (48 square inches of 1/8" thick aluminum)**



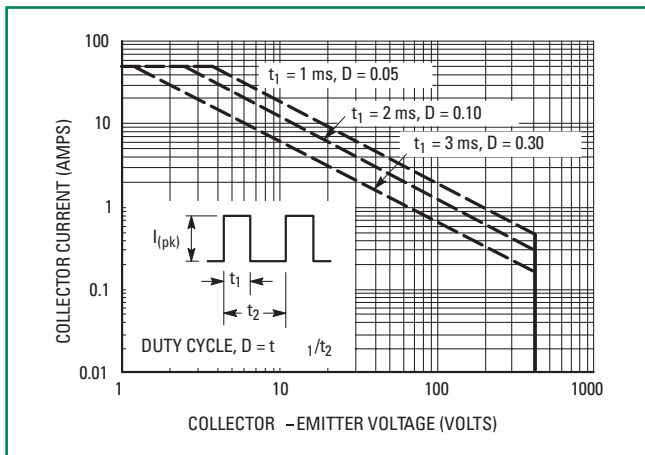
**Figure 15. Single Pulse Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_A = 25^\circ\text{C}$ )



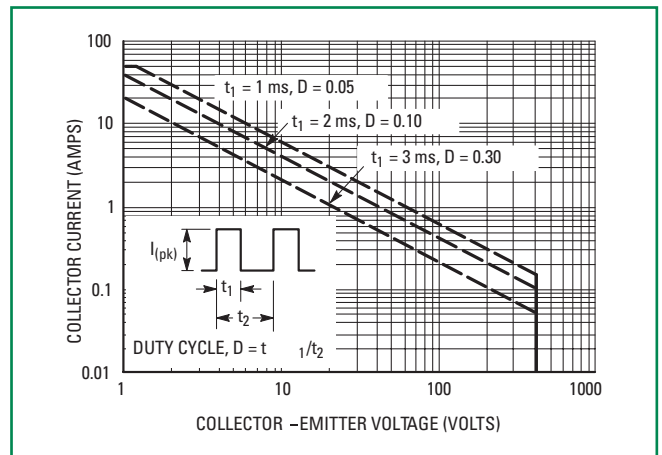
**Figure 16. Single Pulse Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_A = 125^\circ\text{C}$ )



**Figure 17. Pulse Train Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_C = 25^\circ\text{C}$ )

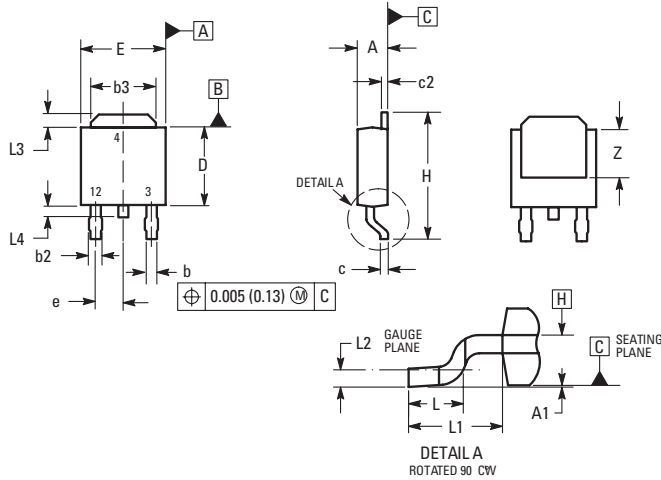


**Figure 18. Pulse Train Safe Operating Area**  
 (Mounted on an Infinite Heatsink at  $T_C = 125^\circ\text{C}$ )





**Dimensions**

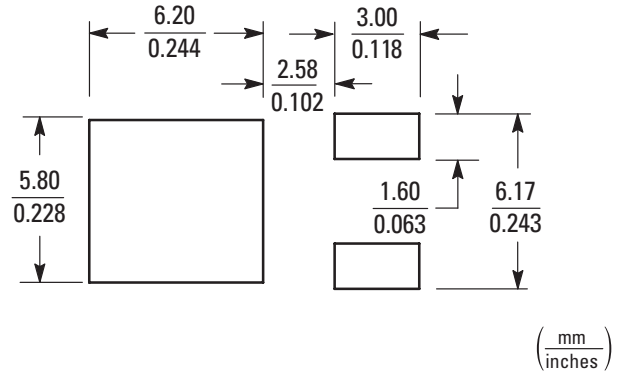


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

**NOTES:**

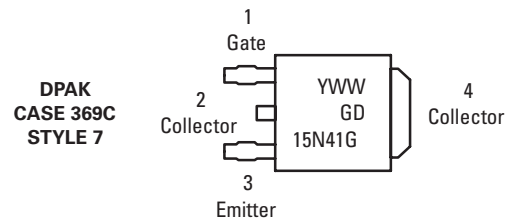
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSION: INCHES. CONTROLLING
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

**Soldering Footprint**

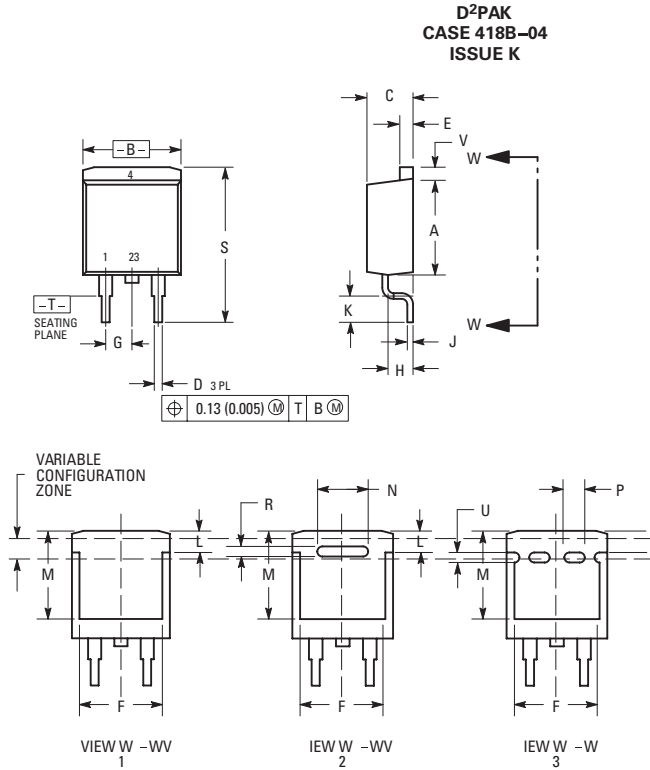


**Part Marking System**

- A= Assembly Location
- Y= Year
- WW = Work Week
- G= Pb -Free Device



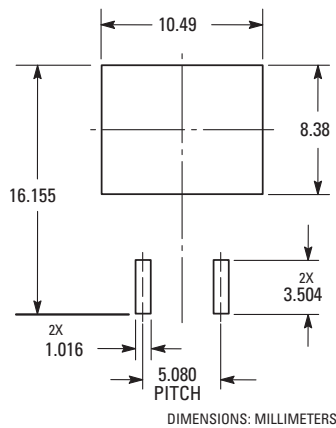
**Dimensions**



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

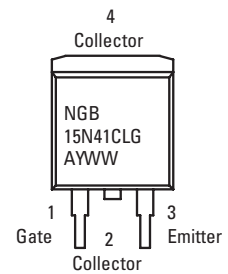
**Soldering Footprint**



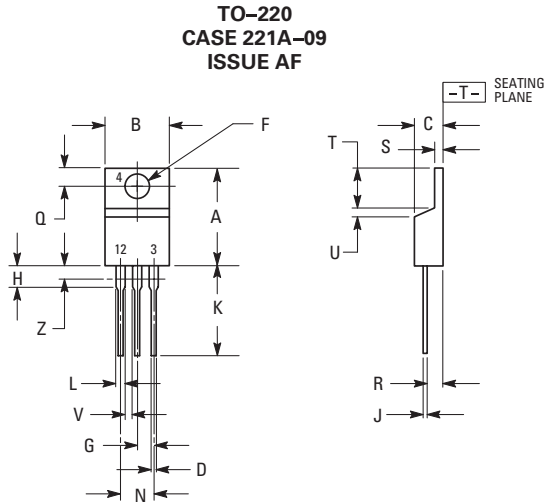
**Part Marking System**

- A= Assembly Location  
Y= Year  
WW = Work Week  
G= Pb -Free Device

**D<sup>2</sup>PAK CASE 418B STYLE 4**



**Dimensions**



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

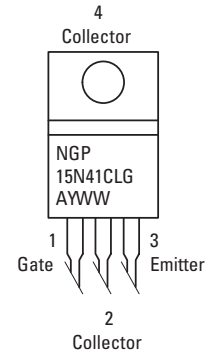
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

**Part Marking System**

A= Assembly Location  
Y= Year  
WW = Work Week  
G= Pb - Free Device

**TO-220AB  
CASE 221A  
STYLE 9**



**ORDERING INFORMATION**

Device	Package	Shipping†
NGD15N41ACL4G	DPAK (Pb-Free)	2500 / Tape & Reel
NGB15N41ACL4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NGP15N41ACLG	TO-220 (Pb-Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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