

NJT4031N, NJV4031NT1G, NJV4031NT3G

Bipolar Power Transistors

NPN Silicon

Features

- Epoxy Meets UL 94, V-0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	40	Vdc
Collector-Base Voltage	V _{CB}	40	Vdc
Emitter-Base Voltage	V _{EB}	6.0	Vdc
Base Current - Continuous	I _B	1.0	Adc
Collector Current - Continuous	I _C	3.0	Adc
Collector Current - Peak	I _{CM}	5.0	Adc
ESD - Human Body Model	HBM	3B	V
ESD - Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Power Dissipation Total P _D @ T _A = 25°C (Note 1) Total P _D @ T _A = 25°C (Note 2)	P _D	2.0 0.80	W
Thermal Resistance, Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R _{θJA} R _{θJA}	64 155	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150	°C

1. Mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material.

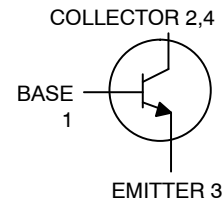
2. Mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material.



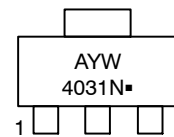
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NPN TRANSISTOR 3.0 AMPERES 40 VOLTS, 2.0 WATTS



MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
4031N = Specific Device Code
■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NJT4031NT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NJV4031NT1G		
NJT4031NT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NJV4031NT3G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NJT4031N, NJV4031NT1G, NJV4031NT3G

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0\text{ A}$)	$V_{CEO(sus)}$	40	–	–	Vdc
Emitter–Base Voltage ($I_E = 50\text{ }\mu\text{A}$, $I_C = 0\text{ A}$)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}$)	I_{EBO}	–	–	100	nAdc

ON CHARACTERISTICS (Note 3)

Collector–Emitter Saturation Voltage ($I_C = 0.5\text{ A}$, $I_B = 5.0\text{ mA}$) ($I_C = 1.0\text{ A}$, $I_B = 10\text{ mA}$) ($I_C = 3.0\text{ A}$, $I_B = 0.3\text{ A}$)	$V_{CE(sat)}$	–	–	0.100 0.150 0.300	Vdc
Base–Emitter Saturation Voltage ($I_C = 1.0\text{ A}$, $I_B = 0.1\text{ A}$)	$V_{BE(sat)}$	–	–	1.0	Vdc
Base–Emitter On Voltage ($I_C = 1.0\text{ A}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	–	–	1.0	Vdc
DC Current Gain ($I_C = 0.5\text{ A}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ A}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 3.0\text{ A}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	220 200 100	– – –	500	

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ob}	–	25	–	pF
Input Capacitance ($V_{EB} = 5.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ib}	–	170	–	pF
Current–Gain – Bandwidth Product (Note 4) ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ V}$, $f_{test} = 1.0\text{ MHz}$)	f_T	–	215	–	MHz

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. $f_T = |h_{FE}| \cdot f_{test}$

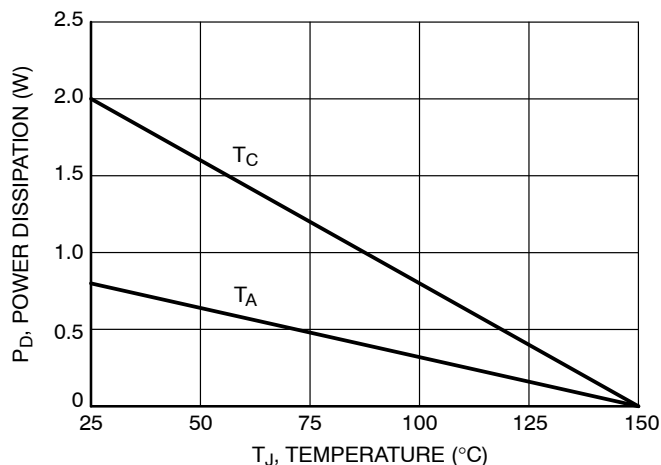


Figure 1. Power Derating

TYPICAL CHARACTERISTICS

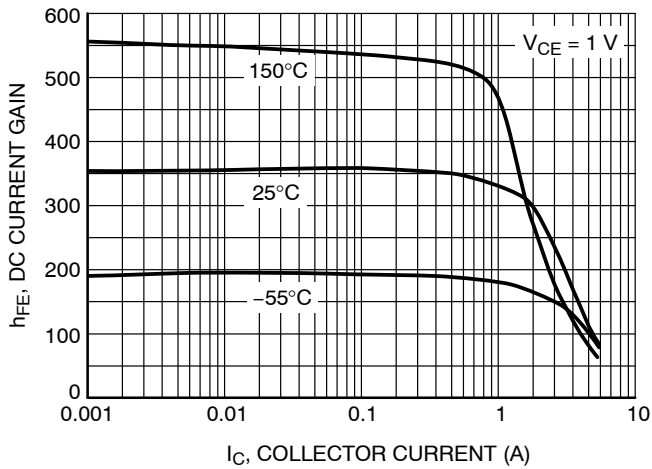


Figure 2. DC Current Gain

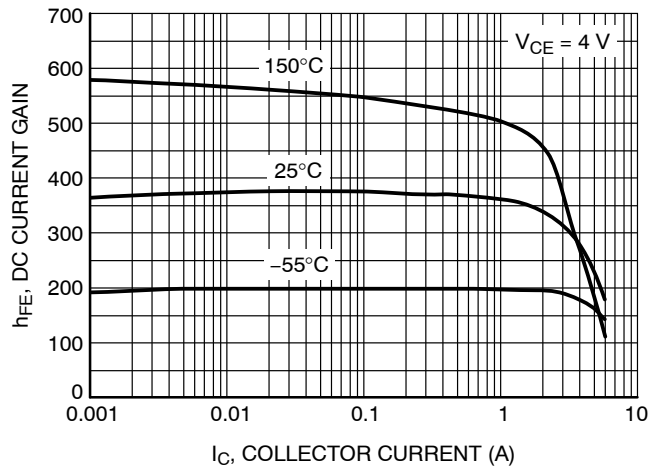


Figure 3. DC Current Gain

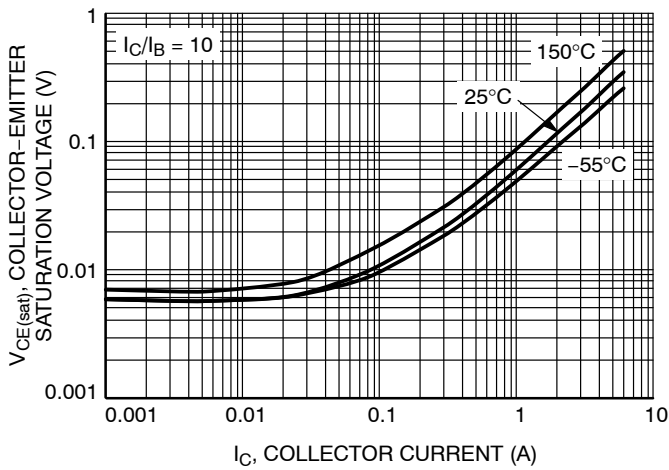


Figure 4. Collector-Emitter Saturation Voltage

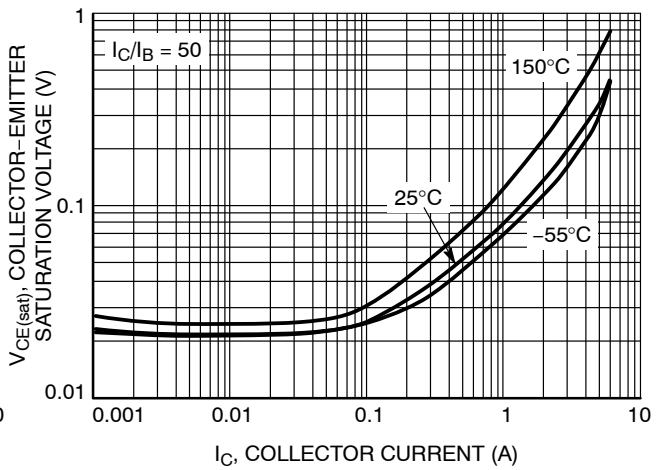


Figure 5. Collector-Emitter Saturation Voltage

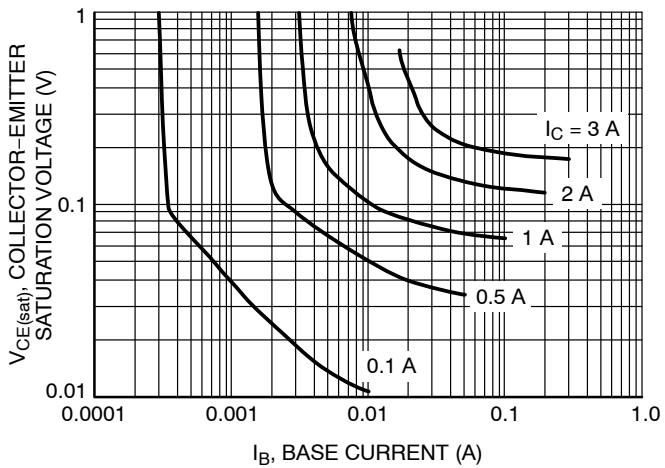


Figure 6. Collector Saturation Region

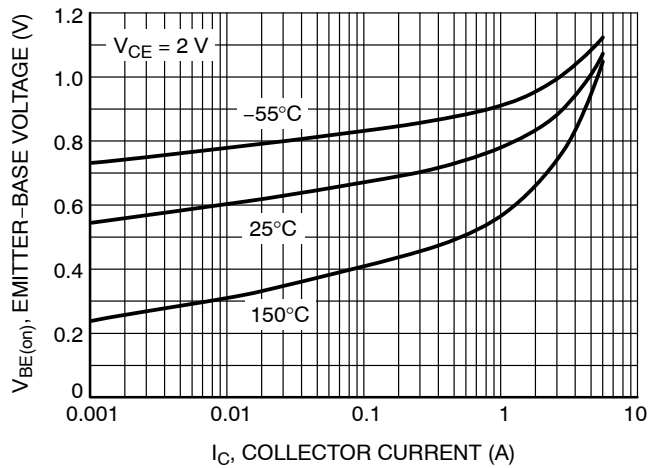


Figure 7. $V_{BE(on)}$ Voltage

TYPICAL CHARACTERISTICS

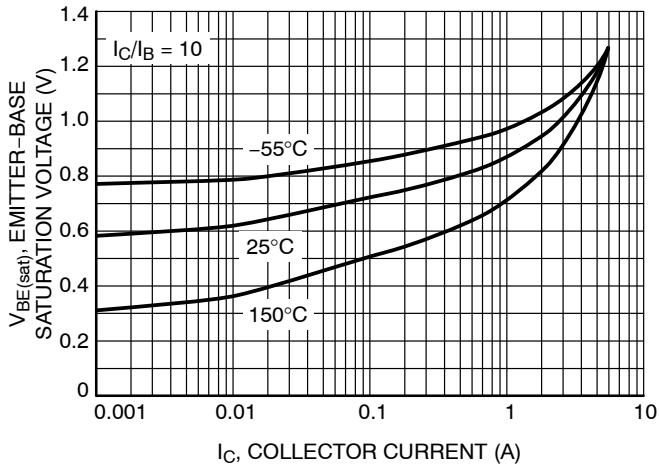


Figure 8. Base-Emitter Saturation Voltage

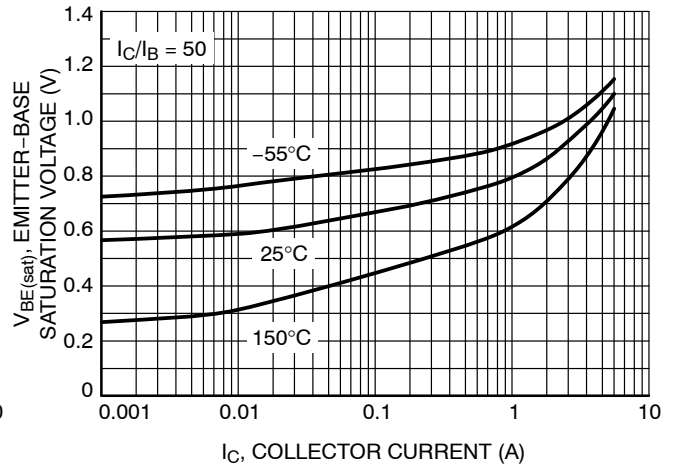


Figure 9. Base-Emitter Saturation Voltage

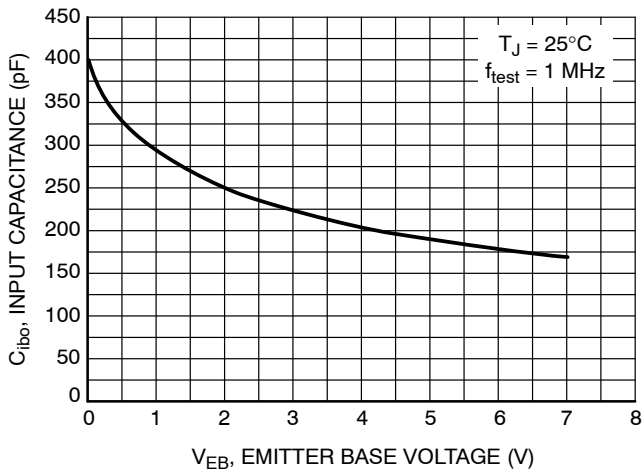


Figure 10. Input Capacitance

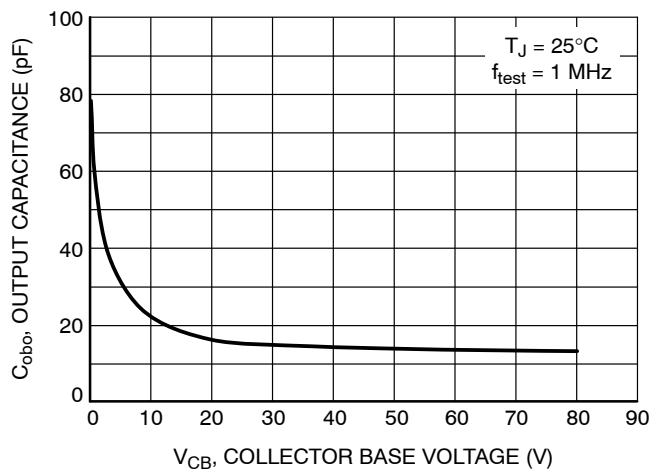


Figure 11. Output Capacitance

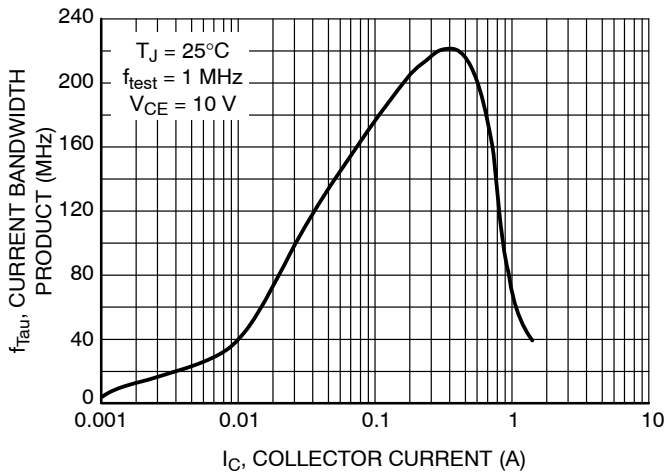


Figure 12. Current-Gain Bandwidth Product

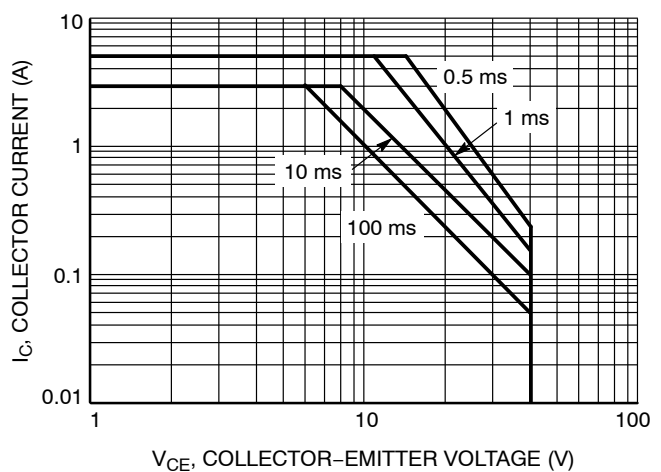


Figure 13. Safe Operating Area

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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