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Buffer with Open Drain Output

NL17SG07MU3TBG

The NL17SG07 is a buffer with open drain output in tiny footprint packages. The device is designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 3.7 ns (Typ) at V_{CC} = 3.0 V, C_L = 15 pF
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Available in UDFN Package
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen−Free/BFR−Free and RoHS−Compliant

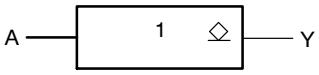

Figure 1. Logic Symbol

PIN ASSIGNMENTS

Pin	UDFN
1	NC
2	A
3	GND
4	Y
5	NC
6	V_{CC}

FUNCTION TABLE

Input	Output
A	**Y**
L	L
H	Z

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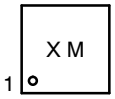
UDFN6
1.0 x 1.0
CASE 517BX

MARKING DIAGRAM

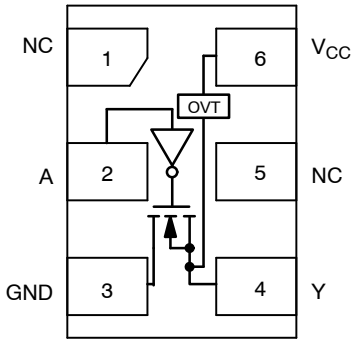


X = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.3	V
V_{IN}	DC Input Voltage		−0.5 to +4.3	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−20	mA
I_{OUT}	DC Output Source/Sink Current		±20	mA
$I_{CC\ or}\ I_{GND}$	DC Supply Current Per Supply Pin or Ground Pin		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		154	°C/W
P_D	Power Dissipation in Still Air		812	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm − by − 1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

Table 1. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		0.9	3.6	V
V_{IN}	Digital Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	Active Mode (High or Low State) Tri−State Mode (Note 1) Power Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate	V_{CC} = 3.3 V ± 0.3 V	0	10	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 2. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		0.9	–	V_{CC}	–	–	–	V
			1.1 to 1.3	$0.7 \times V_{CC}$	–	–	$0.7 \times V_{CC}$	–	
			1.4 to 1.6	$0.65 \times V_{CC}$	–	–	$0.65 \times V_{CC}$	–	
			1.65 to 1.95	$0.65 \times V_{CC}$	–	–	$0.65 \times V_{CC}$	–	
			2.3 to 2.7	1.7	–	–	1.7	–	
			3.0 to 3.6	2.0	–	–	2.0	–	
V_{IL}	Low−Level Input Voltage		0.9	–	GND	–	–	–	V
			1.1 to 1.3	–	–	$0.3 \times V_{CC}$	–	$0.3 \times V_{CC}$	
			1.4 to 1.6	–	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	
			1.65 to 1.95	–	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	
			2.3 to 2.7	–	–	0.7	–	0.7	
			3.0 to 3.6	–	–	0.8	–	0.8	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OL} = 20 μA	0.9	–	0.1	–	–	–	
		I_{OL} = 0.3 mA	1.1 o 1.3	–	–	$0.25 \times V_{CC}$	–	$0.25 \times V_{CC}$	
		I_{OL} = 1.7 mA	1.4 to 1.6	–	–	$0.25 \times V_{CC}$	–	$0.25 \times V_{CC}$	
		I_{OL} = 3.0 mA	1.65 to 1.95	–	–	0.45	–	0.45	
		I_{OL} = 4.0 mA	2.3 to 2.7	–	–	0.4	–	0.4	
		I_{OL} = 8.0 mA	2.7 to 3.6	–	–	0.4	–	0.4	
I_{IN}	Input Leakage Current	V_{IN} = 0 V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 0 V to 3.6 V; V_{OUT} = 0 V to 3.6 V	0	–	–	1.0	–	10.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	0.9 to 3.6	–	–	0.5	–	10.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

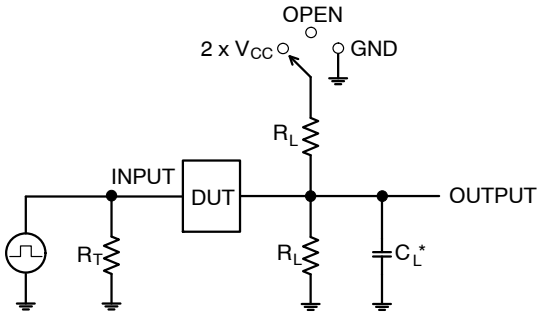
Table 3. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZL}	Propagation Delay A to Y (Figures 3 and 4)	C_L = 10 pF;							ns
		R_L = 100 kΩ	0.9	–	31.6	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	8.2	12.7	–	13.0	
		R_L = 5 kΩ	1.4 to 1.6	–	4.3	5.7	–	7.3	
		R_L = 5 kΩ	1.65 to 1.95	–	3.4	4.5	–	5.9	
		R_L = 5 kΩ	2.3 to 2.7	–	2.2	3.3	–	4.5	
		R_L = 5 kΩ	3.0 to 3.6	–	1.7	2.9	–	3.7	
		C_L = 15 pF;							
		R_L = 100 kΩ	0.9	–	32.5	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	8.5	13.0	–	13.5	
		R_L = 5 kΩ	1.4 to 1.6	–	4.5	6.0	–	7.9	
		R_L = 5 kΩ	1.65 to 1.95	–	3.6	4.5	–	6.2	
		R_L = 5 kΩ	2.3 to 2.7	–	2.3	3.4	–	4.6	
		R_L = 5 kΩ	3.0 to 3.6	–	1.8	3.0	–	3.7	
		C_L = 30 pF;							
		R_L = 100 kΩ	0.9	–	35.2	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	9.3	14.0	–	14.2	
		R_L = 5 kΩ	1.4 to 1.6	–	5.1	6.2	–	8.5	
		R_L = 5 kΩ	1.65 to 1.95	–	4.0	4.9	–	6.4	
		R_L = 5 kΩ	2.3 to 2.7	–	2.6	3.6	–	4.7	
		R_L = 5 kΩ	3.0 to 3.6	–	2.1	3.1	–	3.9	
t_{PLZ}	Propagation Delay, A to Y (Figures 3 and 4)	C_L = 10 pF;							ns
		R_L = 100 kΩ	0.9	–	14.9	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	7.2	10.9	–	11.5	
		R_L = 5 kΩ	1.4 to 1.6	–	5.1	7.2	–	8.3	
		R_L = 5 kΩ	1.65 to 1.95	–	4.8	7.0	–	7.8	
		R_L = 5 kΩ	2.3 to 2.7	–	4.2	6.5	–	7.3	
		R_L = 5 kΩ	3.0 to 3.6	–	3.8	6.2	–	6.8	
		C_L = 15 pF;							
		R_L = 100 kΩ	0.9	–	16.2	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	8.5	13.4	–	14.0	
		R_L = 5 kΩ	1.4 to 1.6	–	6.4	10.0	–	10.8	
		R_L = 5 kΩ	1.65 to 1.95	–	6.1	9.5	–	10.5	
		R_L = 5 kΩ	2.3 to 2.7	–	5.5	7.8	–	10.0	
		R_L = 5 kΩ	3.0 to 3.6	–	5.2	7.2	–	9.3	
		C_L = 30 pF;							
		R_L = 100 kΩ	0.9	–	20.1	–	–	–	
		R_L = 5 kΩ	1.1 to 1.3	–	12.4	18.4	–	20.0	
		R_L = 5 kΩ	1.4 to 1.6	–	10.2	15.0	–	16.0	
		R_L = 5 kΩ	1.65 to 1.95	–	9.9	14.5	–	15.8	
		R_L = 5 kΩ	2.3 to 2.7	–	9.4	13.5	–	15.4	
		R_L = 5 kΩ	3.0 to 3.6	–	9.0	13.2	–	14.3	

Table 4. CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T_A = 25°C)	Unit
C_{IN}	Input Capacitance	V_{CC} = 0 V	3.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 0 V	3.0	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, V_{CC} = 0.9 V to 3.6 V, V_{IN} = 0 V or V_{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_{in} + I_{CC} \times V_{CC}$.



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 2. Test Circuit

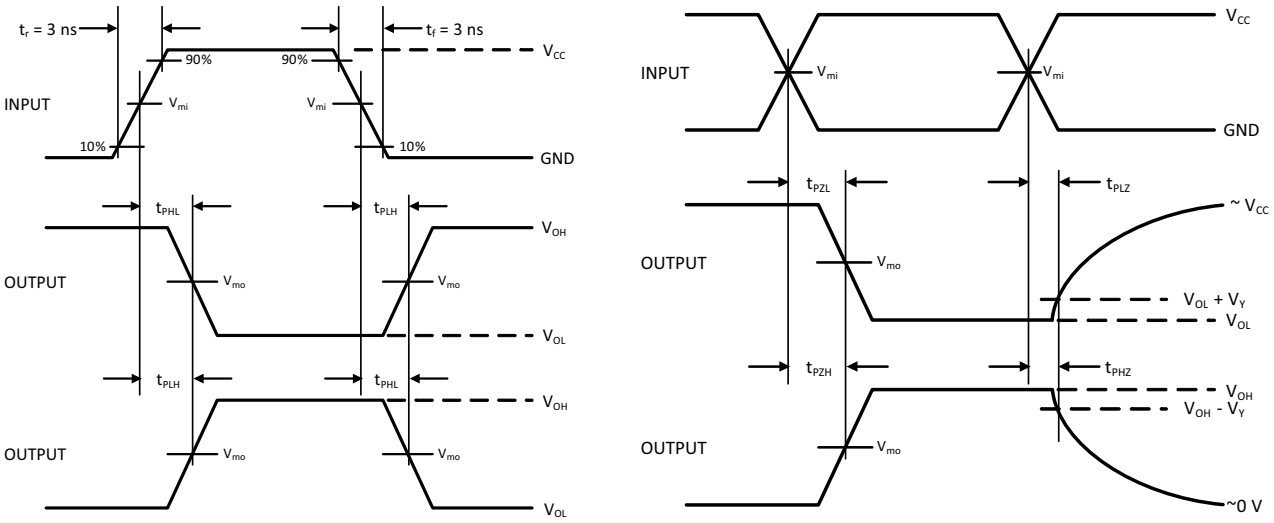


Figure 3. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	$V_{CC}/2$	$V_{CC}/2$	0.1
1.1 to 1.3	$V_{CC}/2$	$V_{CC}/2$	0.1
1.4 to 1.6	$V_{CC}/2$	$V_{CC}/2$	0.1
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	1.5	1.5	0.3

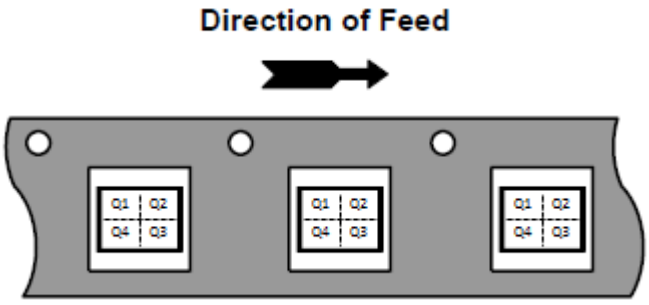
ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NL17SG07MU3TBG	UDFN6, 1.0 x 1.0, 0.35P	J	Q2	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC – Q100 Qualified and PPAP Capable.

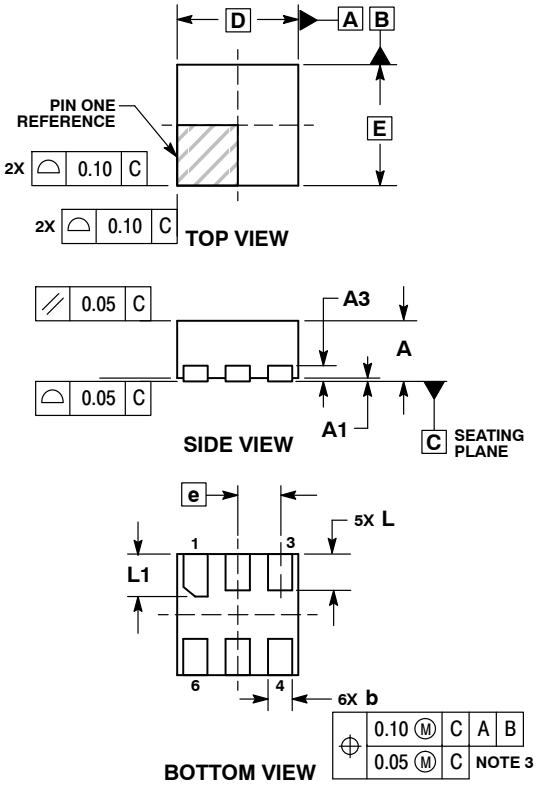
Pin 1 Orientation in Tape and Reel



NL17SG07MU3TBG

PACKAGE DIMENSIONS

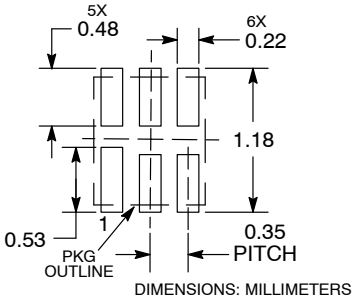
UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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