

NLAS4157

Analog Switch, SPDT, 1 Ω R_{ON}

The NLAS4157 is a low R_{ON} SPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS4157 can handle a balanced microphone/speaker/ringtone generator in a monophone mode. The device contains a break-before-make (BBM) feature.

Features

- Single Supply Operation:
1.65 V to 5.5 V V_{CC}
Function Directly from LiON Battery
- Tiny SC88 6-Pin Pb-Free Package:
Meets JEDEC MO-220 Specifications
- R_{ON} Typical = 0.8 Ω @ V_{CC} = 4.5 V
- Low Static Power
- This is a Pb-Free Device

Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Stereo Balanced (Push-Pull) Switching

Important Information

- Ringtone-Chip/Amplifier Switching
- Continuous Current Rating Through each Switch ± 300 mA
- Conforms to: JEDEC MO-220, Issue H, Variation VEED-6
- Pin for Pin Compatible with FSA4157



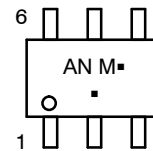
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<http://onsemi.com>



SC-88 (SOT-363)
CASE 419B

MARKING DIAGRAM

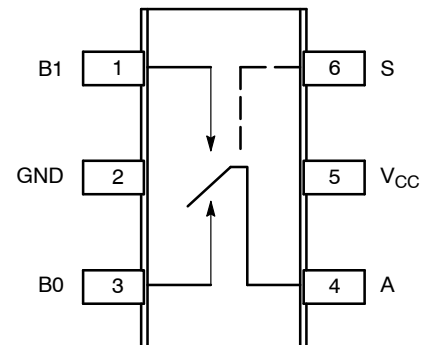


AN = Specific Device Code
M = Date Code*
G = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NLAS4157

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		2.7 4.5				2.0 2.4		V
V _{IL}	LOW Level Input Voltage		2.7 4.5					0.6 0.8	V
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0-5.5			±0.1		±1	μA
I _{OFF}	OFF State Leakage Current (Note 7)	0 ≤ A, B ≤ V _{CC}	5.5	-2.0		+2.0		±20	nA
I _{ON}	ON State Leakage Current (Note 7)	0 ≤ A, B ≤ V _{CC}	5.5	-4.0		+4.0		±40	nA
R _{ON}	Switch On Resistance (Note 2)	I _O = -100 mA, B ₀ or B ₁ = 3.5 V	2.7		2.0	4.0		4.3	Ω
		I _O = -100 mA, B ₀ or B ₁ = 1.5 V	4.5		0.8	1.15		1.3	
I _{CC}	Quiescent Supply Current All Channels ON or OFF	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5			0.5		1.0	μA

Analog Signal Range

ΔR _{ON}	On Resistance Match Between Channels (Notes 2, 3, 4)	I _A = -100 mA, B ₀ or B ₁ = 1.5 V	2.7		0.15				Ω
		I _A = -100 mA, B ₀ or B ₁ = 3.5 V	4.5		0.12			0.15	
R _{flat}	On Resistance Flatness (Notes 2, 3, 5)	I _A = -100 mA, B ₀ or B ₁ = 0 V, 0.75 V, 1.5 V	2.7		1.4				Ω
		I _A = -100 mA, B ₀ or B ₁ = 0 V, 1.0 V, 2.0 V	4.5		0.3			0.4	

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
3. Parameter is characterized but not tested in production.
4. ΔR_{ON} = R_{ON} max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
5. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
6. Guaranteed by Design.
7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Unit	Figure #
				Min	Typ	Max	Min	Max		
t _{PHL} t _{PLH}	Propagation Delay Bus-to-Bus (Note 9)	V _I = OPEN	2.7 4.5			2.0 0.3			ns	3, 4
t _{ON}	Output Enable Time Turn On Time (A to B _n)	B ₀ or B ₁ = 1.5 V, R _L = 50 Ω, C _L = 35 pF B ₀ or B ₁ = 3.0 V, R _L = 50 Ω, C _L = 35 pF	2.7 4.5			30 20		35 25	ns	3, 4
t _{OFF}	Output Disable Time Turn Off Time (A Port to B Port)	B ₀ or B ₁ = 1.5V, R _L = 50 Ω, C _L = 35 pF B ₀ or B ₁ = 3.0 V, R _L = 50 Ω, C _L = 35 pF	2.7 4.5			20 15		25 20	ns	3, 4
t _{BBM}	Break Before Make Time (Note 8)		2.7 4.5	0.5 0.5			0.5 0.5		ns	2
Q	Charge Injection (Note 8)	C _L = 1.0 nF, V _{GEN} = 0 V R _{GEN} = 0 Ω	2.7 4.5		26 48				pC	6
O _{IRR}	Off Isolation (Note 10)	R _L = 50 Ω f = 1.0 MHz	2.7 – 5.5		-52				dB	5
X _{talk}	Crosstalk	R _L = 50 Ω f = 1.0 MHz	2.7 – 5.5		-57				dB	7
BW	-3 dB Bandwidth	R _L = 50 Ω	2.7 – 5.5		40				MHz	8
THD	Total Harmonic Distortion (Note 8)	R _L = 600 Ω 0.5 V _{P-P} f = 20 Hz to 20 kHz	2.7 – 5.5		0.012				%	9

8. Guaranteed by Design.

9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

10. Off Isolation = 20 log₁₀ [V_A/V_{Bn}].

CAPACITANCE (Note 11)

Symbol	Parameter	Test Conditions	Typ	Max	Unit	Figure #
C _{IN}	Select Pin Input Capacitance	V _{CC} = 0 V, f = 1 MHz	10		pF	
C _{IO-B}	B Port Off Capacitance	V _{CC} = 4.5 V, f = 1 MHz	25		pF	
C _{IOA-ON}	A Port Capacitance when Switch is Enabled	V _{CC} = 4.5 V, f = 1 MHz	87		pF	

11. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

DEVICE ORDERING INFORMATION

Device Order Number	Package	Shipping [†]
NLAS4157DFT2G	SC-88 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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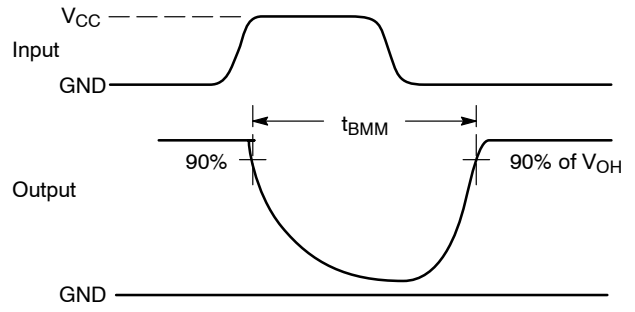
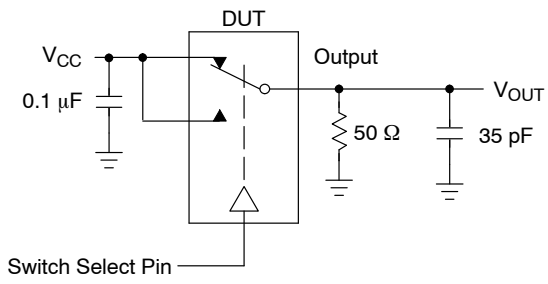


Figure 2. t_{BMM} (Time Break-Before-Make)

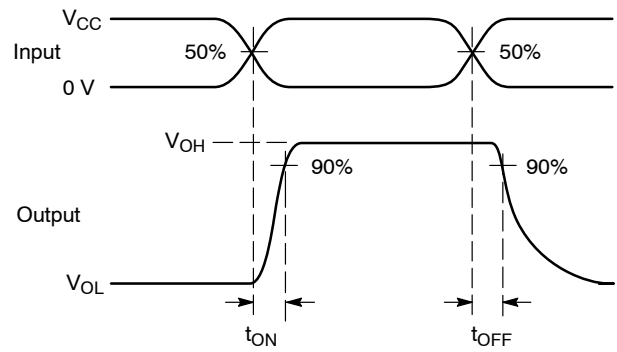
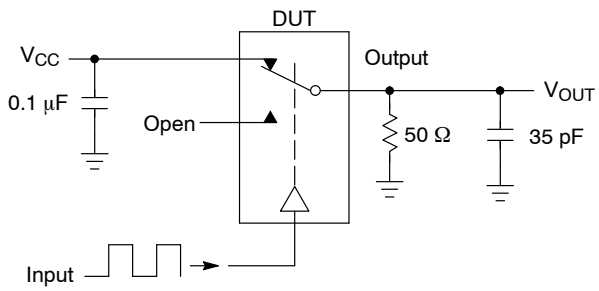


Figure 3. t_{ON}/t_{OFF}

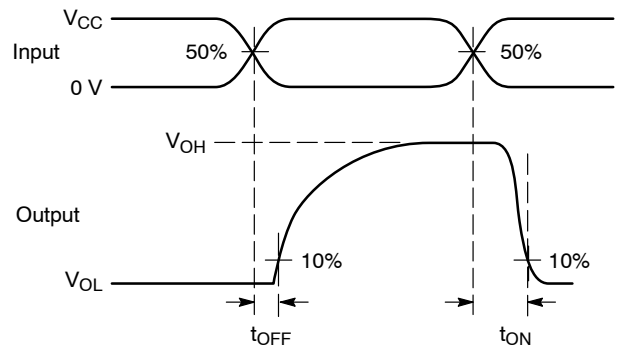
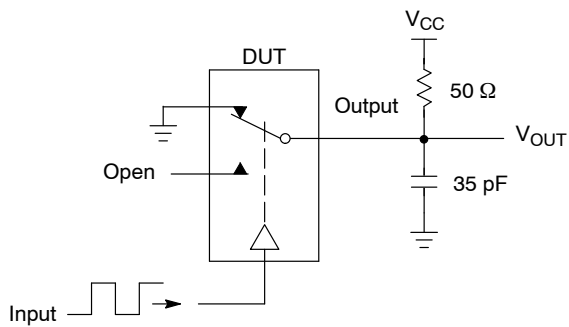
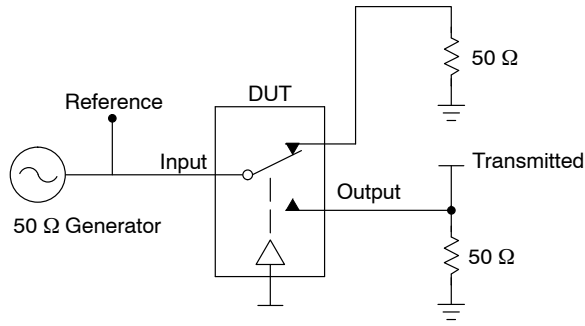


Figure 4. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

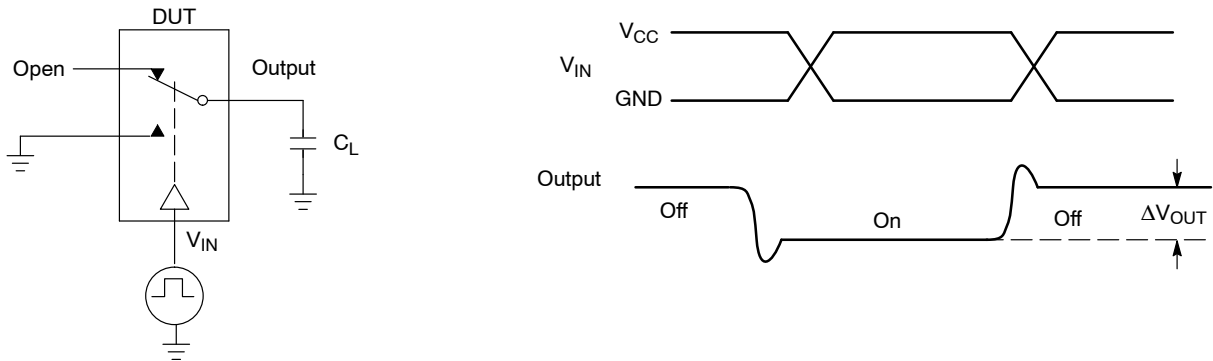


Figure 6. Charge Injection: (Q)

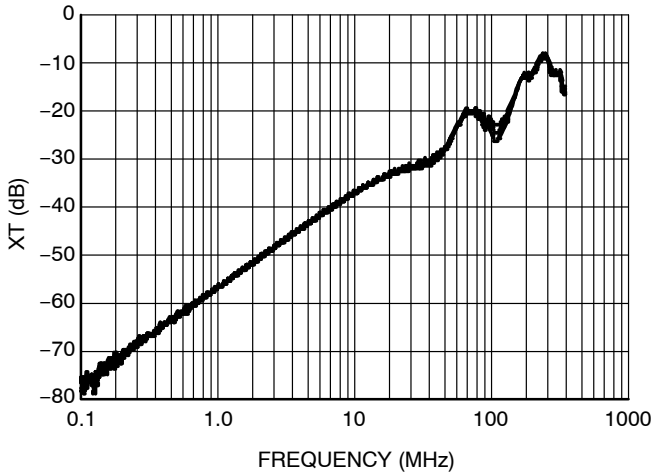


Figure 7. Cross Talk vs. Frequency
@ $V_{CC} = 4.5\text{ V}$

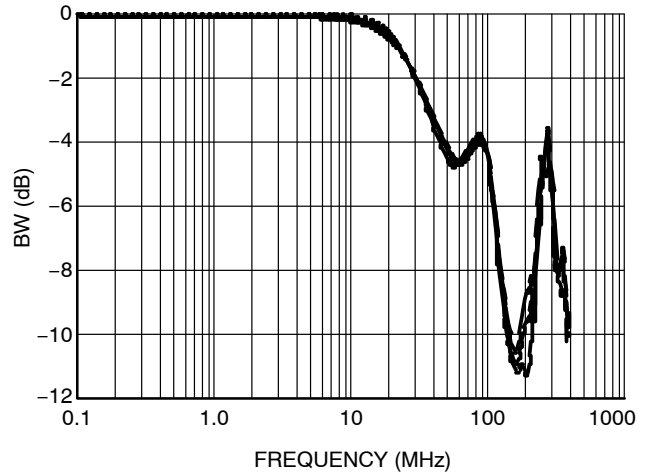


Figure 8. Bandwidth vs. Frequency

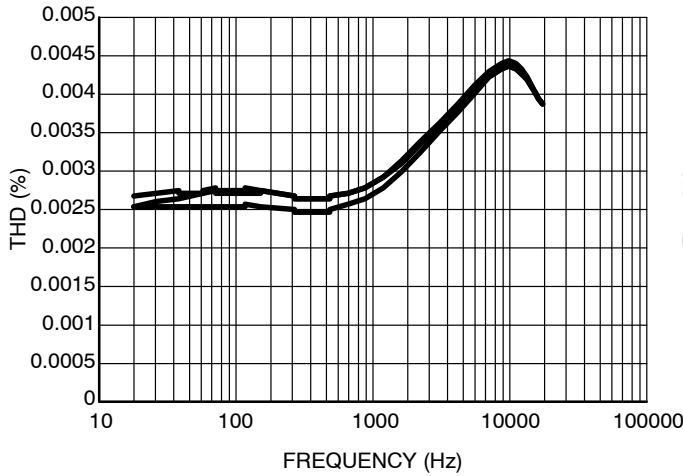


Figure 9. Total Harmonic Distortion

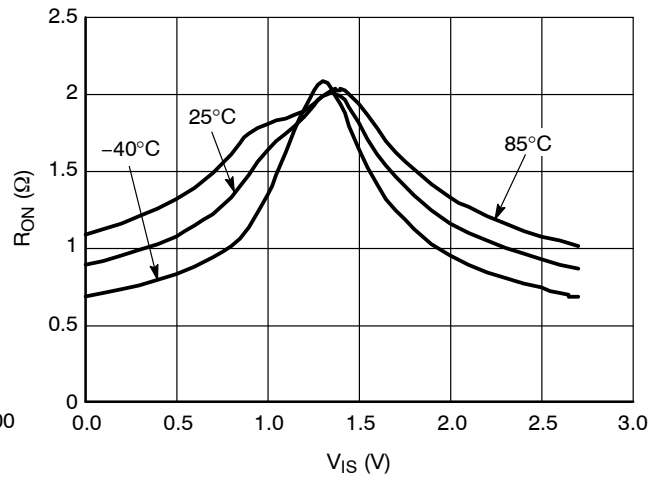


Figure 10. On-Resistance vs. Signal Voltage
@ $V_{CC} = 2.7\text{ V}$

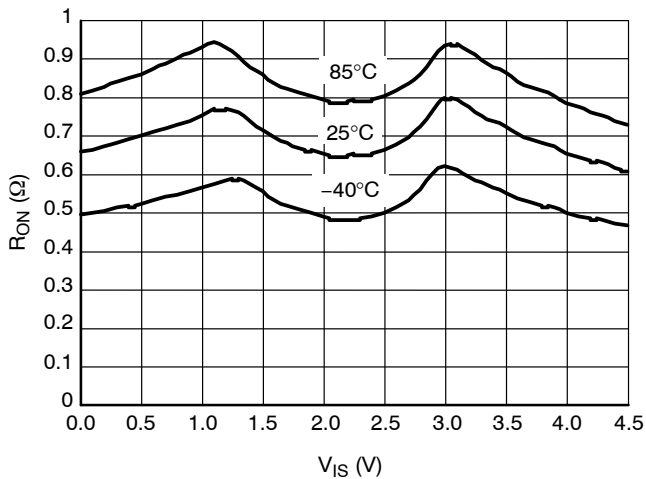


Figure 11. On-Resistance vs. Signal Voltage
@ $V_{CC} = 4.5\text{ V}$

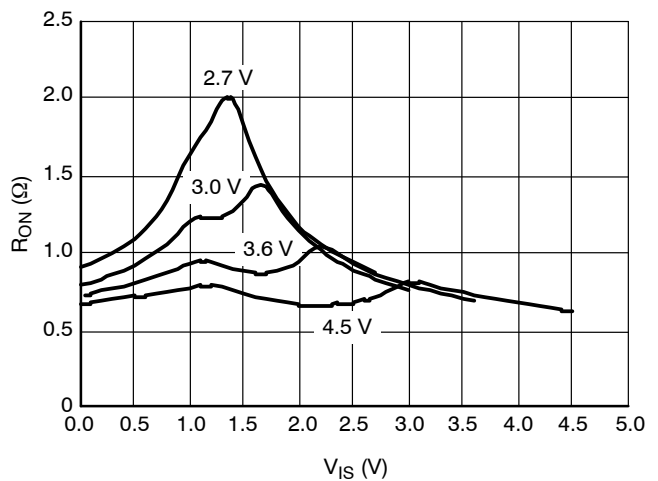


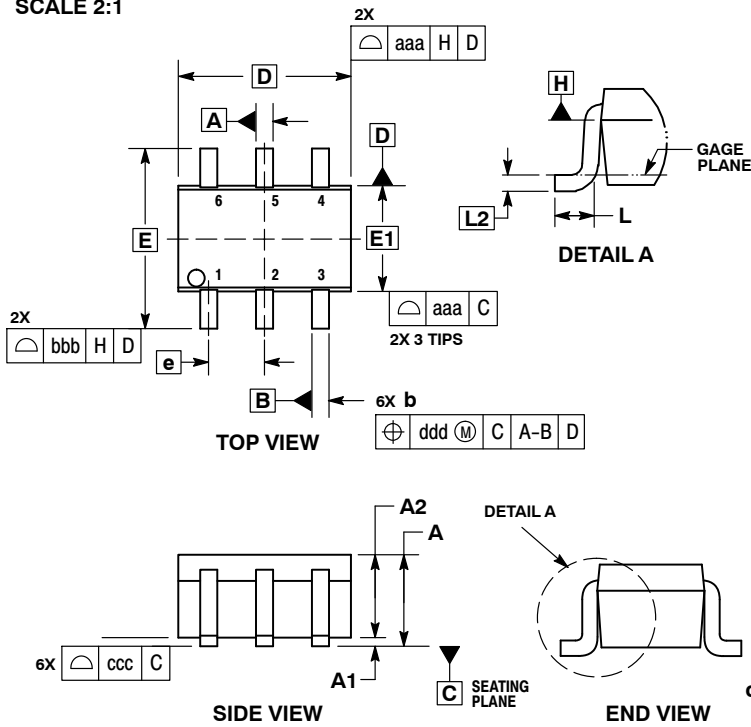
Figure 12. On-Resistance vs. Signal Voltage



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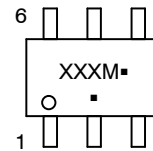
1
SCALE 2:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



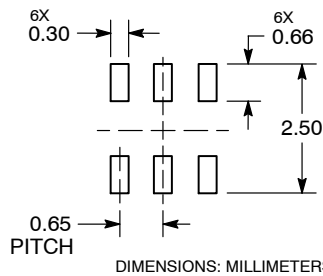
- XXX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (j) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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