## NLAS5123

## SPDT, $1 \mathbf{\Omega}$ Ron Switch

The NLAS5123 is a low $\mathrm{R}_{\text {ON }}$ SPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS5123 can handle a balanced microphone/ speaker/ringtone generator in a monophone mode. The device contains a break-before-make (BBM) feature.

## Features

- Single Supply Operation:

$$
1.65 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}
$$

- Function Directly from LiON Battery
- $\mathrm{R}_{\mathrm{ON}}$ Typical $=1.0 \Omega @ \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}$
- Low Static Power
- These are $\mathrm{Pb}-$ Free Devices


## Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Stereo Balanced (Push-Pull) Switching


## Important Information

- Continuous Current Rating Through each Switch $\pm 300 \mathrm{~mA}$
- $1.2 \times 1.0 \times 0.4 \mathrm{P}$ mm 6-Lead Thin DFN Package


PIN ASSIGNMENTS

(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.


Figure 1. Input Equivalent Circuit

## PIN DESCRIPTION

| Pin Name | Description |
| :---: | :---: |
| NC, NO, COM | Data Ports |
| IN | Control Input |

## TRUTH TABLE

| Control Input | Function |
| :---: | :---: |
| L | NC Connected to COM |
| H | NO Connected to COM |

H = HIGH Logic Level.
L = LOW Logic Level.

## MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Positive DC Supply Voltage | -0.5 to +6.0 | V |
| $\mathrm{~V}_{\mathrm{IS}}$ | Analog Input Voltage $\left(\mathrm{V}_{\mathrm{NO}}, \mathrm{V}_{\mathrm{NC}}\right.$, or $\left.\mathrm{V}_{\mathrm{COM}}\right)$ | -0.5 to $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{~V}_{\mathrm{IN}}$ | Digital Select Input Voltage | -0.5 to +6.0 | V |
| $\mathrm{I}_{\text {anl1 }}$ | Continuous DC Current from COM to NC/NO | $\pm 300$ | mA |
| $\mathrm{I}_{\text {anl-pk1 }}$ | Peak Current from COM to NC/NO, 10 Duty Cycles (Note 1$)$ | $\pm 500$ | mA |
| $\mathrm{I}_{\mathrm{clmp}}$ | Continuous DC Current into COM/NC/NO with respect to $\mathrm{V}_{\mathrm{CC}}$ or GND | $\pm 100$ | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Defined as $10 \% \mathrm{ON}, 90 \%$ off duty cycle.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Rating | Min | Max | Unit |
| :--- | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Positive DC Supply Voltage | 1.65 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{IS}}$ | Analog Input Voltage (NC, NO, COM) | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{V}_{\mathrm{IN}}$ | Digital Select Input Voltage (IN) | 0 | $\mathrm{~V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature Range |  | -40 | 85 |
| ${ }^{\circ} \mathrm{C}$ |  |  |  |  |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise or Fall Time, SELECT | $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ |  | 20 |
|  |  | $\mathrm{~V}=5.5 \mathrm{~V}$ |  | 10 |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $\mathrm{V}_{\mathrm{cc}}$ <br> (V) | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Max |  |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH Level Input Voltage |  | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ |  |  |  | $\begin{aligned} & 2.0 \\ & 2.4 \end{aligned}$ |  | V |
| $\mathrm{V}_{\text {IL }}$ | LOW Level Input Voltage |  | $\begin{aligned} & \hline 2.7 \\ & 4.5 \end{aligned}$ |  |  |  |  | $\begin{aligned} & 0.6 \\ & 0.8 \end{aligned}$ | V |
| $\mathrm{I}_{\mathrm{N}}$ | Input Leakage Current | $0 \leq \mathrm{V}_{\mathrm{IN}} \leq 5.5 \mathrm{~V}$ | 0-5.5 |  |  | $\pm 0.1$ |  | $\pm 1$ | $\mu \mathrm{A}$ |
| IofF | OFF State Leakage Current (Note 7) | $0 \leq \mathrm{NO}, \mathrm{NC}, \mathrm{COM} \leq \mathrm{V}_{\mathrm{CC}}$ | 5.5 | -2.0 |  | +2.0 |  | $\pm 20$ | nA |
| I ON | ON State Leakage Current (Note 7) | $0 \leq \mathrm{NO}, \mathrm{NC}, \mathrm{COM} \leq \mathrm{V}_{\mathrm{CC}}$ | 5.5 | -4.0 |  | +4.0 |  | $\pm 40$ | nA |
| $\mathrm{R}_{\text {ON }}$ | Switch On Resistance (Note 2) | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \\ & \mathrm{~V}_{\mathrm{IS}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}} \end{aligned}$ | 2.7 |  |  | 1.7 |  | 2.0 | $\Omega$ |
|  |  | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \\ & \mathrm{~V}_{\mathrm{IS}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}} \end{aligned}$ | 4.5 |  |  | 1.0 |  | 1.2 |  |
| ${ }^{\text {ICC }}$ | Quiescent Supply Current All Channels ON or OFF | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {CC }}$ or GND, $\mathrm{I}_{\text {OUT }}=0$ | 5.5 |  |  | 0.5 |  | 1.0 | $\mu \mathrm{A}$ |

Analog Signal Range

| $\Delta R_{\mathrm{ON}}$ | On Resistance Match <br> Between Channels <br> (Notes 2, 3, 4) | $\mathrm{I}_{\mathrm{A}}=100 \mathrm{~mA}$, <br> $\mathrm{V}_{\mathrm{IS}}=1.5 \mathrm{~V}$ <br> $\mathrm{I}_{\mathrm{A}}=100 \mathrm{~mA}$, <br> $\mathrm{V}_{\mathrm{IS}}=2.5 \mathrm{~V}$ | 2.7 | 0.15 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |

2. Measured by the voltage drop between NC/NO and COM pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (NO, NC, COM).
3. Parameter is characterized but not tested in production.
4. $\Delta R_{O N}=R_{O N} \max -R_{O N}$ min measured at identical $\mathrm{V}_{\mathrm{CC}}$, temperature and voltage levels.
5. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
6. Guaranteed by Design.
7. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} \\ & \text { (V) } \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Unit | Figure \# |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max | Min | Max |  |  |
| $\begin{array}{\|l\|l} \hline \mathrm{t}_{\mathrm{PHL}} \\ \mathrm{t}_{\mathrm{PLH}} \end{array}$ | Propagation Delay Bus-to-Bus (Note 9) | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}}$ or $\mathrm{V}_{\mathrm{IL}}$ | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ |  |  | $\begin{aligned} & 2.0 \\ & 0.3 \end{aligned}$ |  |  | ns |  |
| ton | Output Enable Time <br> Turn On Time <br> (COM to NO or NC) | $\begin{aligned} & \mathrm{V}_{\mathrm{IS}}=1.5 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \\ & \mathrm{~V}_{\text {IS }}=3.0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ |  |  | $\begin{aligned} & 30 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & 35 \\ & 25 \end{aligned}$ | ns | 3, 4 |
| tofF | Output Disable Time Turn Off Time (COM to NO, NC) | $\begin{aligned} & \mathrm{V}_{\mathrm{IS}}=1.5 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \\ & \mathrm{~V}_{\text {IS }}=3.0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ |  |  | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 20 \end{aligned}$ | ns | 3, 4 |
| $\mathrm{t}_{\text {BBM }}$ | Break Before Make Time (Note 8) | $\begin{aligned} & \mathrm{V}_{\mathrm{IS}}=1.5 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 0.5 \end{aligned}$ |  |  | $\begin{aligned} & 0.5 \\ & 0.5 \end{aligned}$ |  | ns | 2 |
| Q | Charge Injection (Note 8) | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{~V}_{\mathrm{GEN}}=0 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{GEN}}=0 \Omega \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 4.5 \end{aligned}$ |  | $\begin{aligned} & 26 \\ & 48 \end{aligned}$ |  |  |  | pC | 6 |
| $\mathrm{O}_{\text {IRR }}$ | Off Isolation (Note 10) | $\begin{aligned} & R_{L}=50 \Omega \\ & \mathrm{f}=1.0 \mathrm{MHz} \end{aligned}$ | $\begin{gathered} \hline 2.7- \\ 5.5 \end{gathered}$ |  | -62 |  |  |  | dB | 5 |
| $\mathrm{X}_{\text {talk }}$ | Crosstalk | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega \\ & \mathrm{f}=1.0 \mathrm{MHz} \end{aligned}$ | $\begin{gathered} \hline 2.7- \\ 5.5 \end{gathered}$ |  | -70 |  |  |  | dB | 7 |
| BW | -3 dB Bandwidth | $\mathrm{R}_{\mathrm{L}}=50 \Omega$ | $\begin{gathered} 2.7- \\ 5.5 \end{gathered}$ |  | 55 |  |  |  | MHz | 8 |
| THD | Total Harmonic Distortion (Note 8) | $\begin{aligned} & \hline \mathrm{R}_{\mathrm{L}}=600 \Omega \\ & 0.5 \mathrm{~V}_{\mathrm{P}-\mathrm{P}} \\ & \mathrm{f}=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz} \end{aligned}$ | $\begin{gathered} 2.7- \\ 5.5 \end{gathered}$ |  | 0.012 |  |  |  | \% | 9 |

8. Guaranteed by Design.
9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
10. Off Isolation $=20 \log _{10}\left[\mathrm{~V}_{\mathrm{COM}} / \mathrm{V}_{\mathrm{NO}, \mathrm{NCC}}\right]$.

CAPACITANCE (Note 11)

| Symbol | Parameter | Test Conditions | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{C}_{\mathrm{IN}}$ | Select Pin Input Capacitance | $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ | 2.0 |  | pF |
| $\mathrm{C}_{\mathrm{NC} / \mathrm{NO}}$ | NC, NO Port Off Capacitance | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ | 20 |  | pF |
| $\mathrm{C}_{\mathrm{COM}}$ | COM Port Capacitance when Switch is Enabled | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ | 55 |  | pF |

11. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{MHz}$, Capacitance is characterized but not tested in production.


Figure 2. $\mathrm{t}_{\mathrm{BB}}$ (Time Break-Before-Make)


Figure 3. $\mathrm{t}_{\mathrm{ON}} / \mathrm{t}_{\mathrm{OFF}}$


Figure 4. $\mathrm{t}_{\mathrm{ON}} / \mathrm{t}_{\mathrm{OFF}}$


Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $\mathrm{V}_{\text {ISO }}$, Bandwidth and $\mathrm{V}_{\text {ONL }}$ are independent of the input signal direction.
$\mathrm{V}_{\text {ISO }}=$ Off Channel Isolation $=20 \log \left(\frac{\mathrm{VOUT}}{\mathrm{V}_{\text {IN }}}\right)$ for $\mathrm{V}_{\text {IN }}$ at 100 kHz
$\mathrm{V}_{\mathrm{ONL}}=$ On Channel Loss $=20 \log \left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{V}_{\text {IN }}}\right)$ for $\mathrm{V}_{\text {IN }}$ at 100 kHz to 50 MHz
Bandwidth (BW) = the frequency 3 dB below $\mathrm{V}_{\mathrm{ONL}}$
$\mathrm{V}_{\mathrm{CT}}=$ Use $\mathrm{V}_{\text {ISO }}$ setup and test to all other switch analog input/outputs terminated with $50 \Omega$

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ $V_{\text {ONL }}$


Output


Figure 6. Charge Injection: (Q)


Figure 7. Cross Talk vs. Frequency @ $\mathrm{V}_{\mathrm{cc}}=4.5 \mathrm{~V}$


Figure 9. Total Harmonic Distortion


Figure 8. Bandwidth vs. Frequency


Figure 10. On-Resistance vs. Input Voltage @ $\mathrm{V}_{\mathrm{Cc}}=2.7 \mathrm{~V}$


Figure 11. On-Resistance vs. Input Voltage @ $\mathrm{V}_{\mathrm{cc}}=4.5 \mathrm{~V}$


Figure 12. On-Resistance vs. Input Voltage

## DEVICE ORDERING INFORMATION

| Device Order Number | Device Nomenclature |  |  |  |  | Package Type | Tape \& Reel Size ${ }^{\dagger}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Circuit Indicator | Technology | Device Function | Package Suffix | Tape \& Reel Suffix |  |  |
| NLAS5123MNR2G | NL | AS | 5123 | MN | 2 | WDFN6 ( $\mathrm{Pb}-\mathrm{Free}$ ) | 3000 / Tape \& Reel |
| NLAS5123MUR2G | NL | AS | 5123 | MU | 2 | UDFN6 (Pb-Free) | 3000 / Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb -Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | WDFN6, 1.2 X1.0, 0.4 P | PAGE 1 OF 1 |

[^0]
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| ---: | :--- | :--- | :--- |
| DESCRIPTION: | 6 PIN UDFN, 1.2X1.0, 0.4P | PAGE 1 OF 1 |

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