# Dual 2-Bit Dual-Supply Non-Inverting Level Translator

The NLSV22T244 is a dual 2-bit configurable dual-supply bus buffer level translator. The input ports A and the output ports B are designed to track two different power supply rails  $V_{CCA}$  and  $V_{CCB}$ . Both supply rails are configurable from 1.6 V to 3.6 V allowing universal low-voltage translations from the input port A to the output B port.

#### **Features**

- Wide V<sub>CCA</sub> and V<sub>CCB</sub> Operating Range: 1.6 V to 3.6 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 5.5 V
- Non-preferential V<sub>CCA</sub> and V<sub>CCB</sub> Sequencing
- Outputs at 3-State until Active V<sub>CC</sub> is reached
- Power-Off Protection
- Ultra-Small packaging: 1.7mm x 2.0 mm UQFN-12
- This is a Pb-Free Device

#### **Typical Applications**

• Mobile Phones, PDAs, Other Portable Devices

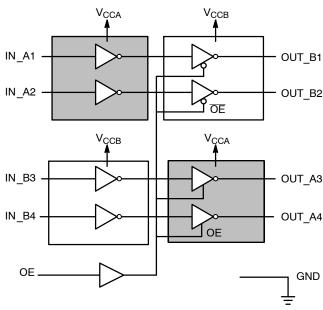


Figure 1. Logic Diagram



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## MARKING DIAGRAM

**WEM**■

UQFN12 MU SUFFIX CASE 523AE

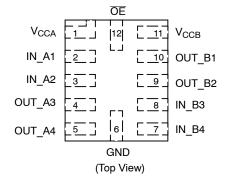
WE = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

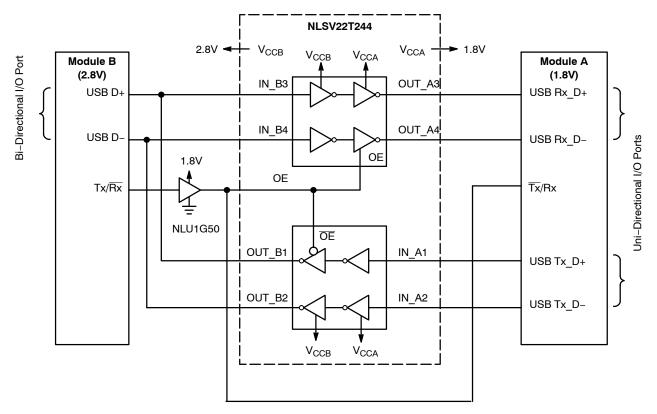
#### **PIN ASSIGNMENT**



#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NLSV22T244MUTAG	UQFN12 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



 $\mathsf{OE} = \mathsf{High}, \, \mathsf{Module} \, \mathsf{B} \, \mathsf{Transmits}, \, \mathsf{Module} \, \mathsf{A} \, \mathsf{Receives} = \mathsf{B} \to \mathsf{A}$ 

OE = Low, Module A Transmits, Module B Receives =  $\mathbf{A} \to \mathbf{B}$ 

Figure 2. Typical Application Bi-Directional to Uni-Directional Logic Level Translator

#### **PIN ASSIGNMENT**

Pin	Function
V <sub>CCA</sub>	A DC Power Supply
V <sub>CCB</sub>	B DC Power Supply
GND	Ground
IN_A1, IN_A2, IN_B3, IN_B4	Inputs
OUT_B1, OUT_B2, OUT_A3, OUT_A4	Outputs
OE	Output Enable

Inputs			Outp	outs
OE	IN_A1 IN_A2	IN_B3, IN_B4	OUT_B1, OUT_B2	OUT_A3 OUT_A4
Н	Х	L	3-State	L
	L	Н		Н
L	L	Х	L	3-State
	Н		Н	

## **MAXIMUM RATINGS**

Symbol	Rating		Value	Condition	Unit
V <sub>CCA</sub> , V <sub>CCB</sub>	DC Supply Voltage		-0.5 to +5.5		V
VI	DC Input Voltage IN_X	⟨n	-0.5 to +5.5		V
V <sub>C</sub>	Control Input	DE	-0.5 to +5.5		V
Vo	DC Output Voltage (Power Down) OUT_X	⟨n	-0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode) OUT_X <sub>n</sub>		-0.5 to +5.5		
	(Tri-State Mode) OUT_X	( <sub>n</sub>	-0.5 to +5.5		
I <sub>IK</sub>	DC Input Diode Current		-20	V <sub>I</sub> < GND	mA
lok	DC Output Diode Current		-50	V <sub>O</sub> < GND	mA
I <sub>O</sub>	DC Output Source/Sink Current		±50		mA
I <sub>CCA</sub> , I <sub>CCB</sub>	DC Supply Current Per Supply Pin		±100		mA
I <sub>GND</sub>	DC Ground Current per Ground Pin		±100		mA
T <sub>STG</sub>	Storage Temperature		-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CCA</sub> , V <sub>CCB</sub>	Positive DC Supply Voltage	1.6	3.6	V
VI	Bus Input Voltage	GND	3.6	V
V <sub>C</sub>	Control Input OE	GND	3.6	V
V <sub>IO</sub>	Bus Output Voltage (Power Down Mode) OUT_X <sub>n</sub>	GND	3.6	V
	(Active Mode) OUT_X <sub>n</sub>	GND	3.6	V
	(Tri-State Mode) OUT_X <sub>n</sub>	GND	3.6	V
T <sub>A</sub>	Operating Temperature Range	-40	+85	°C
Δt / ΔV	Input Transition Rise or Rate V <sub>I</sub> , from 30% to 70% of V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V $\pm$ 0.3 V	0	10	nS

## DC ELECTRICAL CHARACTERISTICS

					-40°C t	o +85°C	
Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.7 – 3.6	1.6 – 3.6	2.0	_	V
			2.3 – 2.7	1	1.6	-	
			1.4 – 2.3	1	0.65 * V <sub>CCA</sub>	_	
$V_{IL}$	Input LOW Voltage		2.7 – 3.6	1.6 – 3.6	-	0.8	V
			2.3 – 2.7	1	-	0.7	
			1.6 – 2.3	1	-	0.35 * V <sub>CCA</sub>	
V <sub>OH</sub>	Output HIGH Voltage	$I_{OH} = -100 \mu A; V_I = V_{IH}$	1.6 – 3.6	1.6 – 3.6	V <sub>CCB</sub> - 0.2	_	V
		$I_{OH} = -6 \text{ mA}; V_I = V_{IH}$	1.6	1.6	1.25	_	
			2.3	2.3	2.0	_	
		$I_{OH} = -12 \text{ mA}; V_I = V_{IH}$	2.3	2.3	1.8	_	
			2.7	2.7	2.2	_	
		$I_{OH} = -18 \text{ mA}; V_I = V_{IH}$	2.3	2.3	1.7	-	
			3.0	3.0	2.4	_	
		$I_{OH} = -24 \text{ mA}; V_I = V_{IH}$	3.0	3.0	2.2	_	
V <sub>OL</sub>	Output LOW Voltage	$I_{OL} = 100 \mu A; V_I = V_{IL}$	1.6 – 3.6	1.6 – 3.6	-	0.2	V
		$I_{OL} = 6 \text{ mA}; V_I = V_{IL}$	1.6	1.6	-	0.3	
		$I_{OL}$ = 12 mA; $V_I$ = $V_{IL}$	2.3	2.3	-	0.4	
			2.7	2.7	-	0.4	
		$I_{OL}$ = 18 mA; $V_I = V_{IL}$	2.3	2.3	-	0.6	
			3.0	3.0	-	0.5	
		$I_{OL}$ = 24 mA; $V_I$ = $V_{IL}$	3.0	3.0	-	0.6	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.6 – 3.6	1.6 – 3.6	-1.0	+1.0	μΑ
I <sub>OZ</sub>	I/O Tri-State Output Leakage Current	$T_A = 25^{\circ}C$ , OE = GND	1.6 – 3.6	1.6 – 3.6	_	2.0	μΑ
I <sub>CCA</sub>	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	1.6 – 3.6	1.6 – 3.6	-	2.0	μΑ
I <sub>CCB</sub>	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	1.6 – 3.6	1.6 – 3.6	_	2.0	μΑ
I <sub>CCA</sub> + I <sub>CCB</sub>	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	1.6 – 3.6	1.6 – 3.6	_	4.0	μΑ

## TOTAL STATIC POWER CONSUMPTION ( $I_{CCA} + I_{CCB}$ )

		-40°C to +85°C					
	V <sub>CCB</sub> (V)						
	3	.6	2.8		1.6		
V <sub>CCA</sub> (V)	Min	Max	Min	Max	Min	Max	Unit
3.6		2		2		2	μΑ
2.8		< 1		< 1		< 0.5	μΑ
1.6		< 1		< 1		< 0.5	μΑ

NOTE: Connect ground before applying supply voltage  $V_{CCA}$  or  $V_{CCB}$ . This device is designed with the feature that the power-up sequence of  $V_{CCA}$  and  $V_{CCB}$  will not damage the IC.

#### **AC ELECTRICAL CHARACTERISTICS**

					-40°C 1	o +85°C			
					V <sub>CC</sub>	<sub>B</sub> (V)			
			3	.6	2	.8	1	.6	1
Symbol	Parameter	V <sub>CCA</sub> (V)	Min	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> ,	Propagation Delay,	3.6		3.4		3.6		3.8	nS
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub>	2.8		3.6		3.8		4.0	1
		1.6		3.9		4.0		4.5	1
t <sub>PZH</sub> ,	Output Enable, OE to OUT_X <sub>n</sub>	3.6		5.8		6.0		6.2	nS
t <sub>PZL</sub>		2.8		6.0		6.2		6.4	7
		1.6		8.2		8.4		8.6	1
t <sub>PHZ</sub> ,	Output Disable,	3.6		5.8		6.0		6.2	nS
$t_{PLZ}$	OE to OUT_X <sub>n</sub>	2.8		6.0		6.2		6.4	1
		1.6		8.2		8.4		8.6	1
toshL,	Output-to-Output Skew, Data-to-Output	3.6		0.15		0.15		0.15	nS
toslh		2.8		0.15		0.15		0.15	1
		1.6		0.15		0.15		0.15	1

<sup>1.</sup> Propagation delays defined per Figure 3.

## **CAPACITANCE**

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA/B}$	3.5	pF
C <sub>I/O</sub>	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA/B}$	5.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CCA}, f = 10 \text{ MHz}$	10	pF

Typical values are at T<sub>A</sub> = +25°C.
 C<sub>PD</sub> is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$  where  $I_{CC} = I_{CCA} + I_{CCB}$  and  $N_{SW} = \text{total number of outputs switching.}$ 

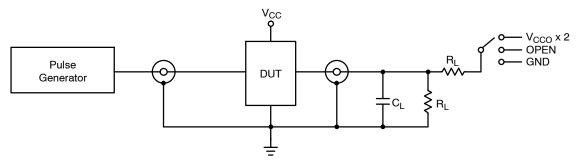


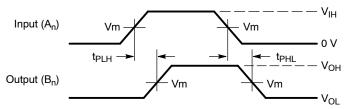
Figure 3. AC (Propagation Delay) Test Circuit

Test	Switch
t <sub>PLH</sub> , t <sub>PHL</sub>	OPEN
t <sub>PLZ</sub> , t <sub>PZL</sub>	V <sub>CCO</sub> x 2 at VCCB = 3.0 V - 3.6 mV, 2.3 V - 2.7 V, 1.6 V - 1.95 V
t <sub>PHZ</sub> , t <sub>PZH</sub>	GND

C<sub>L</sub> = 15 pF or equivalent (includes probe and jig capacitance)

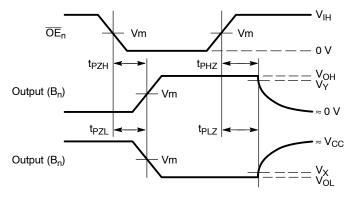
 $R_L$  = 2  $k\Omega$  or equivalent

 $Z_{OUT}$  of pulse generator = 50  $\Omega$ 



## Waveform 1 - Propagation Delays

 $t_R = t_F = 2.0 \text{ ns}, 10\% \text{ to } 90\%; f = 1 \text{ MHz}; t_W = 500 \text{ ns}$ 



Waveform 2 - Output Enable and Disable Times

 $t_R$  =  $t_F$  = 2.0 ns, 10% to 90%; f = 1 MHz;  $t_W$  = 500 ns

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

	V <sub>CC</sub>
Symbol	3.0 V – 3.6 V
$V_{mA}$	V <sub>CCA</sub> /2
$V_{mB}$	V <sub>CCB</sub> /2
V <sub>X</sub>	V <sub>OL</sub> x 0.1
V <sub>Y</sub>	V <sub>OH</sub> x 0.9

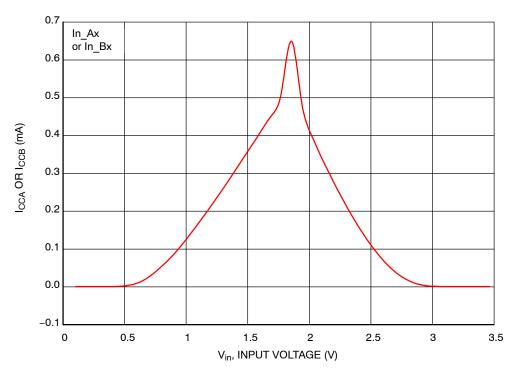
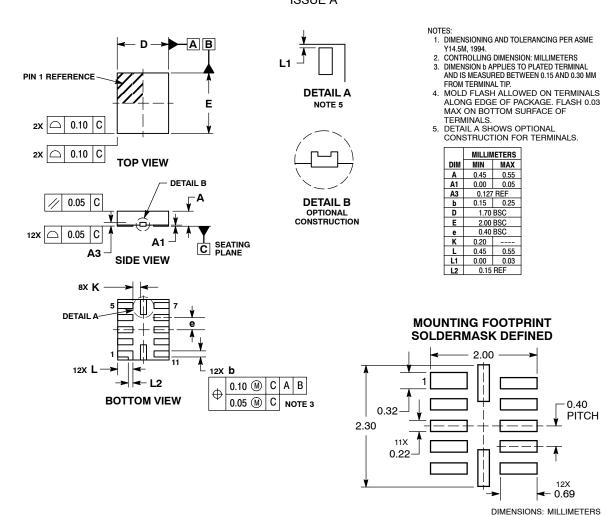


Figure 5. Delta  $I_{CC}$  Increase in  $I_{CC}$  per Input Voltage, Other Inputs at  $V_{CCA}\,/\,V_{CCB}$  or GND

#### PACKAGE DIMENSIONS

#### UQFN12 1.7x2.0, 0.4P CASE 523AE-01 ISSUE A



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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