NLSX3014

4-Bit 100 Mb/s Configurable Dual-Supply Level Translator

The NLSX3014 is a 4−bit configurable dual−supply bidirectional level translator without a direction control pin. The I/O V_{CC}− and I/O V_L−ports are designed to track two different power supply rails, V_{CC} and V_L respectively. The V_{CC} supply rail is configurable from 1.3 V to 4.5 V while the V_L supply rail is configurable from 0.9 V to (V_{CC} − 0.4) V. This allows lower voltage logic signals on the V_L side to be translated into higher voltage logic signals on the V_{CC} side, and vice−versa. Both I/O ports are auto−sensing; thus, no direction pin is required.

The Output Enable (EN) input, when Low, disables both I/O ports by putting them in 3−state. This significantly reduces the supply currents from both V_{CC} and V_L. The EN signal is designed to track V_L.

Features

- Wide High−Side V_{CC} Operating Range: 1.3 V to 4.5 V
  Wide Low−Side V_L Operating Range: 0.9 V to (V_{CC} − 0.4) V
- High−Speed with 100 Mb/s Guaranteed Date Rate for $V_L > 1.6$ V
- Low Bit−to−Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non−preferential Powerup Sequencing
- Small packaging: 1.7 mm x 2.0 mm UQFN12
- This is a Pb−Free Device

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

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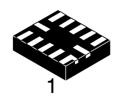
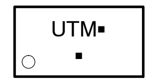


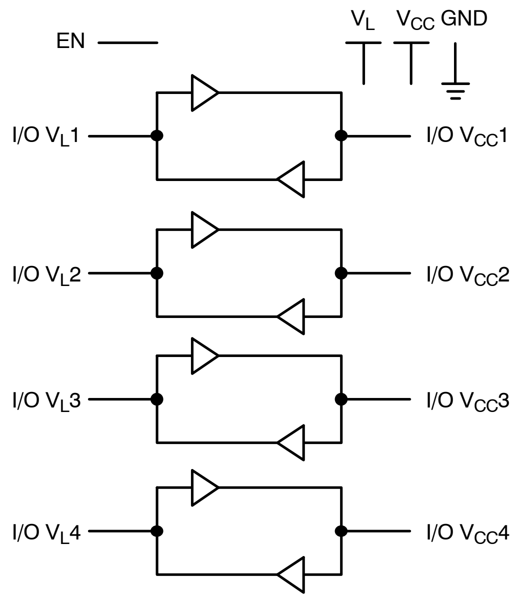
UQFN12
MU SUFFIX
CASE 523AE

MARKING DIAGRAM

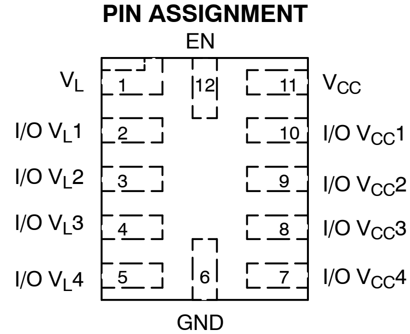


UT = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

LOGIC DIAGRAM



PIN ASSIGNMENT



(TOP VIEW)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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Publication Order Number:
NLSX3014/D

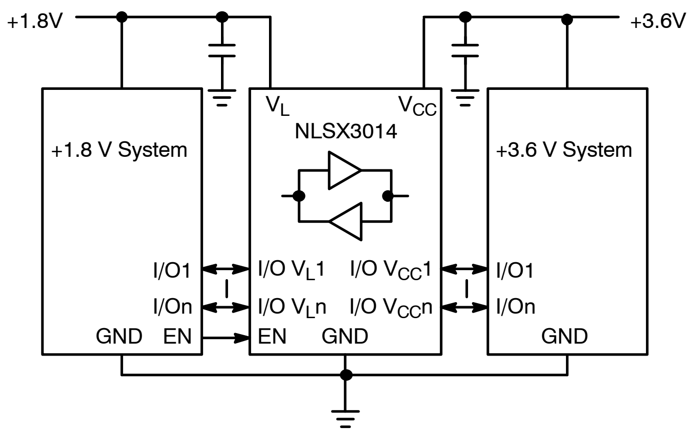


Figure 1. Typical Application Circuit

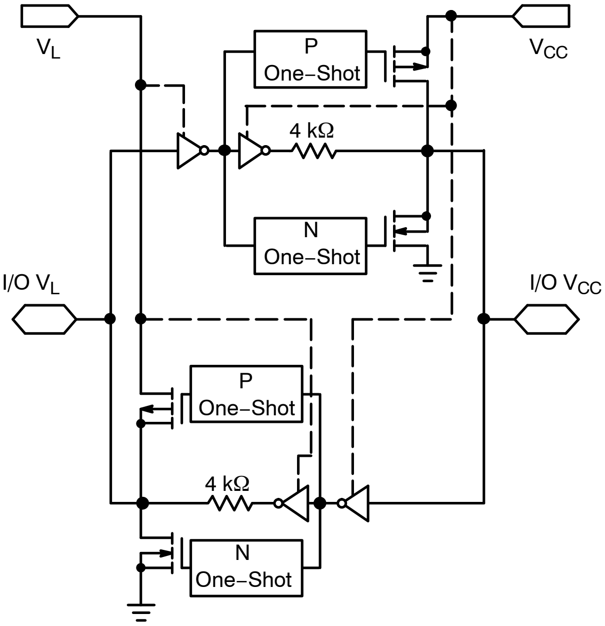


Figure 2. Simplified Functional Diagram (1 I/O Line) (EN = 1)

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Input Voltage
V_L	V_L Input Voltage
GND	Ground
EN	Output Enable
I/O V_{CC}n	I/O Port, Referenced to V_{CC}
I/O V_Ln	I/O Port, Referenced to V_L

FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	V_{CC} Supply Voltage	−0.5 to +5.5		V
V_L	V_L Supply Voltage	−0.5 to +5.5		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.5 to (V_{CC} + 0.3)		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.5 to (V_L + 0.3)		V
V_{EN}	Enable Control Pin DC Input Voltage	−0.5 to +5.5		V
I_{IK}	Input Diode Clamp Current	−50	V_I < GND	mA
I_{OK}	Output Diode Clamp Current	−50	V_O < GND	mA
I_{CC}	DC Supply Current Through V_{CC}	± 100		mA
I_L	DC Supply Current Through V_L	± 100		mA
I_{GND}	DC Ground Current Through Ground Pin	± 100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	V_{CC} Supply Voltage		1.3	4.5	V
V_L	V_L Supply Voltage		0.9	V_{CC} − 0.4	V
V_{EN}	Enable Control Pin Voltage		GND	4.5	V
V_{IO}	Bus Input/Output Voltage	I/O V_{CC} I/O V_L	GND GND	4.5 4.5	V
T_A	Operating Temperature Range		−40	+85	°C
ΔI/ΔV	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ± 0.3 V		0	10	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 1)	V_{CC} (V) (Note 2)	V_L (V) (Note 3)	−40°C to +85°C Min	Typ (Note 4)	Max	Unit
V_{IHC}	I/O V_{CC} Input HIGH Voltage		1.3 to 4.5	0.9 to (V_{CC} – 0.4)	0.8 * V_{CC}	–	–	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		1.3 to 4.5	0.9 to (V_{CC} – 0.4)	–	–	0.2 * V_{CC}	V
V_{IHL}	I/O V_L Input HIGH Voltage		1.3 to 4.5	0.9 to (V_{CC} – 0.4)	0.8 * V_L	–	–	V
V_{ILL}	I/O V_L Input LOW Voltage		1.3 to 4.5	0.9 to (V_{CC} – 0.4)	–	–	0.2 * V_L	V
V_{IH}	Control Pin Input HIGH Voltage	T_A = +25°C	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	0.8 * V_L	–	–	V
V_{IL}	Control Pin Input LOW Voltage	T_A = +25°C	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	–	–	0.2 * V_L	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} Source Current = 20 μA	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	0.8 * V_{CC}	–	–	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} Sink Current = 20 μA	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	–	–	0.2 * V_{CC}	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L Source Current = 20 μA	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	0.8 * V_L	–	–	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L Sink Current = 20 μA	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	–	–	0.2 * V_L	V

1. Normal test conditions are V_{EN} = 0 V, C_{IOVCC} = 15 pF and C_{IOVL} = 15 pF, unless otherwise specified.
2. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
3. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} – 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} – 0.4) V.
4. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

POWER CONSUMPTION

Symbol	Parameter	Test Conditions (Note 5)	V_{CC} (V) (Note 6)	V_L (V) (Note 7)	−40°C to +85°C Min	Typ	Max	Unit
I_{Q-VCC}	Supply Current from V_{CC}	EN = V_L; I/O V_{CCn} = 0 V, I/O V_{Ln} = 0 V, I/O V_{CCn} = V_{CC} or I/O V_{Ln} = V_L and I_o = 0	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	1.0	μA
I_{Q-VL}	Supply Current from V_L	EN = V_L; I/O V_{CCn} = 0 V, I/O V_{Ln} = 0 V, I/O V_{CCn} = V_{CC} or I/O V_{Ln} = V_L and I_o = 0	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	1.0	μA
		EN = V_L, I/O V_{CCn} = 0 V, I/O V_{Ln} = 0 V, I/O V_{CCn} = V_{CC} or I/O V_{Ln} = (V_{CC} – 0.2 V) and I_o = 0		< (V_{CC} – 0.2)	–	–	2.0	
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	1.0	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	0.2	μA
		EN = 0 V		V_{CC} – 0.2	–	–	2.0	
I_{OZ}	I/O Tristate Output Mode Leakage Current	EN = 0 V	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	0.15	μA
		EN = 0 V		V_{CC} – 0.2	–	–	2.0	
I_{EN}	Output Enable Pin Input Current	–	1.3 to 3.6	0.9 to (V_{CC} – 0.4)	–	–	1.0	μA

5. Normal test conditions are V_{EN} = 0 V, C_{IOVCC} = 15 pF and C_{IOVL} = 15 pF, unless otherwise specified.
6. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 3.6 V.
7. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} – 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} – 0.4) V.

TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 8)	V_{CC} (V) (Note 9)	V_L (V) (Note 10)	−40°C to +85°C Min	Typ (Note 11)	Max	Unit
t_{R-VCC}	I/O V_{CC} Rise Time (Output = I/O_V_{CC})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		1.3	1.7	ns
			> 2.0	> 1.6		0.9	1.1	
t_{F-VCC}	I/O V_{CC} Falltime (Output = I/O_V_{CC})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		0.8	1.2	ns
			> 2.0	> 1.6		0.6	1.0	
t_{R-VL}	I/O V_L Risetime (Output = I/O_V_L)	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		2.7	3.0	ns
			> 2.0	> 1.6		0.8	1.0	
t_{F-VL}	I/O V_L Falltime (Output = I/O_V_L)	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		0.8	1.0	ns
			> 2.0	> 1.6		0.7	0.8	
Z_{O-VCC}	I/O V_{CC} One−Shot Output Impedance		1.3 to 4.5	0.9 to (V_{CC} – 0.4)		30		Ω
Z_{O-VL}	I/O V_L One−Shot Output Impedance		1.3 to 4.5	0.9 to (V_{CC} – 0.4)		30		Ω
t_{PD_VL-VCC}	Propagation Delay (Output = I/O_V_{CC}, t_{PHL}, t_{PLH})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		15	17	ns
			> 2.0	> 1.6		4	5	
t_{PD_VCC-VL}	Propagation Delay (Output = I/O_V_L, t_{PHL}, t_{PLH})	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		10	11	ns
			> 2.0	> 1.6		3	4	
$t_{SK\ VL-VCC}$	Channel−to−Channel Skew (Output = I/O_V_{CC})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		0.6	1	nS
			> 2.0	> 1.6		0.2	0.8	
t_{SK_VCC-VL}	Channel−to−Channel Skew (Output = I/O_V_L)	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		0.4	0.6	nS
			> 2.0	> 1.6		0.2	0.3	
	Maximum Data Rate	(Output = I/O_V_{CC}, C_{IOVCC} = 15 pF)	1.3 to 4.5	0.9 to (V_{CC} – 0.4)	60			Mb/s
		(Output = I/O_V_L, C_{IOVL} = 15 pF)	> 2.0	> 1.6	100			

8. Normal test conditions are V_{EN} = 0 V, C_{IOVCC} = 15 pF and C_{IOVL} = 15 pF, unless otherwise specified.
9. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
10. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} – 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} – 0.4) V.
11. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

ENABLE / DISABLE TIME MEASUREMENTS

Symbol	Parameter	Test Conditions (Note 12)	V_{CC} (V) (Note 13)	V_L (V) (Note 14)	−40°C to +85°C Min	Typ (Note 15)	Max	Unit
t_{EN-VCC}	Turn−On Enable Time (Output = I/O_V_{CC}, t_{pZH})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		80	140	ns
	Turn−On Enable Time (Output = I/O_V_{CC}, t_{pZL})	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		175	300	ns
t_{EN-VL}	Turn−On Enable Time (Output = I/O_V_L, t_{pZH})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		250	475	ns
	Turn−On Enable Time (Output = I/O_V_L, t_{pZL})	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		175	250	ns
$t_{DIS-VCC}$	Turn−Off Disable Time (Output = I/O_V_{CC}, t_{pHZ})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		90	140	ns
	Propagation Delay (Output = I/O_V_{CC}, t_{PLZ})	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		150	200	ns
t_{DIS-VL}	Turn−Off Disable Time (Output = I/O_V_L, t_{pHZ})	C_{IOVCC} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		200	300	ns
	Propagation Delay (Output = I/O_V_L, t_{PLZ})	C_{IOVL} = 15 pF	1.3 to 4.5	0.9 to (V_{CC} – 0.4)		150	250	ns

12. Normal test conditions are V_{EN} = 0 V, C_{IOVCC} = 15 pF and C_{IOVL} = 15 pF, unless otherwise specified.
13. V_{CC} is the supply voltage associated with the high voltage port, and V_{CC} ranges from +1.3 V to 4.5 V under normal operating conditions.
14. V_L is the supply voltage associated with the low voltage port. V_L must be less than or equal to (V_{CC} – 0.4) V during normal operation. However, during startup and shutdown conditions, V_L can be greater than (V_{CC} – 0.4) V.
15. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25 °C. All units are production tested at T_A = +25 °C. Limits over the operating temperature range are guaranteed by design.

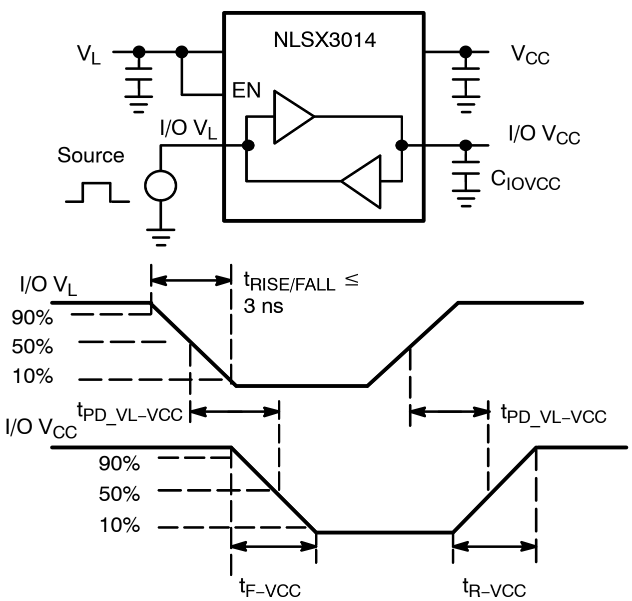


Figure 3. Driving I/O V_L Test Circuit and Timing

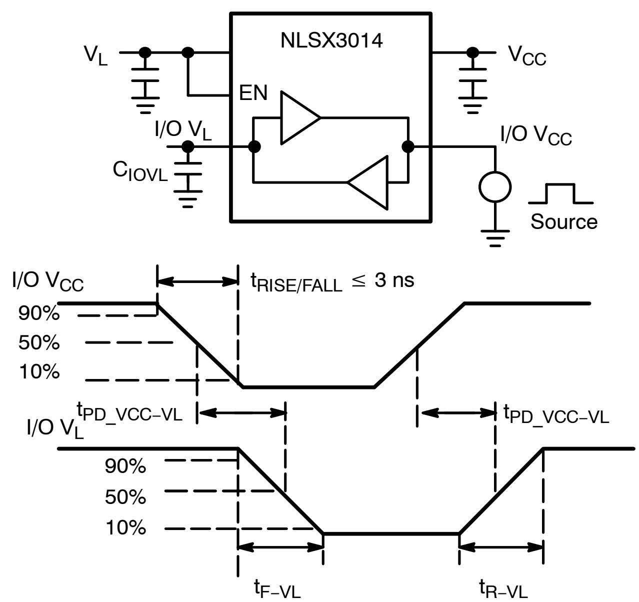
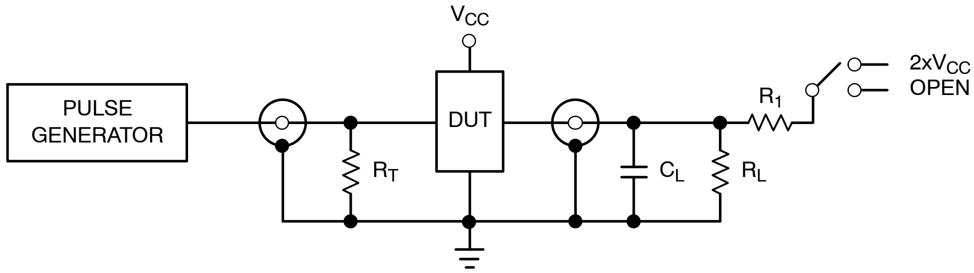


Figure 4. Driving I/O V_{CC} Test Circuit and Timing



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 5. Test Circuit for Enable/Disable Time Measurement

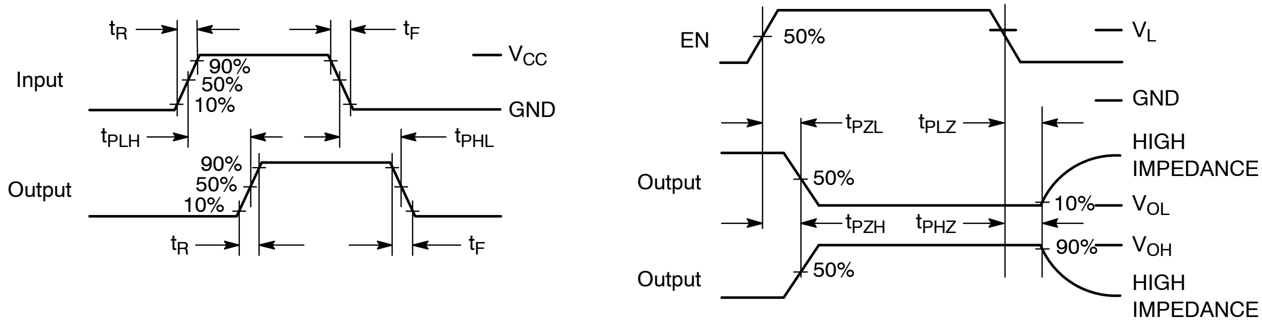


Figure 6. Timing Definitions for Propagation Delays and Enable/Disable Measurement

TEST CONDITIONS

1. T_A = +25°C,
2. Input Applied to 1 channel, the other 3 inputs are grounded,
3. C_{Load} = 15 pF

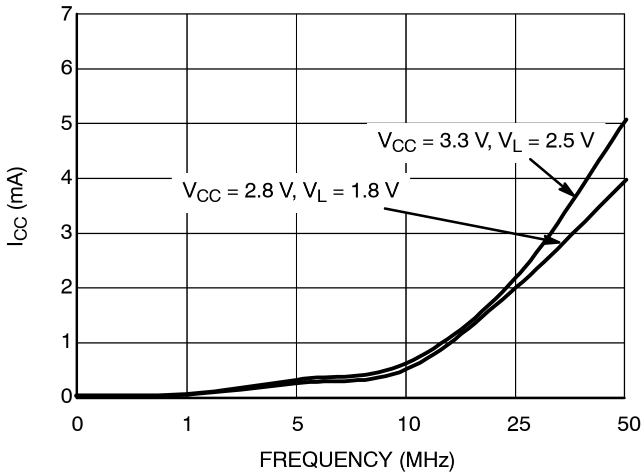


Figure 7. I_{CC} vs. Frequency (Input = I/O V_{CC}, Output = I/O V_L)

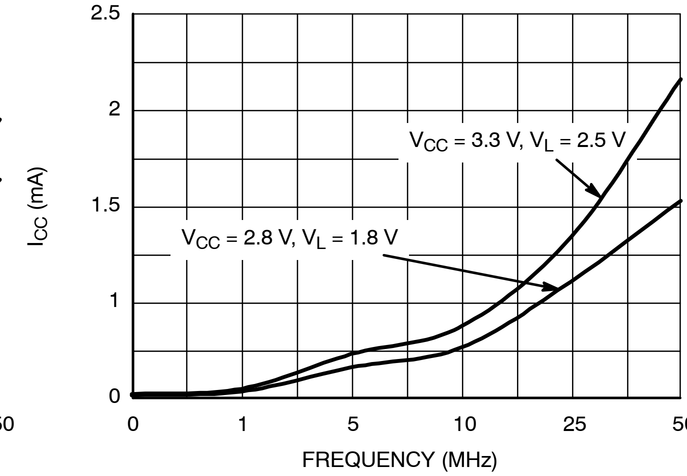


Figure 8. I_L vs. Frequency (Input = I/O V_{CC}, Output = I/O V_L)

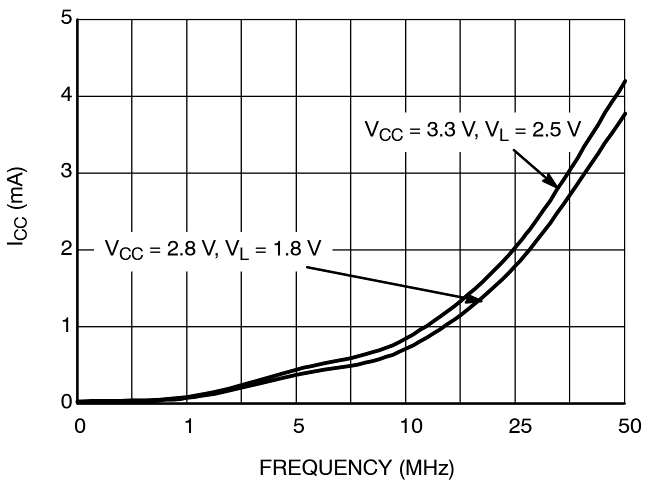


Figure 9. I_{CC} vs. Frequency (Input = I/O V_L, Output =I/O V_{CC})

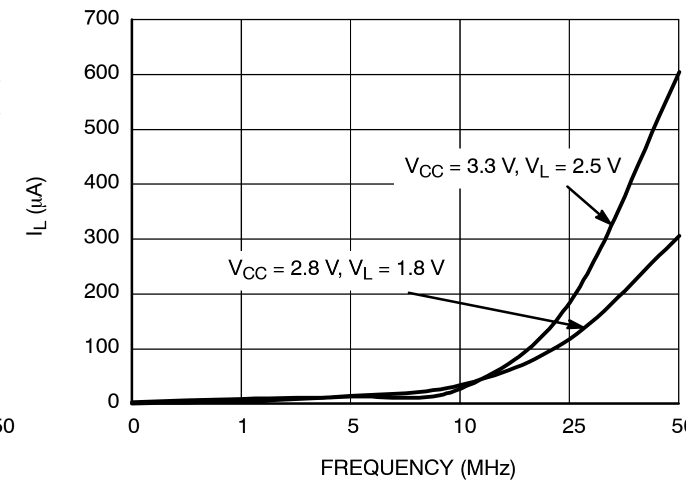


Figure 10. I_L vs. Frequency (Input = I/O V_L, Output = I/O V_{CC})

IMPORTANT APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX3014 auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX3014 consists of four bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high−to−low and low−to−high transitions.

Input Driver Requirements

For proper operation, the input driver to the auto sense translator should be capable of driving 2.0 mA of peak output current.

Output Load Requirements

The NLSX3014 is designed to drive CMOS inputs. Resistive pullup or pulldown loads of less than 50 kΩ should not be used with this device. The NLSX3373 or NLSX3378 open−drain auto sense translators are alternate translator options for an application such as the I^2C bus that requires pullup resistors.

Enable Input (EN)

The NLSX3014 has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over−Voltage Tolerant (OVT) protection.

Uni−Directional versus Bi−Directional Translation

The NLSX3014 can function as a non−inverting uni−directional translator. One advantage of using the translator as a uni−directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni−directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

It is recommended that the V_L supply should be less than or equal to the value of the V_{CC} minus 0.4 V. The sequencing of the power supplies will not damage the device during the power up operation; however, the current consumption of the device will increase if V_L exceeds V_{CC} minus 0.4 V. The Enable (EN) pin can be used to provide power savings. Both I/O ports are tri−stated and in low power consumption state if the EN input equals 0 V.

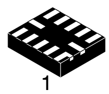
The enable pin should be used to enter the low current tri−state mode, rather than setting either the V_L or V_{CC} supplies to 0 V. The NLSX3014 will not be damaged if either V_L or V_{CC} is equal to 0 V while the other supply voltage is at a nominal operating value; however, the operation of the translator cannot be guaranteed during single supply operation.

For optimal performance, 0.01 to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the power supply voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

ORDERING INFORMATION

Device	Package	Shipping†
NLSX3014MUTAG	UQFN12 (Pb−Free)	3000 / Tape & Reel

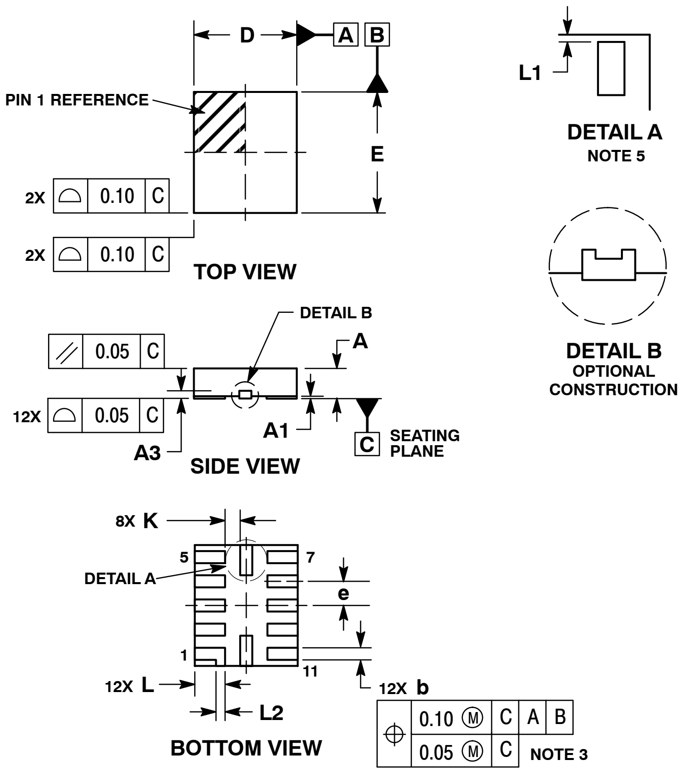
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 4:1

UQFN12 1.7x2.0, 0.4P
CASE 523AE−01
ISSUE A

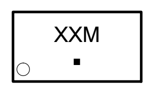
DATE 11 JUN 2007



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

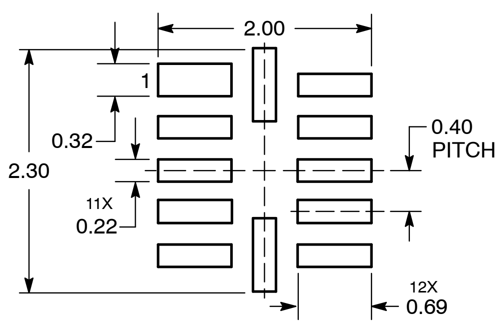
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

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