2-Bit 20 Mb/s Dual-Supply Level Translator

NLSX4302E

The NLSX4302E is a 2−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The V_{CC} I/O and V_L I/O ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both the V_{CC} and V_L supply rails are configurable from 1.5 V to 5.5 V. This allows voltage logic signals on the V_L side to be translated into lower, higher or equal value voltage logic signals on the V_{CC} side, and vice−versa.

The NLSX4302E translator uses external pull−up resistors on the I/O lines. The external pull−up resistors are used to pull up the I/O lines to either V_L or V_{CC}. The NLSX4302E is an excellent match for open−drain applications such as the I^2C communication bus.

Features

- V_L can be Less than, Greater than or Equal to V_{CC}
- Wide V_{CC} Operating Range: 1.5 V to 5.5 V
  Wide V_L Operating Range: 1.5 V to 5.5 V
- High−Speed with 20 Mb/s Guaranteed Date Rate
- Low Bit−to−Bit Skew
- Enable Input and I/O Pins are Overvoltage Tolerant (OVT) to 5.5 V
- Non−preferential Powerup Sequencing
- Power−Off Protection
- Small Space Saving Package: 1.4 mm x 1.2 mm UQFN8 Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- I^2C, SMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

Important Information

- ESD Protection for All Pins
  - Human Body Model (HBM) > 6000 V
  - Machine Model (MM) > 400 V

ON Semiconductor®

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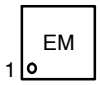
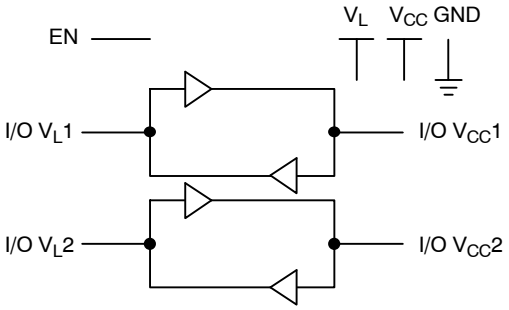
MARKING DIAGRAMS

UQFN8
MU SUFFIX
CASE 523AS



E = Specific Device Code
M = Date Code

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NLSX4302EBMUTCG	UQFN8 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

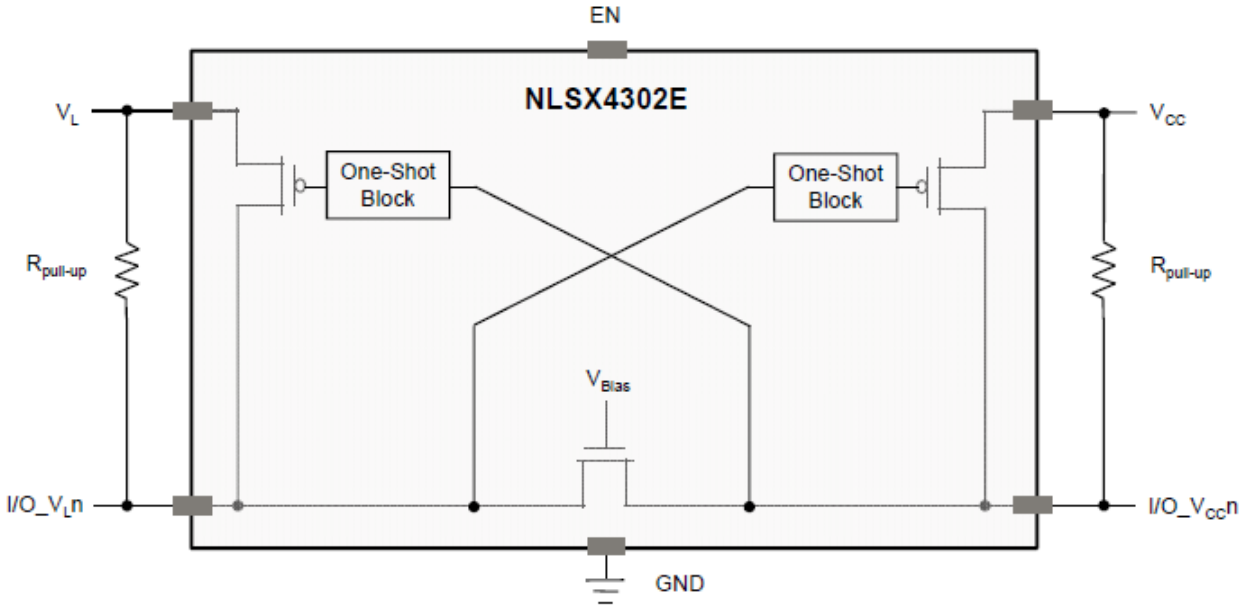
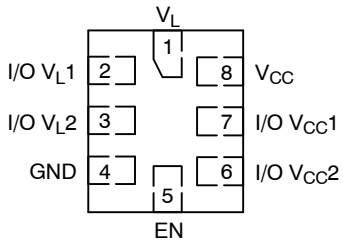


Figure 1. Block Diagram (1 I/O Line)



UQFN8
(Top Through View)

Figure 2. Pin−out Diagram

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Supply Voltage
V_L	V_L Supply Voltage
GND	Ground
EN	Output Enable, Referenced to V_L
I/O V_{CC}n	I/O Port, Referenced to V_{CC}
I/O V_Ln	I/O Port, Referenced to V_L

FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	High−side DC Supply Voltage	−0.3 to +7.0		V
V_L	High−side DC Supply Voltage	−0.3 to +7.0		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.3 to (V_{CC} + 0.3)		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.3 to (V_L + 0.3)		V
V_{EN}	Enable Control Pin DC Input Voltage	−0.3 to +7.0		V
I_{I/O_SC}	Short−Circuit Duration (I/O V_L and I/O V_{CC} to GND)	40	Continuous	mA
T_{STG}	Storage Temperature	−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	High−side Positive DC Supply Voltage	1.5	5.5	V
V_L	High−side Positive DC Supply Voltage	1.5	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	5.5	V
V_{IO_VCC}	I/O Pin Voltage (Side referred to V_{CC})	GND	V_{CC}	V
V_{IO_VL}	I/O Pin Voltage (Side referred to V_L)	GND	V_L	V
$\Delta t/\Delta V$	Input Transition Rise and Fall Rate I/O V_L− or I/O V_L− Ports, Push−Pull Driving Control Input		10 10	ns/V
T_A	Operating Temperature Range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS (V_L = 1.5 V to 5.5 V and V_{CC} = 1.5 V to 5.5 V, unless otherwise specified) (Note 1)

Symbol	Parameter	Test Conditions (Note 2)		V_L (V)	V_{CC} (V)	–40°C to +85°C			Unit
						Min	Typ	Max	
V_{IH_VL}	I/O High Level I/O_VL	Data Inputs I/O_VL$_n$		1.65–5.50	1.65–5.50	V_L – 0.4			V
		Control Input EN		1.65–5.50	1.65–5.50	V_L x 0.7			
V_{IH_VCC}	I/O High Level I/O_VCC	Data Inputs I/O_VCC$_n$		1.65–5.50	1.65–5.50	V_{CC} – 0.4			V
V_{IL_VL}	I/O Low Level I/O_VL	Data Inputs I/O_VL$_n$		1.65–5.50	1.65–5.50			0.4	V
		Control Input EN		1.65–5.50	1.65–5.50			V_L x 0.3	
V_{IL_VCC}	I/O Low Level I/O_VCC	Data Inputs I/O_VCC$_n$		1.65–5.50	1.65–5.50			0.4	V
V_{OL}	Low Level Output Voltage	V_{IL} = 0.15 V, I_{OL} = 6 mA		1.65–5.50	1.65–5.50			0.4	V
I_L	Input Leakage Current	Control Input EN, V_{IN} = V_L or GND		1.65–5.50	1.65–5.50			±1	μA
I_{OFF}	Power–Off Leakage Current	I/O_VL$_n$, I/O_VCC$_n$	V_{IN} or V_O = 0 to 5.5 V	0	0			±2	μA
		I/O_VL$_n$		0	5.50				
		I/O_VCC$_n$		5.50	0				
I_{OZ}	Tristate Output Mode Leakage Current (Note 3)	I/O_VL$_n$, I/O_VCC$_n$	V_O = 0 to 5.5 V, EN = V_{IL}	5.50	5.50			±2	μA
		I/O_VL$_n$	V_O = 0 to 5.5 V, EN = Don't Care	5.50	0				
		I/O_VCC$_n$		0	5.50				
I_{CC}	Quiescent Supply Current, Active Mode (Notes 4, 5)	V_L	V_{IN} = V_{CCI} or GND, I_O = 0, EN = V_{IH_VL}	1.65–5.50	1.65–5.50			5.0	μA
		V_{CC}							
I_{CCZ}	Quiescent Supply Current, Standby Mode (Notes 4, 5)	V_L	V_{IN} = V_{CCI} or GND, I_O = 0, EN = V_{IL_VL}	1.65–5.50	1.65–5.50			5.0	μA
		V_{CC}							
I_{CC_OFF}	Quiescent Supply Current, Power–Off (Notes 3, 5)	V_L	V_{IN} = 5.5 V or GND, I_O = 0, EN = Don't Care, I/O_VCC to I/O_VL	0	1.65–5.50			2.0	μA
				1.65–5.50	0				
		V_{CC}	V_{IN} = 5.5 V or GND, I_O = 0, EN = Don't Care, I/O_VL to I/O_VCC	1.65–5.50	0				
				0	1.65–5.50				

1. Typical values are for V_L = +1.8 V, V_{CC} = +3.3 V and T_A = +25°C.
2. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
3. "Don't care" indicates any valid logic level.
4. V_{CCI} is the power supply associated with the input side.
5. Reflects current per supply, V_L or V_{CC}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

OUTPUT RISE / FALL TIMES (Output Load: C_L = 50 pF, R_{PU} = 2.2 kΩ, push/pull driver, T_A = −40°C to +85°C) (Note 6)

Symbol	Parameter	V_{CCO} (Note 7)				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Typ	Typ	Typ	Typ	
t_{RISE}	Output Rise Time, I/O_VL_n, I/O_VCC_n	6.4	5	6.5	10.7	ns
t_{FALL}	Output Fall Time, I/O_VL_n, I/O_VCC_n	10	9.5	8.6	9.5	ns

6. Output rise and fall times guaranteed by design and are not production tested.
7. V_{CCO} is the V_L or V_{CC} power supply associated with the output side.

MAXIMUM DATA RATE (Output Load: C_L = 50 pF, R_{PU} = 2.2 kΩ, push/pull driver, T_A = −40°C to +85°C) (Note 8)

V_L	Parameter	V_{CC}				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Min	Min	Min	Min	
4.5 to 5.5 V	I/O_VL_n,to I/O_VCC_n or I/O_VCC_n to I/O_VL_n	50	41	31	17	MHz
3.0 to 3.6 V		34	35	36	23	MHz
2.3 to 2.7 V		25	27	30	24	MHz
1.65 to 1.95 V		14	16	22	21	MHz

8. Maximum frequency guaranteed by design and is not production tested.

AC ELECTRICAL CHARACTERISTICS (Output Load: C_L = 50 pF, R_{PU} = 2.2 kΩ, push/pull driver, T_A = −40°C to +85°C) (Note 9)

Symbol	Parameter	V_{CC}								Unit
		4.5 to 5.5 V		3.0 to 3.6 V		2.3 to 2.7 V		1.65 to 1.95 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
V_L = 4.5 to 5.5 V										
t_{PLH}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	2.5	4.3	3	5	3	6.4	4	8.6	ns
t_{PHL}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	5	8.1	8	13	8	17.3	15	28.5	ns
t_{PZL}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	14	19.6	16	20	22	26.5	33	44	ns
t_{PLZ}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	24	31.4	25	32	24	31.8	28	36.2	ns
t_{skew}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$ (Note 10)	0.3	0.3	0.5	0.6	0.8	0.8	1.2	1.9	ns
V_L = 3.0 to 3.6 V										
t_{PLH}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	2.5	4.7	3	5.4	3	6.5	5	9.3	ns
t_{PHL}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	7	14.2	6	10.1	8	14.6	15	27	ns
t_{PZL}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	15	18.8	18	22.3	19	23.5	29	38.3	ns
t_{PLZ}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	25	34.9	22	27.6	22	27.9	23	28.8	ns
t_{skew}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$ (Note 10)	0.4	0.5	0.5	0.6	0.6	0.7	2.5	3.0	ns
V_L = 2.3 to 2.7 V										
t_{PLH}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	3	5.6	4	6	4	7.3	6	10.3	ns
t_{PHL}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	12	18.1	11	14.1	8	11.9	15	22.1	ns
t_{PZL}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	16	23.7	17	21.5	25	30	31	36.6	ns
t_{PLZ}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	28	33.8	26	31	25	30.8	25	30	ns
t_{skew}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$ (Note 10)	0.5	0.7	0.8	1	0.6	0.6	2.3	2.7	ns
V_L = 1.65 to 1.95 V										
t_{PLH}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	5	9	5	9.2	6	9.2	7	12.7	ns
t_{PHL}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$	19	28.3	15	25.5	12	17.3	14	19	ns
t_{PZL}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	23	32.2	22	26.5	25	32	40	72	ns
t_{PLZ}	OE to I/O_VI$_n$, OE to I/O_VCC$_n$	35	44	32	38.7	33	36.7	30	36.5	ns
t_{skew}	I/O_VL$_n$ to I/O_VCC$_n$, I/O_VCC$_n$ to I/O_VL$_n$ (Note 10)	0.5	1.1	1.4	1.5	0.8	1.1	2.0	2.5	ns

9. AC characteristics are guaranteed by design and are not production tested.
10. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O_VL$_n$ or I/O_VCC$_n$) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Test Condition	Typical	Unit
C_{IN}	Input Capacitance, Control Pin (EN)	V_L = V_{CC} = GND	2	pF
C_{IO}	Input / Output Capacitance (I/O_VL_n, I/O_VCC_n)	V_L = V_{CC} = 5 V,EN = GND, I/O_VL_n = I/O_VCC_n = 5 V	3	pF
C_{PD}	Power Dissipation Capacitance (Note 11)	V_L = V_{CC} = 5 V,EN = 5 V, V_{IN} = 5 V or GND, f = 400 KHz	17	pF

11. C_{PD} is defined as the value of the internal equivalent capacitance per channel.

TEST SETUP AND TIMING DEFINITIONS

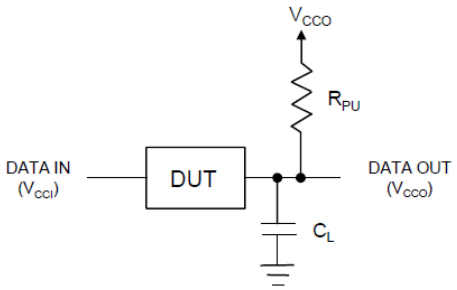


Figure 3. AC Test Circuit

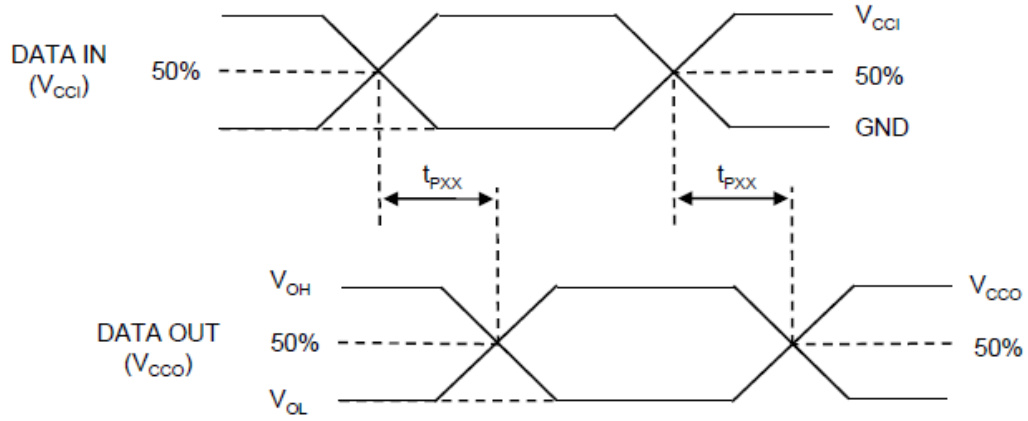


Figure 4. Propagation Delays and Tri-State Measurements

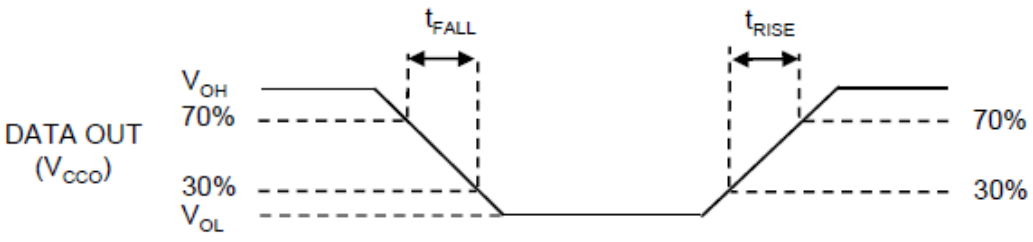


Figure 5. Definition of Rise and Fall Times

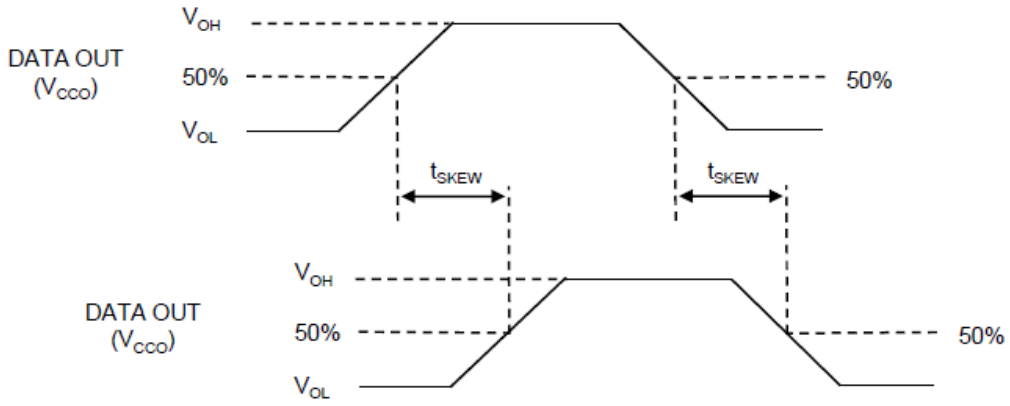


Figure 6. Definition of Output Skew

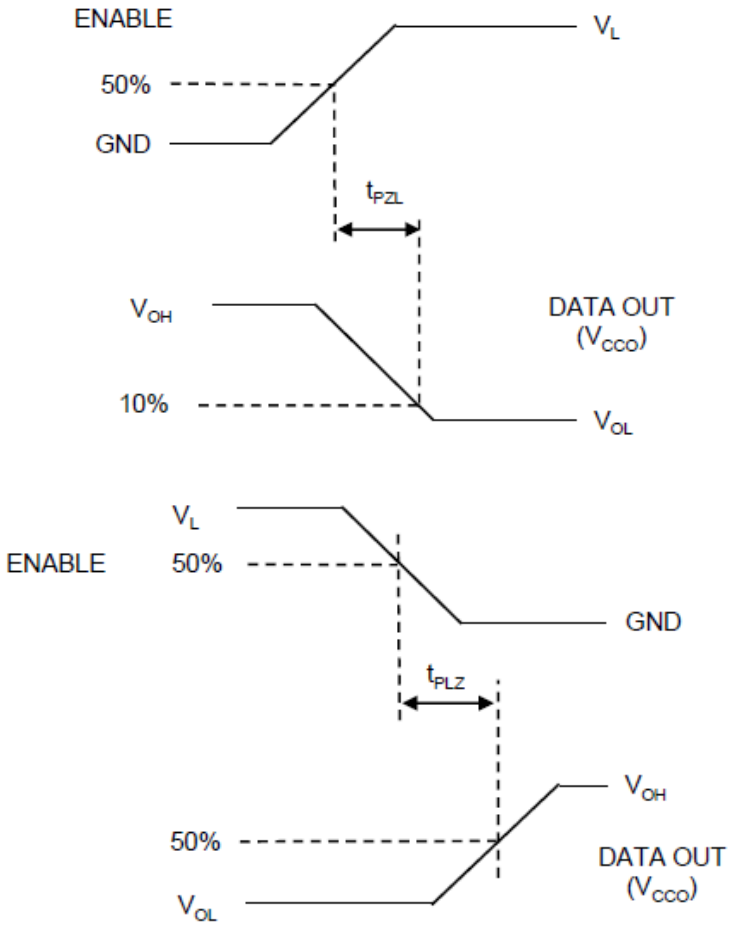


Figure 7. Definition of Output Tri-State Times

APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX4302E auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX4302E consists of two bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high−to−low and low−to−high transitions. Each input/output channel requires external pullup resistors.

Enable Input (EN)

The NLSX4302E has an Enable pin (EN) that can be used to minimize the power consumption of the device when the transmitter is not transmitting data. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Overvoltage Tolerant (OVT) protection.

Power Supply Guidelines

The sequencing of the power supplies will not damage the device during the power up operation. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V. For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

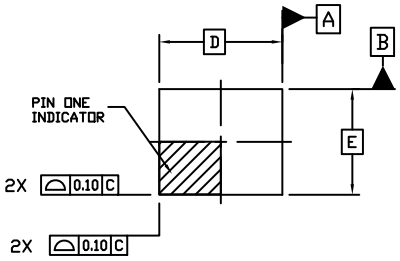
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

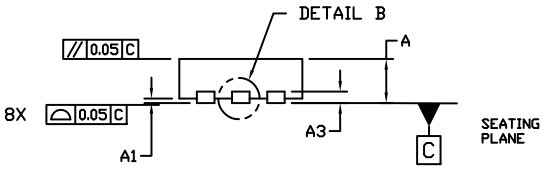
UQFN8, 1.4x1.2, 0.4P
CASE 523AS
ISSUE B

SCALE 4:1

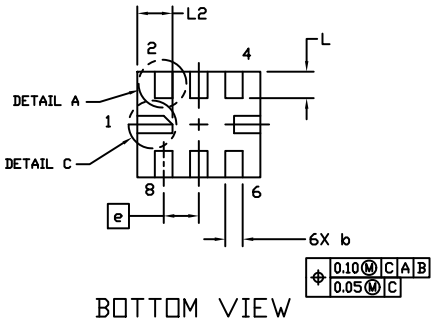
DATE 19 AUG 2021



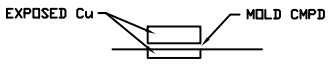
TOP VIEW



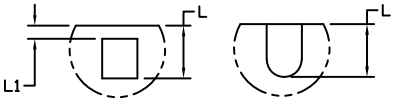
SIDE VIEW



BOTTOM VIEW



DETAIL B
ALTERNATE CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTIONS

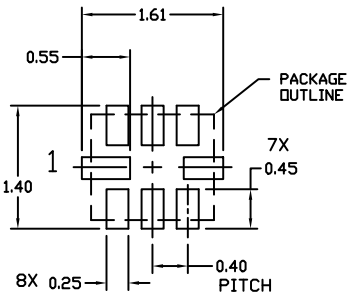
DETAIL C
ALTERNATE CONSTRUCTION

NOTE 4

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. REFER TO SPECIFIC DEVICE DATA SHEET FOR PIN 1 NOTCH LOCATION.

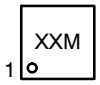
	MILLIMETERS	
DIM	MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.20	0.40
L1	---	0.15
L2	0.30	0.50



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON58906E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**UQFN8, 1.4X1.2, 0.4P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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onsemi Website: www.onsemi.com

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