NLSX5012

2-Bit 100 Mb/s Configurable Dual-Supply Level Translator

The NLSX5012 is a 2-bit configurable dual-supply autosensing bidirectional level translator that does not require a direction control pin. The I/O V_{CC}- and I/O V_L-ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both the V_{CC} and the V_L supply rails are configurable from 0.9 V to 4.5 V. This allows a logic signal on the V_L side to be translated to either a higher or a lower logic signal voltage on the V_{CC} side, and vice-versa.

The NLSX5012 offers the feature that the values of the V_{CC} and V_L supplies are independent. Design flexibility is maximized because V_L can be set to a value either greater than or less than the V_{CC} supply. In contrast, the majority of competitive auto sense translators have a restriction that the value of the V_L supply must be equal to less than (V_{CC} - 0.4) V.

The NLSX5012 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. Another feature of the NLSX5012 is that each I/O_V_{Ln} and I/O_V_{CCn} channel can function as either an input or an output.

An Output Enable (EN) input is available to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current from both V_{CC} and V_L. The EN signal is referenced to the V_L supply.

Features

- Wide V_{CC}, V_L Operating Range: 0.9 V to 4.5 V
- V_L and V_{CC} are independent
  - V_L may be greater than, equal to, or less than V_{CC}
- High 100 pF Capacitive Drive Capability
- High−Speed with 140 Mb/s Guaranteed Date Rate for V_{CC}, V_L > 1.8 V
- Low Bit−to−Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non−preferential Power−Up Sequencing
- Power−Off Protection
- Small packaging: UDFN8, SO−8, Micro8
- These are Pb−Free Devices

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
  - HBM (Human Body Model) > 8000 V

ON Semiconductor®

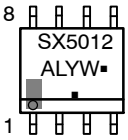
http://onsemi.com

MARKING DIAGRAMS

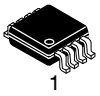
UDFN8
MU SUFFIX
CASE 517AJ

VA = Specific Device Code
M = Date Code
▪ = Pb−Free Package

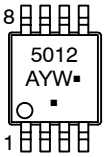
SO−8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package



Micro8
DM SUFFIX
CASE 846A



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NLSX5012MUTAG	UDFN8 (Pb−Free)	3000/Tape & Reel
NLSX5012DR2G	SO−8 (Pb−Free)	2500/Tape & Reel
NLSX5012DMR2G	Micro8 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

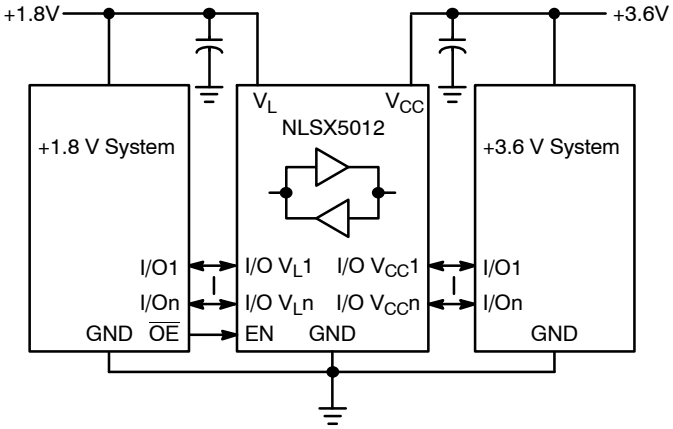


Figure 1. Typical Application Circuit

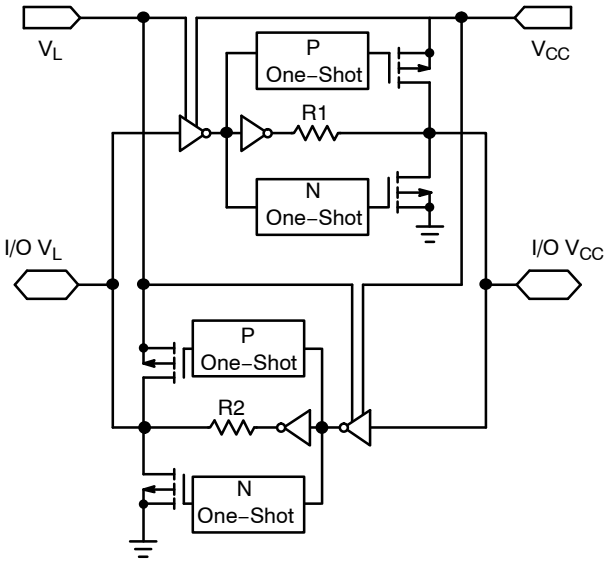


Figure 2. Simplified Functional Diagram (1 I/O Line)

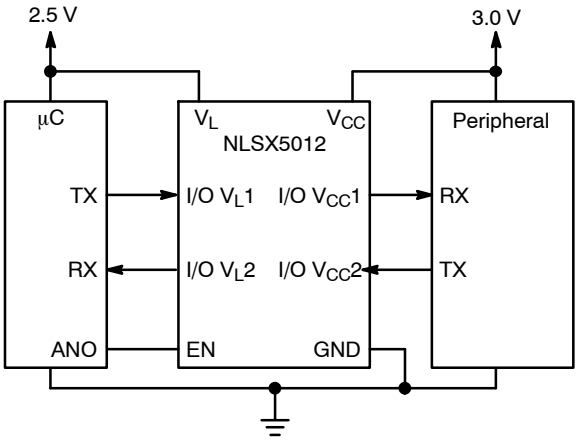


Figure 3. Application Example for $V_L < V_{CC}$

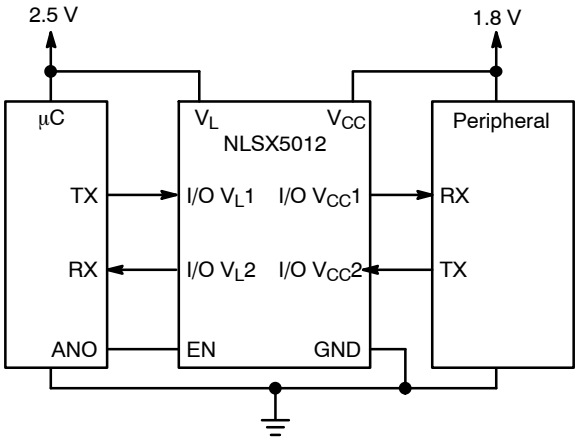


Figure 4. Application Example for $V_L > V_{CC}$

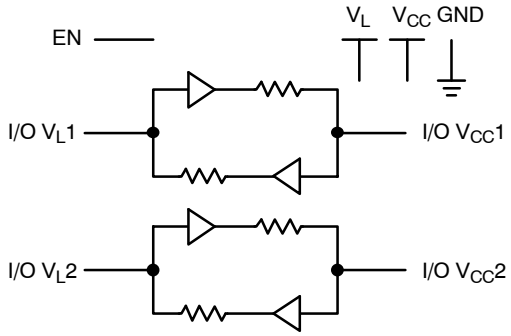


Figure 5. Logic Diagram

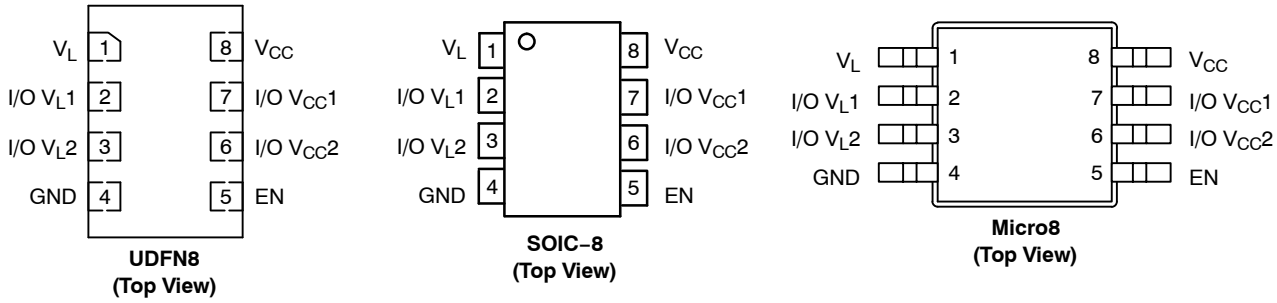


Figure 6. Pin Assignments

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Input Voltage
V_L	V_L Input Voltage
GND	Ground
EN	Output Enable
I/O V_{CC}n	I/O Port, Referenced to V_{CC}
I/O V_Ln	I/O Port, Referenced to V_L

FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	High−side DC Supply Voltage	−0.5 to +5.5		V
V_L	Low−side DC Supply Voltage	−0.5 to +5.5		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.5 to +5.5		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.5 to +5.5		V
V_I	Enable Control Pin DC Input Voltage	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_{CC}	DC Supply Current Through V_{CC}	±100		mA
I_L	DC Supply Current Through V_L	±100		mA
I_{GND}	DC Ground Current Through Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	High−side Positive DC Supply Voltage		0.9	4.5	V
V_L	Low−side Positive DC Supply Voltage		0.9	4.5	V
V_I	Enable Control Pin Voltage		GND	4.5	V
V_{IO}	Bus Input/Output Voltage	I/O V_{CC} I/O V_L	GND GND	4.5 4.5	V
T_A	Operating Temperature Range		−55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ± 0.3 V		0	10	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 1)	V_{CC} (V) (Note 2)	V_L (V) (Note 3)	−40°C to +85°C			−55°C to +125°C		Unit
					Min	Typ (Note 4)	Max	Min	Max	
V_{IHC}	I/O V_{CC} Input HIGH Voltage		0.9 – 4.5	0.9 – 4.5	2/3 * V_{CC}	–	–	2/3 * V_{CC}	–	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		0.9 – 4.5	0.9 – 4.5	–	–	1/3 * V_{CC}	–	1/3 * V_{CC}	V
V_{IHL}	I/O V_L Input HIGH Voltage		0.9 – 4.5	0.9 – 4.5	2/3 * V_L	–	–	2/3 * V_L	–	V
V_{ILL}	I/O V_L Input LOW Voltage		0.9 – 4.5	0.9 – 4.5	–	–	1/3 * V_L	–	1/3 * V_L	V
V_{IH}	Control Pin Input HIGH Voltage	T_A = +25°C	0.9 – 4.5	0.9 – 4.5	2/3 * V_L	–	–	2/3 * V_L	–	V
V_{IL}	Control Pin Input LOW Voltage	T_A = +25°C	0.9 – 4.5	0.9 – 4.5	–	–	1/3 * V_L	–	1/3 * V_L	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} source current = 20 μA	0.9 – 4.5	0.9 – 4.5	0.9 * V_{CC}	–	–	0.9 * V_{CC}	–	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} sink current = 20 μA	0.9 – 4.5	0.9 – 4.5	–	–	0.2	–	0.2	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L source current = 20 μA	0.9 – 4.5	0.9 – 4.5	0.9 * V_L	–	–	0.9 * V_L	–	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L sink current = 20 μA	0.9 – 4.5	0.9 – 4.5	–	–	0.2	–	0.2	V
I_{QVCC}	V_{CC} Supply Current	EN = V_L, I_O = 0 A, (I/O V_{CC} = 0 V or V_{CC}, I/O V_L = float) or (I/O V_{CC} = float, I/O V_L = 0 V or V_L)	0.9 – 4.5	0.9 – 4.5	–	–	1	–	2.5	μA
I_{QVL}	V_L Supply Current		0.9 – 4.5	0.9 – 4.5	–	–	1	–	2.5	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	T_A = +25°C, EN = 0 V (I/O V_{CC} = 0 V or V_{CC}, I/O V_L = float) or (I/O V_{CC} = float, I/O V_L = 0 V or V_L)	0.9 – 4.5	0.9 – 4.5	–	–	0.5	–	1.5	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current		0.9 – 4.5	0.9 – 4.5	–	–	0.5	–	1.5	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	T_A = +25°C, EN = 0V	0.9 – 4.5	0.9 – 4.5	–	–	±1	–	±1.5	μA
I_I	Control Pin Input Current	T_A = +25°C	0.9 – 4.5	0.9 – 4.5	–	–	±1	–	±1	μA
I_{OFF}	Power Off Leakage Current	I/O V_{CC} = 0 to 4.5V,	0	0	–	–	1	–	1.5	μA
		I/O V_L = 0 to 4.5 V	0.9 – 4.5	0	–	–	1	–	1.5	
			0	0.9 – 4.5	–	–	1	–	1.5	

1. Normal test conditions are V_I = 0 V, $C_{IOVCC} \le$ 15 pF and $C_{IOVL} \le$ 15 pF, unless otherwise specified.
2. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +0.9 V to 4.5 V under normal operating conditions.
3. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +0.9 V to 4.5 V under normal operating conditions.
4. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 5)	V_{CC} (V) (Note 6)	V_L (V) (Note 7)	−55°C to +125°C			Unit
					Min	Typ (Note 8)	Max	
t_{R-VCC}	I/O V_{CC} Rise Time	C_{IOVCC} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	8.5	nS
			1.8 – 4.5	1.8 – 4.5	–	–	3.5	
t_{F-VCC}	I/O V_{CC} Fall Time	C_{IOVCC} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	8.5	nS
			1.8 – 4.5	1.8 – 4.5	–	–	3.5	
t_{R-VL}	I/O V_L Rise Time	C_{IOVL} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	8.5	nS
			1.8 – 4.5	1.8 – 4.5	–	–	3.5	
t_{F-VL}	I/O V_L Fall Time	C_{IOVL} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	8.5	nS
			1.8 – 4.5	1.8 – 4.5	–	–	3.5	
Z_{OVCC}	I/O V_{CC} One−Shot Output Impedance	(Note 9)	0.9 1.8 4.5	0.9 – 4.5	– – –	37 20 6.0	– – –	Ω
Z_{OVL}	I/O V_L One−Shot Output Impedance	(Note 9)	0.9 1.8 4.5	0.9 – 4.5	– – –	37 20 6.0	– – –	Ω
t_{PD_VL-VCC}	Propagation Delay (Driving I/O V_{CC})	C_{IOVCC} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	35	nS
			1.8 – 4.5	1.8 – 4.5	–	–	10	
		C_{IOVCC} = 30 pF	0.9 – 4.5	0.9 – 4.5	–	–	35	
			1.8 – 4.5	1.8 – 4.5	–	–	10	
		C_{IOVCC} = 50 pF	1.0 – 4.5	1.0 – 4.5	–	–	37	
			1.8 – 4.5	1.8 – 4.5	–	–	11	
		C_{IOVCC} = 100 pF	1.2 – 4.5	1.2 – 4.5	–	–	40	
			1.8 – 4.5	1.8 – 4.5	–	–	13	
t_{PD_VCC-VL}	Propagation Delay (Driving I/O V_L)	C_{IOVL} = 15 pF	0.9 – 4.5	0.9 – 4.5	–	–	35	nS
			1.8 – 4.5	1.8 – 4.5	–	–	10	
		C_{IOVL} = 30 pF	0.9 – 4.5	0.9 – 4.5	–	–	35	
			1.8 – 4.5	1.8 – 4.5	–	–	10	
		C_{IOVL} = 50 pF	1.0 – 4.5	1.0 – 4.5	–	–	37	
			1.8 – 4.5	1.8 – 4.5	–	–	11	
		C_{IOVL} = 100 pF	1.2 – 4.5	1.2 – 4.5	–	–	40	
			1.8 – 4.5	1.8 – 4.5	–	–	13	
t_{SK}	Channel−to−Channel Skew	C_{IOVCC} = 15 pF, C_{IOVL} = 15 pF (Note 9)	0.9 – 4.5	0.9 – 4.5	–	–	0.15	nS
I_{IN_PEAK}	Input Driver Maximum Peak Current	EN = V_L; I/O_V_{CC} = 1 MHz Square Wave, Amplitude = V_{CC}, or I/O_V_L = 1 MHz Square Wave, Amplitude = V_L (Note 9)	0.9 – 4.5	0.9 – 4.5	–	–	5.0	mA

5. Normal test conditions are V_I = 0 V, $C_{IOVCC} \leq$ 15 pF and $C_{IOVL} \leq$ 15 pF, unless otherwise specified.
6. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +0.9 V to 4.5 V under normal operating conditions.
7. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +0.9 V to 4.5 V under normal operating conditions.
8. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
9. Guaranteed by design.

TIMING CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions (Note 10)	V_{CC} (V) (Note 11)	V_L (V) (Note 12)	−55°C to +125°C			Unit
						Min	Typ (Note 13)	Max	
t_{EN-VCC}	I/O_V_{CC} Output Enable Time	t_{PZH}	C_{IOVCC} = 15 pF, I/O_V_L = V_L	0.9 – 4.5	0.9 – 4.5	–	–	160	nS
		t_{PZL}	C_{IOVCC} = 15 pF, I/O_V_L = 0 V	0.9 – 4.5	0.9 – 4.5	–	–	130	
t_{EN-VL}	I/O_V_L Output Enable Time	t_{PZH}	C_{IOVL} = 15 pF, I/O_V_{CC} = V_{CC}	0.9 – 4.5	0.9 – 4.5	–	–	160	nS
		t_{PZL}	C_{IOVL} = 15 pF, I/O_V_{CC} = 0 V	0.9 – 4.5	0.9 – 4.5	–	–	130	
$t_{DIS-VCC}$	I/O_V_{CC} Output Disable Time	t_{PHZ}	C_{IOVCC} = 15 pF, I/O_V_L = V_L	0.9 – 4.5	0.9 – 4.5	–	–	210	nS
		t_{PLZ}	C_{IOVCC} = 15 pF, I/O_V_L = 0 V	0.9 – 4.5	0.9 – 4.5	–	–	175	
t_{DIS-VL}	I/O_V_L Output Disable Time	t_{PHZ}	C_{IOVL} = 15 pF, I/O_V_{CC} = V_{CC}	0.9 – 4.5	0.9 – 4.5	–	–	210	nS
		t_{PLZ}	C_{IOVL} = 15 pF, I/O_V_{CC} = 0 V	0.9 – 4.5	0.9 – 4.5	–	–	175	
MDR	Maximum Data Rate		C_{IO} = 15 pF	0.9 – 4.5	0.9 – 4.5	50	–	–	mbps
				1.8 – 4.5	1.8 – 4.5	140	–	–	
			C_{IO} = 30 pF	0.9 – 4.5	0.9 – 4.5	40	–	–	
				1.8 – 4.5	1.8 – 4.5	120	–	–	
			C_{IO} = 50 pF	1.0 – 4.5	1.0 – 4.5	30	–	–	
				1.8 – 4.5	1.8 – 4.5	100	–	–	
			C_{IO} = 100 pF	1.2 – 4.5	1.2 – 4.5	20	–	–	
				1.8 – 4.5	1.8 – 4.5	60	–	–	

10. Normal test conditions are V_I = 0 V, $C_{IOVCC} \le$ 15 pF and $C_{IOVL} \le$ 15 pF, unless otherwise specified.
11. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +0.9 V to 4.5 V under normal operating conditions.
12. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +0.9 V to 4.5 V under normal operating conditions.
13. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

DYNAMIC POWER CONSUMPTION (T_A = +25°C)

Symbol	Parameter	Test Conditions	V_{CC} (V) (Note 14)	V_L (V) (Note 15)	Typ (Note 16)	Unit
C_{PD_VL}	V_L = Input port, V_{CC} = Output Port	C_{Load} = 0, f = 1 MHz, EN = V_L (outputs enabled)	0.9	4.5	39	pF
			1.5	1.8	20	
			1.8	1.5	17	
			1.8	1.8	14	
			1.8	2.8	13	
			2.5	2.5	14	
			2.8	1.8	13	
			4.5	0.9	19	
	V_{CC} = Input port, V_L = Output Port	C_{Load} = 0, f = 1 MHz, EN = V_L (outputs enabled)	0.9	4.5	37	pF
			1.5	1.8	30	
			1.8	1.5	29	
			1.8	1.8	29	
			1.8	2.8	29	
			2.5	2.5	30	
			2.8	1.8	29	
			4.5	0.9	19	
C_{PD_VCC}	V_L = Input port, V_{CC} = Output Port	C_{Load} = 0, f = 1 MHz, EN = V_L (outputs enabled)	0.9	4.5	29	pF
			1.5	1.8	29	
			1.8	1.5	29	
			1.8	1.8	29	
			1.8	2.8	29	
			2.5	2.5	30	
			2.8	1.8	29	
			4.5	0.9	35	
	V_{CC} = Input port, V_L = Output Port	C_{Load} = 0, f = 1 MHz, EN = V_L (outputs enabled)	0.9	4.5	21	pF
			1.5	1.8	18	
			1.8	1.5	18	
			1.8	1.8	14	
			1.8	2.8	13	
			2.5	2.5	14	
			2.8	1.8	13	
			4.5	0.9	30	

14. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +0.9 V to 4.5 V under normal operating conditions.
15. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +0.9 V to 4.5 V under normal operating conditions.
16. Typical values are at T_A = +25°C.
17. $C_{PD\ VL}$ and $C_{PD\ VCC}$ are defined as the value of the IC's equivalent capacitance from which the operating current can be calculated for the V_L and V_{CC} power supplies, respectively. $I_{CC} = I_{CC}$ (dynamic) + I_{CC} (static) ≈ I_{CC}(operating) ≈ C_{PD} x V_{CC} x f_{IN} x N_{SW} where $I_{CC} = I_{CC\_VCC}$ + $I_{CC\ VL}$ and N_{SW} = total number of outputs switching.

STATIC POWER CONSUMPTION (T_A = +25°C)

Symbol	Parameter	Test Conditions	V_{CC} (V) (Note 18)	V_L (V) (Note 19)	Typ (Note 20)	Unit
C_{PD_VL}	V_L = Input port, V_{CC} = Output Port	C_{Load} = 0, f = 1 MHz, EN = GND (outputs disabled)	0.9	4.5	0.01	pF
			1.5	1.8	0.01	
			1.8	1.5	0.01	
			1.8	1.8	0.01	
			1.8	2.8	0.01	
			2.5	2.5	0.01	
			2.8	1.8	0.01	
			4.5	0.9	0.01	
	V_{CC} = Input port, V_L = Output Port	C_{Load} = 0, f = 1 MHz, EN = GND (outputs disabled)	0.9	4.5	0.01	pF
			1.5	1.8	0.01	
			1.8	1.5	0.01	
			1.8	1.8	0.01	
			1.8	2.8	0.01	
			2.5	2.5	0.01	
			2.8	1.8	0.01	
			4.5	0.9	0.01	
C_{PD_VCC}	V_L = Input port, V_{CC} = Output Port	C_{Load} = 0, f = 1 MHz, EN = GND (outputs disabled)	0.9	4.5	0.01	pF
			1.5	1.8	0.01	
			1.8	1.5	0.01	
			1.8	1.8	0.01	
			1.8	2.8	0.01	
			2.5	2.5	0.01	
			2.8	1.8	0.01	
			4.5	0.9	0.01	
	V_{CC} = Input port, V_L = Output Port	C_{Load} = 0, f = 1 MHz, EN = GND (outputs disabled)	0.9	4.5	0.01	pF
			1.5	1.8	0.01	
			1.8	1.5	0.01	
			1.8	1.8	0.01	
			1.8	2.8	0.01	
			2.5	2.5	0.01	
			2.8	1.8	0.01	
			4.5	0.9	0.01	

18. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +0.9 V to 4.5 V under normal operating conditions.
19. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +0.9 V to 4.5 V under normal operating conditions.
20. Typical values are at T_A = +25°C

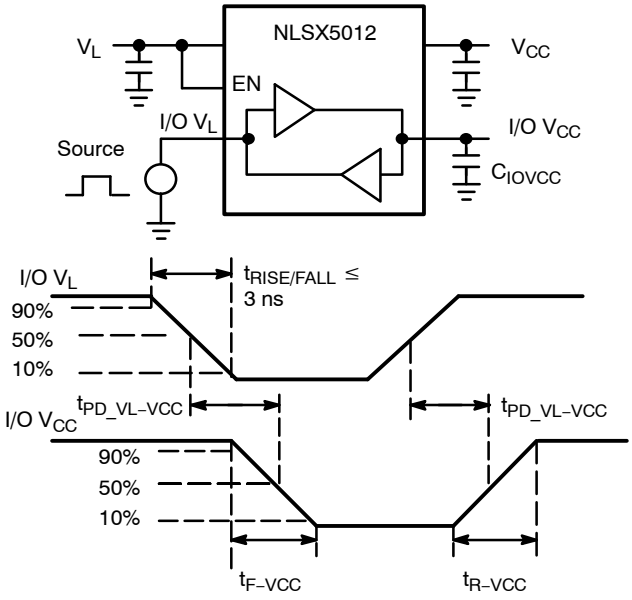


Figure 7. Driving I/O V_L Test Circuit and Timing

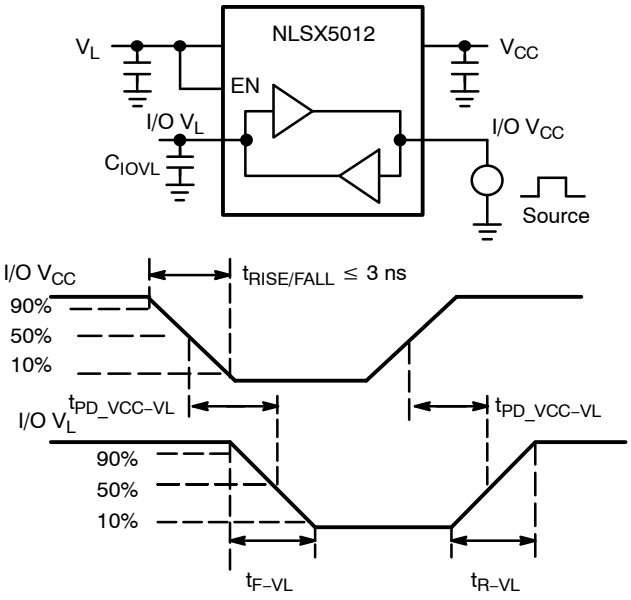
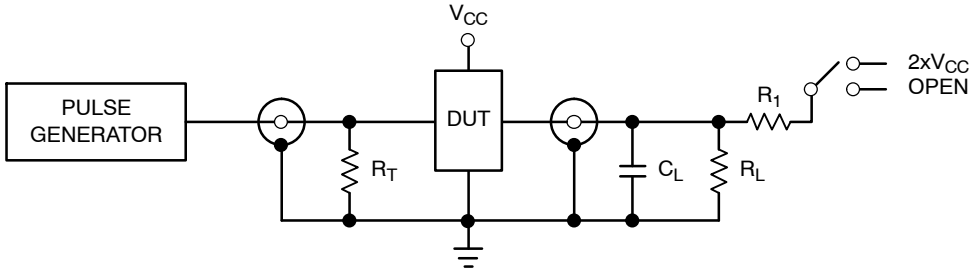


Figure 8. Driving I/O V_{CC} Test Circuit and Timing



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 9. Test Circuit for Enable/Disable Time Measurement

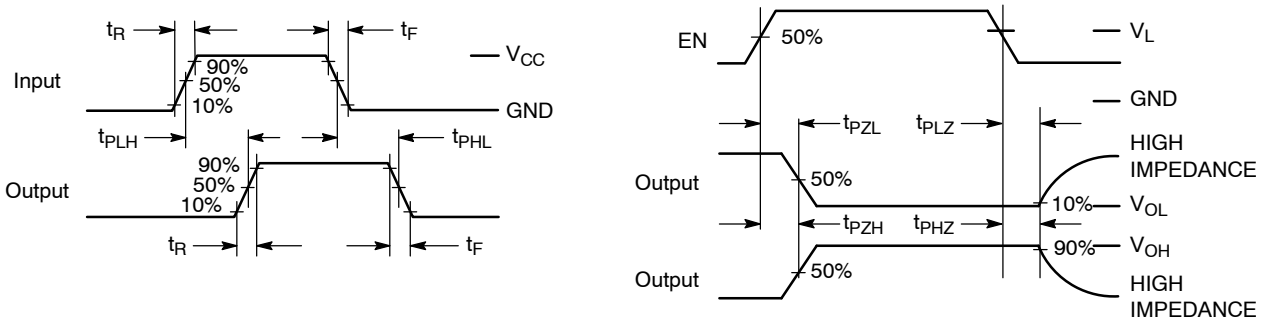


Figure 10. Timing Definitions for Propagation Delays and Enable/Disable Measurement

IMPORTANT APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX5012 auto−sense translator provides bi−directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_L to the I/O V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the I/O V_{CC} to I/O V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX5012 translator consists of bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. One−shot circuits are used to detect the rising or falling input signals. In addition, the one−shots decrease the rise and fall times of the output signal for high−to−low and low−to−high transitions.

Input Driver Requirements

Auto−sense translators such as the NLSX5012 have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi−directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent in the opposite direction. For proper operation, the input driver to the auto−sense translator should be capable of driving 2 mA of peak output current. The bi−directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

Enable Input (EN)

The NLSX5012 translator has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over−Voltage Tolerant (OVT) protection.

Uni−Directional versus Bi−Directional Translation

The NLSX5012 translator can function as a non−inverting uni−directional translator. One advantage of using the translator as a uni−directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni−directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

The values of the V_L and V_{CC} supplies can be set to anywhere between 0.9 and 4.5 V. Design flexibility is maximized because V_L may be either greater than or less than the V_{CC} supply. In contrast, the majority of the competitive auto sense translators has a restriction that the value of the V_L supply must be equal to less than (V_{CC} − 0.4) V.

The sequencing of the power supplies will not damage the device during power−up operation. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V. For optimal performance, 0.01 to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

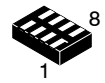
The NLSX5012 translators have a power down feature that provides design flexibility. The output ports are disabled when either power supply is off (V_L or V_{CC} = 0 V). This feature causes all of the I/O pins to be in the power saving high impedance state.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

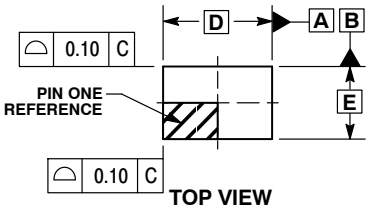
ON Semiconductor®

UDFN8 1.8x1.2, 0.4P
CASE 517AJ−01
ISSUE O

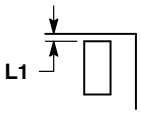
DATE 08 NOV 2006



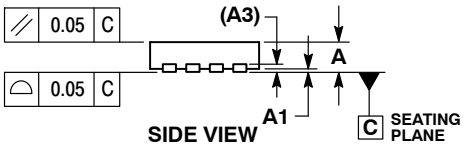
SCALE 4:1



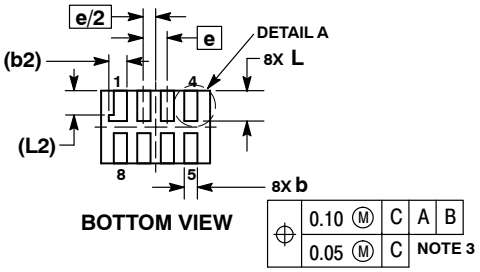
TOP VIEW



DETAIL A
NOTE 5



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

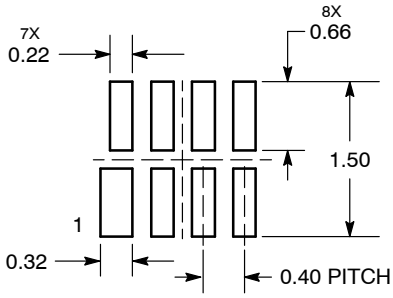
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON23417D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**UDFN8 1.8X1.2, 0.4P**		**PAGE 1 OF 1**

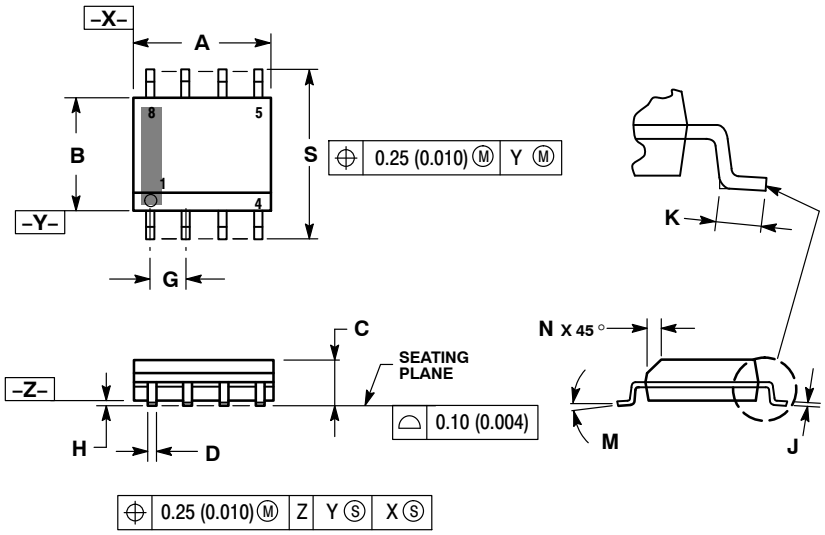
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

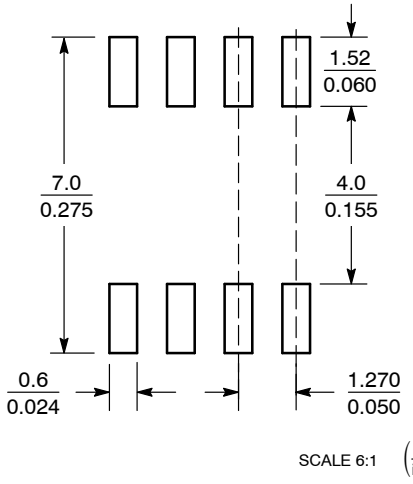
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

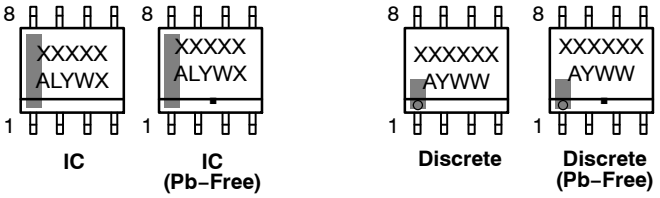
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

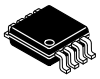
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

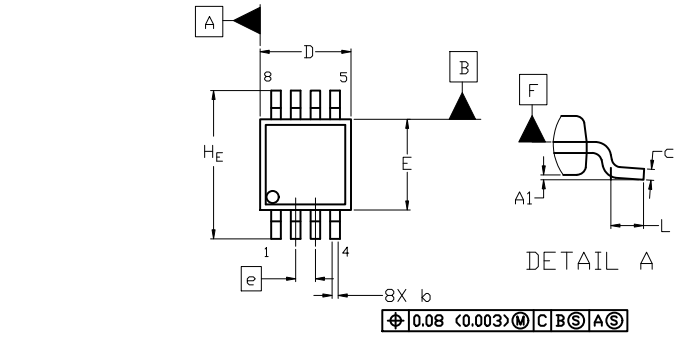
ON Semiconductor®

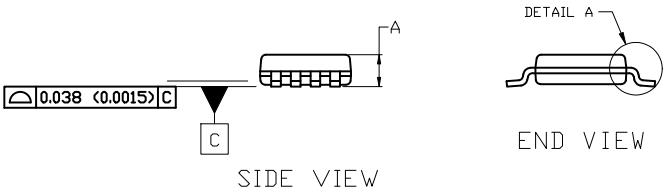


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

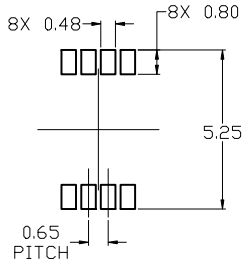
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

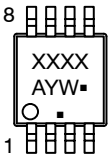


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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