NLU1GT86

Single 2-Input Exclusive OR Gate, TTL Level

LSTTL−Compatible Inputs

The NLU1GT86 MiniGate™ is an advanced CMOS high−speed 2−input Exclusive OR gate in ultra−small footprint.

The device input is compatible with TTL−type input thresholds and the output has a full 5.0 V CMOS level output swing.

The NLU1GT86 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} = 3.1 ns (Typ) @ V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- TTL−Compatible Input: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- CMOS−Compatible Output:
  $V_{OH} > 0.8 \, V_{CC}$; $V_{OL} < 0.1 \, V_{CC}$ @ Load
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
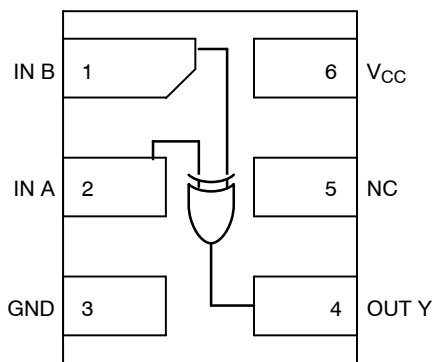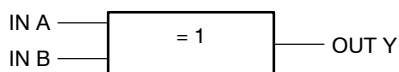- Ultra−Small Packages
- These are Pb−Free Devices

ON Semiconductor®

MARKING DIAGRAMS

UDFN6
1.2 x 1.0
CASE 517AA

6M

6 = Device Marking
M = Date Code

ORDERING INFORMATION

Figure 1. Pinout (Top View)

Figure 2. Logic Symbol

FUNCTION TABLE

Input		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

PIN ASSIGNMENT

1	IN B
2	IN A
3	GND
4	OUT Y
5	NC
6	V_{CC}

July, 2016 – Rev. 4

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	$V_{IN} <$ GND	−20	mA
I_{OK}	DC Output Diode Current	$V_{OUT} <$ GND	±20	mA
I_O	DC Output Source/Sink Current		±12.5	mA
I_{CC}	DC Supply Current Per Supply Pin		±25	mA
I_{GND}	DC Ground Current per Ground Pin		±25	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 150 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
T_A	Operating Free−Air Temperature		−55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Low–Level Input Voltage		3.0 4.5 to 5.5	1.4 2.0			1.4 2.0		1.4 2.0		V
V_{IL}	Low–Level Input Voltage		3.0 4.5 to 5.5			0.53 0.8		0.53 0.8		0.53 0.8	V
V_{OH}	High–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5$ V	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25 °C			T_A = +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Input A to Output Y	3.0 to 3.6	C_L = 15 pF		5.0	11.0		13.0		15.5	ns
			C_L = 50 pF		6.2	14.5		16.5		19.5	
		4.5 to 5.5	C_L = 15 pF		3.1	6.8		6.0		10.0	
			C_L = 50 pF		4.2	8.8		10.0		12.0	
C_{IN}	Input Capacitance				5.5	10		10		10.0	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	5.0			11						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.
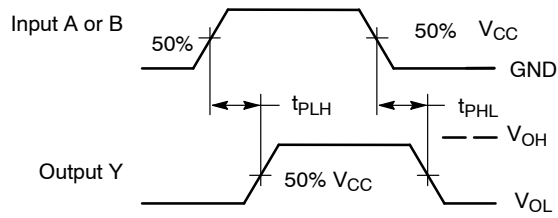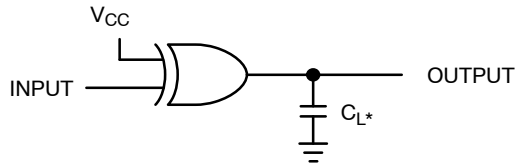
NLU1GT86

Figure 3. Switching Waveforms

*Includes all probe and jig capacitance.
A 1−MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NLU1GT86MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

UDFN6, 1.2x1.0, 0.4P
CASE 517AA–01
ISSUE D

DATE 03 SEP 2010

SCALE 8:1

1

PIN ONE REFERENCE

D | A
B

E

2X △ 0.10 C

TOP VIEW

2X △ 0.10 C

EDGE OF PACKAGE

L1

DETAIL A
Bottom View
(Optional)

EXPOSED Cu | **MOLD CMPD**

A3

A1

DETAIL B
Side View
(Optional)

// 0.10 C

(A3)

A

10X △ 0.08 C

SIDE VIEW

A1

C

SEATING PLANE

5X L

1 | 3

L2

6 | 4

6X b

⊕ 0.10 C A B
0.05 C **NOTE 3**

e

BOTTOM VIEW
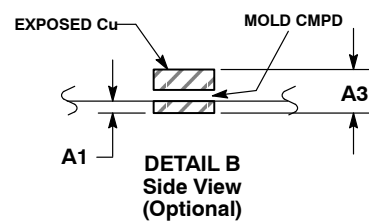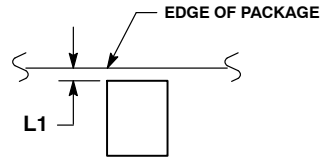
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	**MAX**
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

GENERIC
MARKING DIAGRAM*

X M
●

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪ ", may or may not be present.

MOUNTING FOOTPRINT*

6X
0.42

6X
0.22

0.40
PITCH

1.07
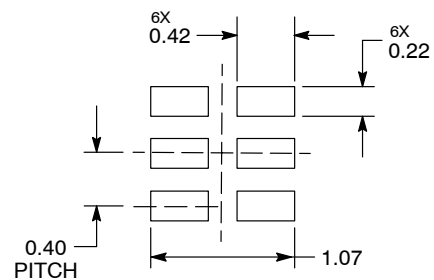
DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON22068D	
DESCRIPTION:	6 PIN UDFN, 1.2X1.0, 0.4P	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊

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NLV74HC02ADR2G 74HC32S14-13 74LS133 74LVC1G32Z-7 M38510/30402BDA 74LVC1G86Z-7 74LVC2G08RA3-7
NLV74HC08ADTR2G NLV74HC14ADR2G NLV74HC20ADR2G NLX2G86MUTCG 5962-8973601DA 74LVC2G02HD4-7
NLU1G00AMUTCG 74LVC2G32RA3-7 74LVC2G00HD4-7 NL17SG02P5T5G 74LVC2G00HK3-7 74LVC2G86HK3-7
NLX1G99DMUTWG NLVVHC1G00DFT2G NLVHC1G08DFT2G NLV7SZ57DFT2G NLV74VHC04DTR2G NLV27WZ86USG
NLV27WZ00USG NLU1G86CMUTCG NLU1G08CMUTCG NL17SZ32P5T5G NL17SZ00P5T5G NL17SH02P5T5G 74AUP2G00RA3-7
NLV74HC02ADTR2G NLX1G332CMUTCG NL17SG86P5T5G NL17SZ05P5T5G