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Dual Schmitt-Trigger Inverter

The NLU2G14 MiniGate[™] is an advanced high–speed CMOS dual Schmitt–trigger inverter in ultra–small footprint.

The NLU2G14 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

The NLU2G14 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- High Speed: $t_{PD} = 4.0 \text{ ns} (Typ) @ V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \ \mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb–Free Devices

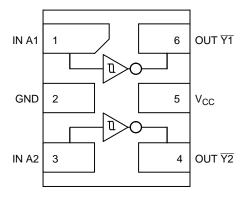


Figure 1. Pinout (Top View)



Figure 2. Logic Symbol

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT Y2
5	V _{CC}
6	OUT Y1

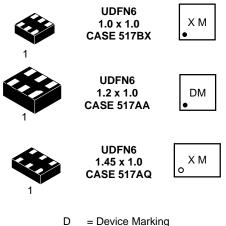
FUNCTION TABLE				
Α	Y			
L H	H L			



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MARKING DIAGRAMS



M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V	
V _{OUT}	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current	V _{OUT} < GND	±20	mA
Ι _Ο	DC Output Source/Sink Current	±12.5	mA	
I _{CC}	DC Supply Current Per Supply Pin	±25	mA	
I _{GND}	DC Ground Current per Ground Pin	±25	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
ΤL	Lead Temperature, 1 mm from Case for 10 Second	ds	260	°C
TJ	Junction Temperature Under Bias	150	°C	
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V–0 @ 0.125 in	
ILATCHUP	Latchup Performance Above V_{CC} and Below GND	±500	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free–Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	No Limit No Limit	ns/V

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	T _A = 25 °C		T _A = +85°C		T _A = −55°C to +125°C			
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{T+}	Positive Threshold Voltage		3.0 4.5 5.5	1.85 2.86 3.50	2.0 3.0 3.6	2.2 3.15 3.85		2.2 3.15 3.85		2.2 3.15 3.85	V
V _{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65	1.5 2.3 2.9	1.65 2.46 3.05	0.9 1.35 1.65		0.9 1.35 1.65		V
V _H	Hysteresis Voltage		3.0 4.5 5.5	0.30 0.40 0.50	0.57 0.67 0.74	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	0.30 0.40 0.50	1.20 1.40 1.60	V
V _{OH}	Minimum High–Level Output	$V_{IN} \le V_{T-MIN}$ I_{OH} = -50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
	Voltage	$\begin{array}{l} V_{IN} \leq V_{T-MIN} \\ I_{OH} = -4 \text{ mA} \\ I_{OH} = -8 \text{ mA} \end{array}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Maximum Low–Level Output	$V_{IN} \ge V_{T+MAX}$ $I_{OL} = 50 \ \mu A$	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
	Voltage	$\begin{array}{l} V_{IN} \geq V_{T+MAX} \\ I_{OL} = 4 \text{ mA} \\ I_{OL} = 8 \text{ mA} \end{array}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I _{CC}	Quiescent Supply Current	$0 \le V_{IN} \le V_{CC}$	5.5			1.0		10		40	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

		V _{CC}	Test		T _A = 25 °	с	T _A =	+85°C	T _A = -5 +12	55°C to 5°C	
Symbol	Parameter	(V)	Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay,	3.0 to	C _L = 15 pF		7.0	12.8	1.0	15	1.0	17	ns
t _{PHL}	Input Ă to Output Ÿ	3.6	C _L = 50 pF		8.5	16.3	1.0	18.5	1.0	20.5	
		4.5 to	C _L = 15 pF		4.0	8.6	1.0	10	1.0	11.5	
		5.5	C _L = 50 pF		5.5	10.6	1.0	12	1.0	13.5	
C _{IN}	Input Capacitance				5.0	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 3)	5.0			7.0						pF

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

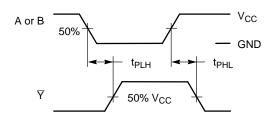
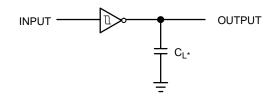
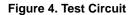


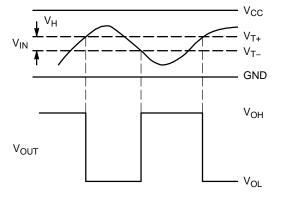
Figure 3. Switching Waveforms

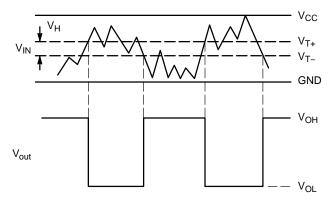


*Includes all probe and jig capacitance.

A 1–MHz square input wave is recommended for propagation delay tests.







(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt–Trigger Offers Maximum Noise Immunity

Figure 5. Typical Schmitt-Trigger Applications

ORDERING INFORMATION

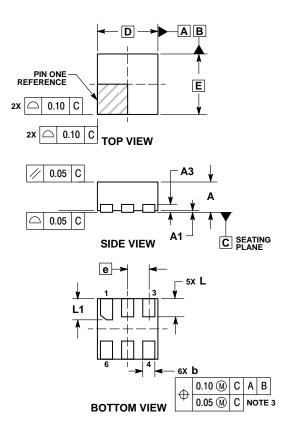
Device	Package	Shipping [†]
NLU2G14MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb–Free)	3000 / Tape & Reel
NLU2G14AMUTCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb–Free)	3000 / Tape & Reel
NLU2G14CMUTCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4

PACKAGE DIMENSIONS

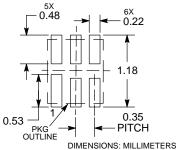
UDFN6 1.0x1.0, 0.35P CASE 517BX ISSUE O



- NOTES:
 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 PACKAGE DIMENSIONS EXCLUSIVE OF BUIDES AND MOLD EI ASH ASH.

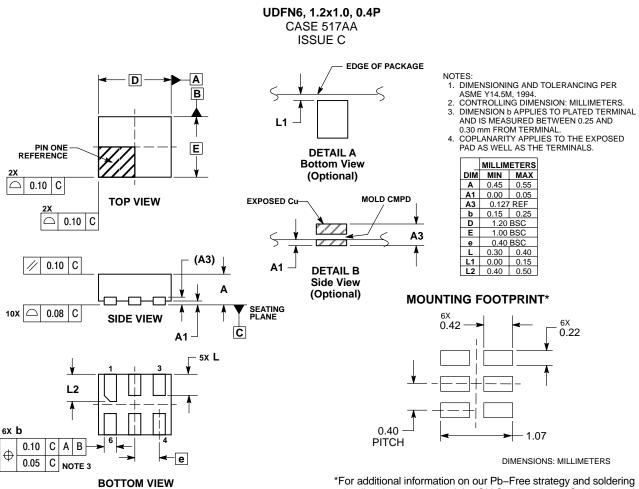
BURF	BURRS AND MOLD FL					
	MILLIMETERS					
DIM	MIN MAX					
Α	0.45	0.55				
A1	0.00	0.05				
A3	0.13 REF					
b	0.12 0.22					
D	1.00	BSC				
E	1.00	BSC				
е	0.35 BSC					
L	0.25	0.35				
L1	0.30 0.40					

RECOMMENDED SOLDERING FOOTPRINT*



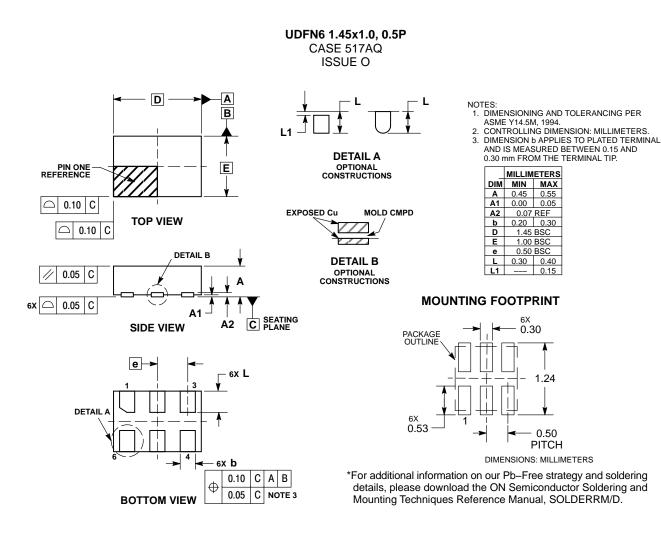
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS



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PACKAGE DIMENSIONS



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